

Ultra Long-term Measurement Results of BTI-induced Aging Degradation on 7-nm Ring Oscillators

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Abstract— We measured ultra-long term BTI-induced degradation of 7-nm ring oscillators (ROs) using a measurement system controlled by an FPGA and a microcontroller unit. The ambient temperature and the supply voltage were set to 125°C and the nominal voltage of 0.75 V. The measurement results showed that even over a very long period around 5 months (1e7 s), the RO oscillation frequency continuously degraded with t^n . We propose a degradation model in which BTI-induced traps are increasing as time. The model can successfully replicate the continuous ever-lasting-like degradation.

Keywords— BTI, long-term, recovery, ring oscillator, FinFET

I. INTRODUCTION

Due to the aggressive process scaling, aging degradation is becoming one of important concerns in semiconductor chips for automotive and other mission-critical applications. Acceleration tests are widely used to measure aging degradation. In acceleration tests, voltage and temperature are raised above a nominal operating point to accelerate degradation. Many research papers measured aging degradation by device or circuit levels. But almost all measurement results were terminated at 10^3 - 10^5 s [1], [2]. Although DUTs (Device Under Tests) are exposed to some accelerated condition with additional stress voltage and high ambient temperature, such short-term measurement data cannot precisely predict aging degradation becoming dominant after a long period.

The paper [3] shows measurement results of built-in ROs in IBM z196 processors fabricated by a 45nm SOI technology over 500 days. In this paper, we firstly reported measurement results of aging degradation of ring oscillators (ROs) in a 7nm FinFET technology over 100 days.

We constructed a measurement system of aging degradation for a ultra long term with an FPGA (Field Programmable Gate Array) and a microcontroller unit (MCU) that can periodically measure frequency degradation of 7-nm ring oscillators (ROs) with the nominal operating voltage of 0.75 V placed in a constant temperature oven at 125°C. We propose a degradation model in which BTI-induced traps are increasing as time. The model can successfully replicate the continuous ever-lasting-like degradation.

II. ULTRA LONG-TERM MEASUREMENT SYSTEM

In order to measure aging degradation on a chip in a circuit level, engineering testers or other measuring instruments are convenient to generate control signals and acquire measurement data. Our previous measurements in [2], [4], [5], [6]



Fig. 1: Short-term measurement system of aging degradation using an engineering tester (left) and a Peltier element (right).

utilized engineering testers and a Peltier element on DUTs as shown in Fig. 1. They cannot keep on running for a long period by the following reasons.

- Engineering testers must be shared by many researches or developments
- They are hard to keep operating for a long period due to power outage or periodical security updates of an operating system.

To overcome the above issues, we constructed a measurement system with the FPGA and the MCU as shown in Figs. 2 and 3. The FPGA generates control signals and obtains output signals from a DUT (7nm chip) with a specified clock frequency. The MCU executes a bare-metal code to control the FPGA and the external power supply to obtain measurement results, and to communicate occasionally with a PC. When the PC is connected to the MCU through the serial interface, measured data stored in internal data memory of the MCU after the latest connection are transferred. The DUT is placed in the constant temperature oven. The core voltage (VDD) of the DUT is supplied from the stable external commercial DC power supply. The ambient temperature in the oven is periodically monitored through the network interface of the temperature oven. A thermocouple is also attached to the surface of the DUT. The temperature on the thermocouple was logged every 10 s by a Raspberry Pi through the digital multimeter. The measured surface temperature is 123.8°C, while the ambient temperature in the oven is 125°C. The list of all parts in the measurement system is as follows.

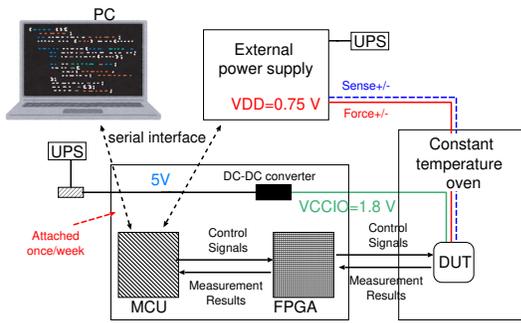


Fig. 2: Schematic diagram of the implemented ultra long-term measurement system with an FPGA and an MCU.

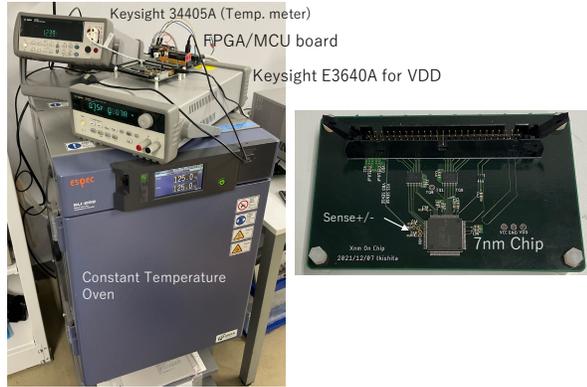


Fig. 3: Photo of the measurement system (left) and the chip board in constant the temperature oven (right).

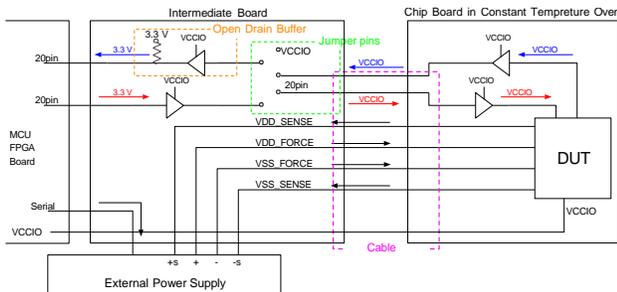


Fig. 4: Schematic diagram of two PCB boards: the intermediate and chip board outside and inside the constant temperature oven respectively.

FPGA/MCU board: Intel Cyclone IV EP4CE30F2317N / Renesas RX210 R5F52108ADFP on MMS MU500-RX.

Constant temperature oven: ESPEC SU-222

External power supply: Keysight E3640A

Digital multimeter: Keysight 34405A

Print circuit boards (PCBs): Designed by our lab. and fabricated by a Japanese PCB company.

The IO voltage ($V_{CCIO} = 1.8 \text{ V}$) is supplied from the MCU/FPGA board by the on-board DC-DC converter since the small change of V_{CCIO} does not influence measurement results. The force and sense lines of VDD from the external supply are short-circuited on the chip board (so called Kelvin

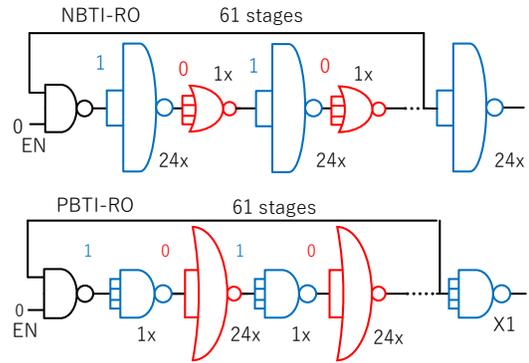


Fig. 5: NBTI-sensitive RO (NBTI-RO) and PBTI-sensitive RO (PBTI-RO).

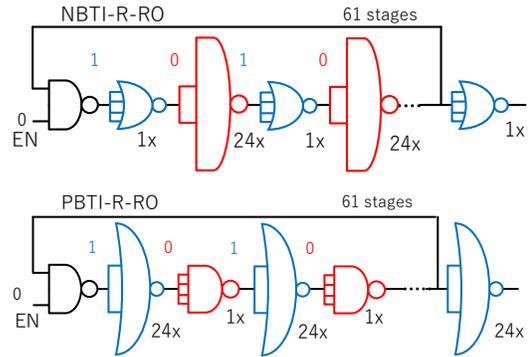


Fig. 6: NBTI-reversely-sensitive RO (NBTI-R-RO) and PBTI-reversely-sensitive RO (PBTI-R-RO).

connection) in order to compensate an unexpected voltage drop during the long-term measurement. Fig. 4 depicts the schematic diagram of two PCB boards. The intermediate board attached to the FPGA/MCU board has buffers to convert the IO voltage of the DUT (1.8 V) to that of the FPGA (3.3 V). The input buffers to the FPGA are open drain buffers that can convert V_{CCIO} to 3.3 V. The 20 IO pins on the intermediate board can be configured to input, output or pullup pins by jumper pins. Thus the intermediate board can be used for other DUTs with IO pins less than 20.

The whole measurement system protected by the UPS (Uninterruptible Power Supply) is capable of operating without interruption at sudden power failures. It can continuously keep operating over several months.

We constructed the measurement system that can keep on operating for a long period. We excluded measuring instruments that cannot be used for a long period due to its heavy power consumption. The measurement system only includes the commercial DC power supply with small power consumption that can run for a short time with the UPS. The commercial power supply is indispensable to guarantee the supply of an accurate voltage level to the DUT. The constant temperature oven turns off at power outage, but ambient temperature inside the oven does not change for short-time outage. It can continue to run powered by an external power generator for long scheduled power outage.

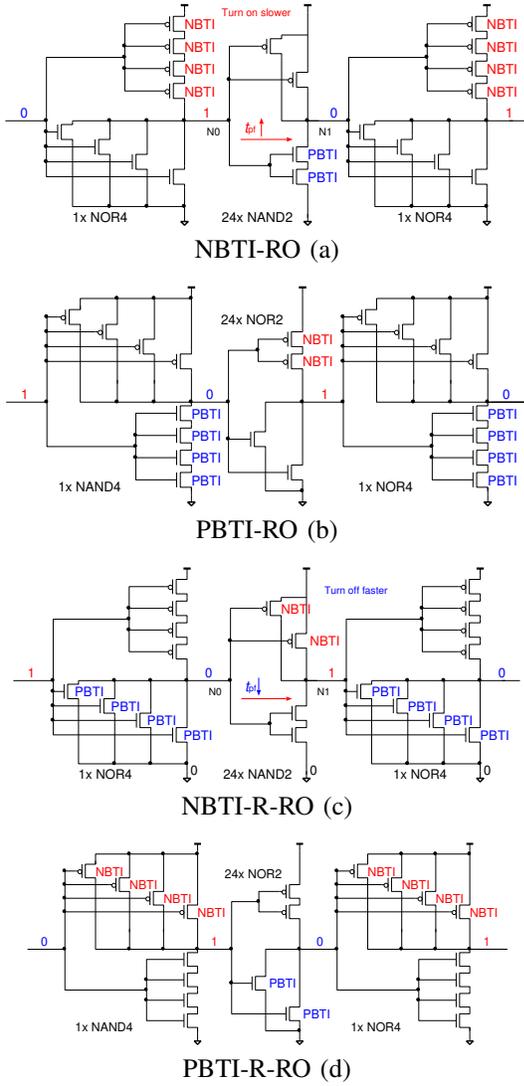


Fig. 7: Schematic diagrams of ROs and the bias conditions when they stop oscillation. P/NMOSFETs marked by “NBTI/PBTI” is negatively or positively biased between the gate and source terminals.

III. 7-NM X-BTI SENSITIVE OR REVERSELY-SENSITIVE RING OSCILLATORS

Fig. 5 shows ring oscillators sensitive to NBTI and PBTI [7] called “NBTI-RO” and “PBTI-RO” respectively. Fig. 6 shows ring oscillators reversely sensitive to NBTI and PBTI called “NBTI-R-RO” and “PBTI-R-RO” respectively. They are constructed with all-input-shortened NAND and NOR gates in order to change delay characteristics unevenly by BTI-induced stress. All ROs consists of 61 stages and the number of transistors is 372. When they stop oscillation, some MOSFETs in the NOR and NAND gates suffer from PBTI and NBTI stress. BTI stress makes PBTI-RO and NBTI-RO slower but PBTI-R-RO and NBTI-R-RO faster due to the difference of the structures and the multiplicity of logic gates in the odd and even stages. Note that they only

TABLE I. RO frequency shifts on SVT (Standard Vth) by NBTI/PBTI stresses at 50 mV Vth degradation. “-” means that the RO oscillates faster than at no stress.

	by NBTI	by PBTI	Total
NBTI-RO	22.8%	2.2%	25.0%
PBTI-RO	2.6%	20.0%	22.7%
NBTI-R-RO	-5.5%	1.2%	-4.3%
PBTI-R-RO	1.5%	-5.1%	-3.5%

oscillate during a short period of 400 μ s after relatively long stress time (from 1 s to 28,800 s). During the long stress time, the feedback loops of the ROs are all open and stop oscillation. Therefore, other degradation issues such as HCD (Hot Carrier Degradation) can be ignored. As for soft and hard breakdown of gate oxide, no leakage current increase was observed and all ROs keep on oscillating after the long period of stress time up to $1e7$ sec.

The transistor-level schematics of all ROs are depicted in Fig. 7. When NBTI-RO stops oscillation, PMOSFETs in the 1x NOR4 gates and NMOSFETs in the 24x NAND2 gates are exposed to NBTI and PBTI stress respectively. On the other hand, in NBTI-R-RO, PMOSFETs in the 24x NAND2 gates and NMOSFETs in the 1x NOR4 gates suffer from NBTI and PBTI stress respectively. The unsymmetrical rise and fall delay time of the 1x NOR4 or 24x NAND4 gates make those ROs faster or slower. The difference between the NBTI (PBTI) and NBTI-R (PBTI-R) ROs are the voltage levels when they stop oscillation. For example, the input level of the 1x NOR gates in NBTI-RO are high (1), while in NBTI-R-RO is low (0).

The 1x NOR4 gates in NBTI-RO suffer from NBTI during the stress phase as in Fig. 7(a). Since the 1x NOR4 gates in NBTI-RO has 4-series-stack PMOSFETs, the fall propagation delay (t_{pf}) between N0 and N1 is dominant to determine the NBTI-RO’s oscillation frequency. When PMOSFETs in the 1x NOR4 gates are degraded, the oscillation frequency of NBTI-RO is decreased. On the other hand, When the PMOSFETs in the 24x NAND2 gates in NBTI-R-RO are degraded, t_{pf} becomes shorter since degraded PMOSFETs in the 24x NAND2 gates turn off faster than fresh PMOSFETs. Thus the oscillation frequency of NBTI-RO is increased.

Table I shows simulation results of frequency shifts at 50 mV threshold voltage (Vth) degradation. We assume that all of the MOSFETs marked by NBTI/PBTI in Fig. 7 are equally degraded due to NBTI or PBTI stress for simplicity. The NBTI-ROs becomes slower, while the N/PBTI-R-ROs become faster as expected.

IV. TEST PROCEDURE

By using the measurement system in Fig. 2 and the 7nm chip including the ROs in Figs. 5 and 6, we have been measuring RO frequencies for a long period. First, the DUT-board was put inside the constant temperature oven. After the temperature was settled around after 30 minutes, the MCU started measurement. The external voltage source was turned on and the first measurement at $t = 1$ was done. The stress time (t_{stress}) was gradually prolonged as shown in Fig. 8. After t_{stress} became 32 s, t_{stress} was doubled every time until

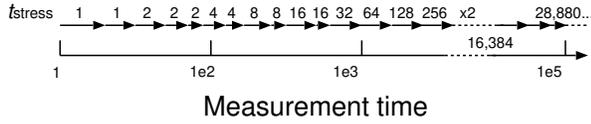
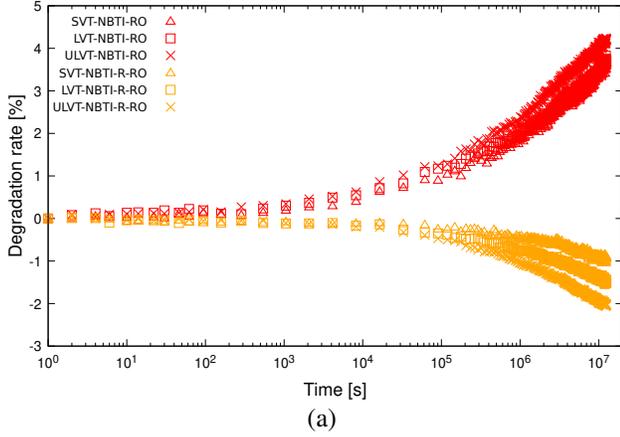
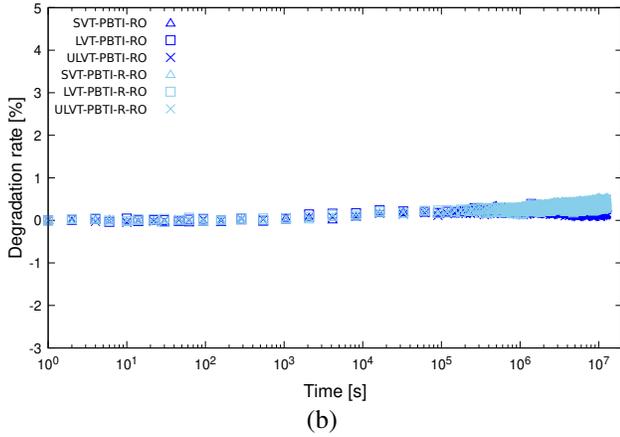


Fig. 8: Time table of t_{stress} .



(a)



(b)

Fig. 9: Degradation rate of frequency of NBTI-RO (a) and PBTI-RO (b).

t_{stress} was 16,384 s. After that, the oscillation frequencies were measured at every 28,800 s (8 hours). The MCU can store 25 measurement results in internal SRAMs. After the stress time became 28,800 s, the PC was attached to the MCU once in week so as to collect 21 (7×3) measurement results in a week.

V. MEASUREMENT RESULTS

We have been measuring BTI-induced degradation of the ROs fabricated in the 7nm FinFET technology by the measurement system as depicted in Fig. 2 at the ambient temperature of 125°C , the chip-surface temperature of 123.8°C and $V_{\text{DD}} = 0.75\text{ V}$ (nominal voltage in the 7nm FinFET). Each RO was implemented with 3 Vth flavors of standard, low and ultra-low threshold voltage levels (SVT, LVT and ULVT). Note that only a single RO of each structure with each Vth flavor is implemented on a chip. Fig. 9 shows the measurement results until $1.25e7\text{ s}$ (≈ 144 days). The y-axis

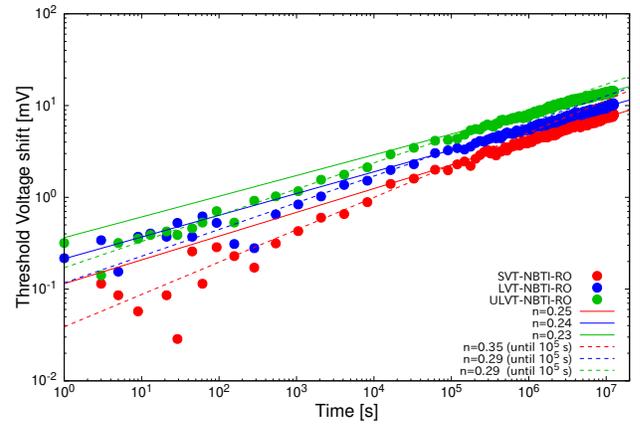


Fig. 10: Vth shifts of NBTI-ROs in log-log scale.

is the degradation rate in the linear scale. The degradation rate ($r_{\text{deg}}(t)$) is computed by Eq. 1, where $f(t)$ is the oscillation frequency at t .

$$r_{\text{deg}}(t) = \frac{f(t) - f(1)}{f(1)}, \quad (1)$$

As the results in Table I, all NBTI-ROs have become slower (degraded), while all NBTI-R-ROs have become faster. On the other hand, the RO frequencies of all PBTI-ROs and PBTI-R-ROs are almost flat throughout the measurement time. The degradation and recovery rates of SVT-NBTI-RO and SVT-NBTI-R-RO are 3.62% and 0.91% at $1.25e7\text{ s}$ as shown in Fig. 9 (a). As shown in Fig. 9 (b), PBTI can be ignored. So the ratio (-0.24) between the recovery rate (-5.5%) of NBTI-R-RO and the degradation rate (22.8%) of NBTI-RO by NBTI obtained from the simulations in Table I is almost consistent to that by the measurement results ($-0.25 = -0.91\%/3.62\%$).

The NBTI-ROs have NMOSFETs that may be degraded by PBTI. But as shown in Fig. 9, PBTI-induced degradation can be ignored. Thus, we assume that all the degradation comes only from NBTI on PMOSFETs. We assume that all of the PMOSFETs are equally degraded by NBTI. Fig. 10 shows the NBTI-induced Vth shifts of PMOSFETs of all NBTI-ROs in the log scale. It clearly shows the Vth shifts are increased by t^n until the end of the measurement period at $1.25e7\text{ s}$. But the time exponents n before $1e6\text{ s}$ are bigger than those after $1e6\text{ s}$. After $1e6\text{ s}$, the time exponents n of all NBTI-ROs are around 0.25 (1/4) which is inconsistent with the value of 1/6 in [1]. But [1] and [8] pointed out that n becomes larger due to larger delay associated with measurements. In our measurement system, the ROs oscillate for $400\ \mu\text{s}$ at the measurement phase. [8] also reveals that the time exponents of thin gate PMOS FinFETs are over 0.20 at 175°C .

The time exponent of SVT (0.25) is biggest which shows contradictory trends that the BTI-induced degradation is reversely proportional to the threshold voltage[9]. But in [10], the thermal budget applied after the deposition of the gate metal improved reliability of low-Vth devices. Some

veiled process flow may affect the measured degradation trends by V_{th} .

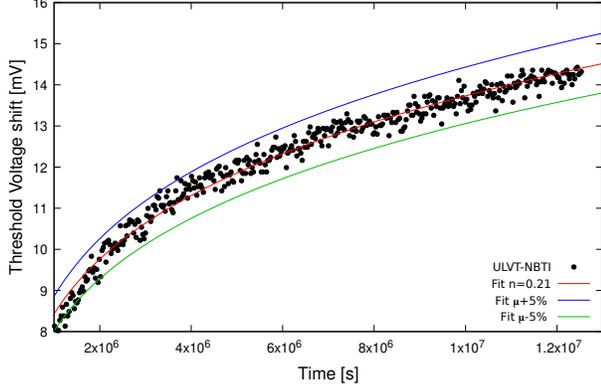


Fig. 11: V_{th} shifts of ULVT-NBTI-RO in semi-log scale. “ $\mu \pm 5\%$ ” shows the region between +5% and -5% from the fit curve in red.

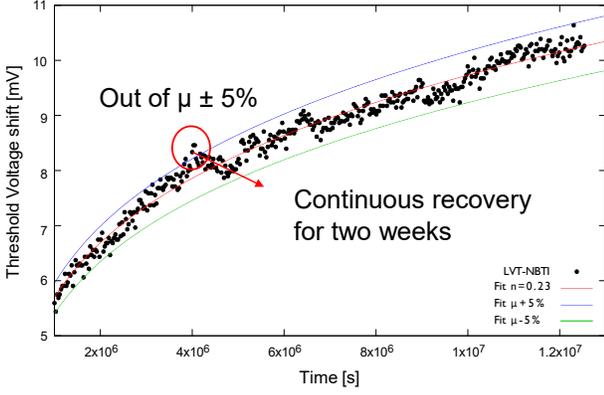


Fig. 12: V_{th} shifts of LVT-NBTI-RO in semi-log scale.

Figs. 11-13 depict the V_{th} shifts from $1e6$ s to $1.25e7$ s. in the linear scale. All plots are almost within the region between +5% and -5% from the fit curve. But in LVT-NBTI-RO, Some plots are outside of the $\pm 5\%$ region. In addition to that V_{th} recovered around $5e6$ s. for over two weeks ($\approx 1e6$ s). However, the other ROs (SVT-NBTI-RO and ULVT-NBTI-RO) have no such tendency. We have to investigate the origin of those variations and continuous recovery.

VI. NUMERICAL SIMULATIONS TO REPLICATE EVER-LASTING-LIKE BTI-INDUCED DEGRADATION

We are now going to replicate the continuous degradation up to 10^7 s by proposing a model in which the number of traps related to the BTI-induced degradation is increasing as time.

Fig. 14 plots the standard deviation $\sigma_{\Delta V_{th}}/\Delta V_{th}$ of the separations between the average of five adjacent ΔV_{th} values and the fitting function ($a \cdot t^n$). It clearly shows the standard deviations are decreasing as the stress time is increasing. It suggests that the number of traps (n_{traps}) which contribute BTI-induced degradation is increasing as stress time.

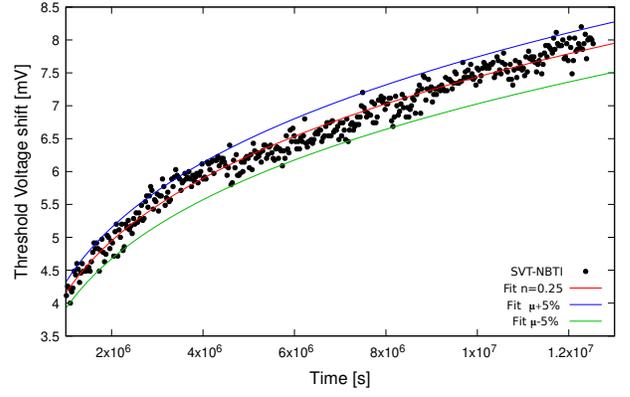


Fig. 13: V_{th} shifts of SVT-NBTI-RO in semi-log scale.

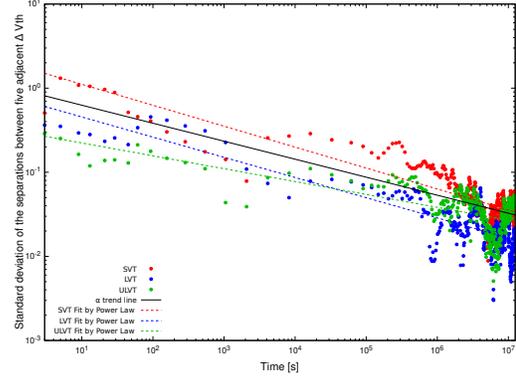


Fig. 14: Standard deviation of the separations between five adjacent ΔV_{th} values and fitting functions ($a \cdot t^n$).

$\sigma_{\Delta V_{th}}(t)/\Delta V_{th}$ can be expressed by Eq. 2.

$$\sigma_{\Delta V_{th}}(t)/\Delta V_{th} = (\sigma_{\Delta V_{th}}(0)/\Delta V_{th})/\sqrt{n_{traps}}, \quad (2)$$

The standard deviations in Fig. 14 follows Eq. 3, where b and m are fitting parameters.

$$\sigma_{\Delta V_{th}}(t)/\Delta V_{th} = b \cdot t^{-m}, \quad (3)$$

Thus, n_{traps} follows Eq. 4.

$$n_{traps} = (\sigma_{\Delta V_{th}}(0)/b) \cdot t^{2m}. \quad (4)$$

The statistical transition of trapped carriers in gate oxide is described by Eq. 5 from rate equations, where $f_T(t)$ is the occupancy rate of a carrier in a trap, τ_c is the time constant to capture (trap) a carrier and τ_e is the time constant to emit (detrap) a carrier. Solving Eq. 5 with $f_T(0) = 0$, Eq. 6 is obtained, where $\frac{\tau_e}{\tau_e + \tau_c}$ is the occupancy rate at the thermal equilibrium state ($t = \infty$) and $\frac{\tau_e + \tau_c}{\tau_e \tau_c}$ is the effective time constant.

$$\frac{df_T(t)}{dt} = -\frac{f_T(t)}{\tau_e} + \frac{1 - f_T(t)}{\tau_c}, \quad (5)$$

$$f_T(t) = \frac{\tau_e}{\tau_e + \tau_c} \left[1 - \exp\left(-\frac{\tau_e + \tau_c}{\tau_e \tau_c} t\right) \right], \quad (6)$$

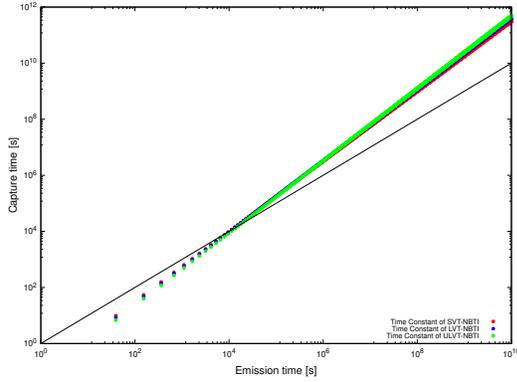


Fig. 15: Three trap distributions to replicate continuous degradation of three ROs with the time exponent n . The black line is $\tau_c = \tau_e$.

The number of traps has been increasing as stress time as described in the previous paragraph, while the degradation time exponent n is almost constant. It means that the number of filled traps has been decreasing as stress time. So we assume the simple trap distributions in Fig. 15 where all traps exist above the line of $\tau_c = \tau_e$ after $1e4$ s. Thus the number of filled traps are decreasing as stress time after $1e4$ s. The cumulative distribution of the traps follows Eq. 4. The tilt angles and Y intercepts are adjusted to follow the degradation curves with n . We assume the simple trap distribution ignoring traps far from the line along $\tau_c = \tau_e$ ($y = x$) since those traps are almost always filled ($\tau_c \ll \tau_e$) or vacant ($\tau_c \gg \tau_e$).

Figs. 16-18 show the simulation results. The dots before $1e2$ - $1e4$ s do not follow the fitting function of $a \cdot t^n$ since the number of BTI-induced traps are small. But after $1e2$ - $1e4$ s, the degradation trends follow $a \cdot t^n$.

Many physics-based complicated BTI degradation models have been proposed [11], [12], [13], [14]. But the proposed simple model obtained from the standard deviations of the separation of ΔV_{th} can replicate the ever-lasting-like BTI-induced degradation up to $1e7$ s. But we must investigate some physics-based model to explain the origin of the proposed model with the increased trends of BTI-induced traps.

VII. CONCLUSION

We constructed the long-term measurement system of aging degradation of the 7-nm ROs and have been measuring frequency degradation over $1e7$ s. The measurement results shows continuous degradation with the time exponent around 0.25. Numerical simulations based on a simple trap distribution obtained from the standard deviations of measured ΔV_{th} can replicate the ultra-long-term ever-lasting-like BTI degradation.

We must construct a physics-based model to replicate the trend where the number of BTI-induced trap is increasing as stress time.

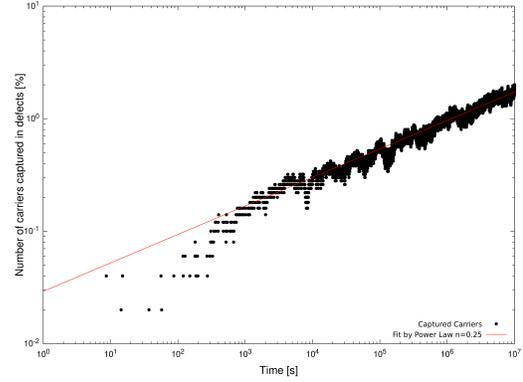


Fig. 16: Simulation results replicating the measurement result of SVT-RO.

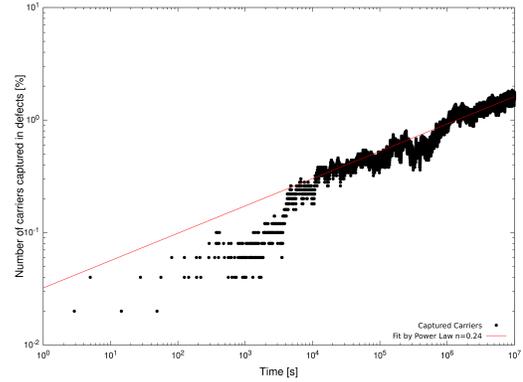


Fig. 17: Simulation results replicating the measurement result of LVT-RO.

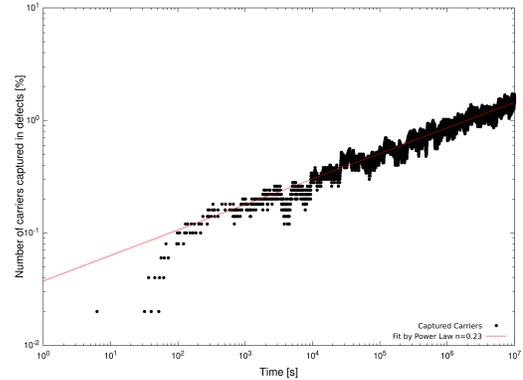


Fig. 18: Simulation results replicating the measurement result of ULVT-RO.

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