Radiation Hardness Evaluations of a Stacked Flip Flop in a 22 nm FD-SOI Process by Heavy-Ion Irradiation

Shotaro Sugitani∗, Ryuichi Nakajima∗, Takafumi Ito∗, Jun Furuta∗, Kazutoshi Kobayashi∗,
Mathieu Louvat†, Francois Jacquet†, Jean-Christophe Eloy†, Olivier Montfort†, Lionel Jure†, and Vincent Huard†
∗Dept. of Electronics, Kyoto Institute of Technology, Japan
†Dolphin Design, France

***Abstract*—In 22 nm FDSOI, the flip-well structure is used instead of the standard-well structure. We evaluated soft-error tolerance by heavy-ion irradiation tests on standard and stacked flip-flops (STDFF and STACKEDFF) in the flip-well structure. The error probability of STACKEDFF was significantly smaller than STDFF. Therefore, the stacked structure is also effective against soft error in the flip-well structure. However, as the supply voltage is lowered, even STACKEDFF becomes vulnerable to soft errors under certain conditions. The origin of these errors was pMOSFETs. Therefore, soft error countermeasures are needed to account for errors from pMOSFETs.**

***Index Terms*—single event effects, soft error, heavy ion, FDSOI, radiation hard, flip-well, flip-flop**

I. Introduction

Reliability issues such as radiation-induced soft errors become more serious with technology down scaling [1]. Soft errors are one of the temporal failures that upset stored values in storage elements such as flip-flops (FFs) or SRAMs caused by a radiation strike.

In the device level, a fully-depleted silicon on insulator (FDSOI) is strong against soft errors [2]. In FDSOI, a buried oxide (BOX) layer prevents charge collection by drift and funneling from substrate [3]. However, soft errors still occur on FFs on FDSOI structures. Therefore, circuit-level countermeasures are mandatory for mission-critical applications.

In the circuit level, several redundant circuits such as triple modular redundancy (TMR) [4] and the dual interlocked storage cell (DICE) [5] [6] have been proposed. However, the number of transistors of these FFs is much larger than that of a standard FF, and the performance overheads is large. Therefore, FFs with lower overhead and higher radiation hardness must be required. In an FDSOI process, the stacked structure is effective against soft errors [7]. Supply voltage dependence on the radiation tolerance of these FFs must be investigated for low-power application since Dynamic Voltage-Frequency Scaling (DVFS) is generally used to minimize power consumption of the circuit [8].

In this paper, the soft error tolerance of standard and stacked FFs (STDFF and STACKEDFF) in a 22 nm FDSOI process was evaluated by heavy-ion irradiation tests. These FFs were designed in the flip-well structure [9]. We examined whether the stacked structure is also an effective countermeasure against soft-errors in the flip-well structure. We also confirmed the dependence of soft error tolerance on supply voltage. This paper is organized as follows. Section II explains details of the device architecture and structure and performance of FFs we used. Section III explains the heavy-ion irradiation tests. Section IV explains and discusses experimental results. We conclude this paper in section V.

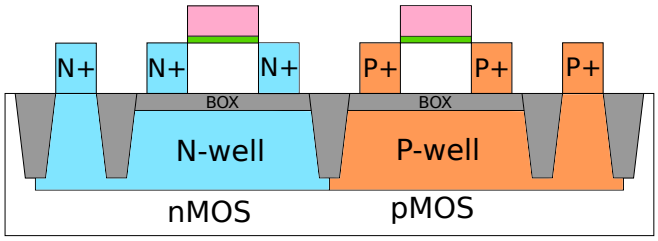

Fig. 1: Cross section of flip well structure.

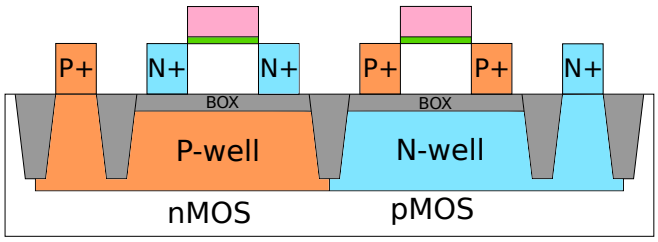

Fig. 2: Cross section of conventional structure.

II. Stacked structure in FDSOI process

The thin-BOX FDSOI process is used for aerospace and automotive applications [10]. The performance of FDSOI transistors can be changed by body bias through the thin BOX layer. Fig. 1 shows the cross section of thin BOX FDSOI devices. The flip-well structure is used in the 22 nm process instead of the conventional well structure in Fig.2 [11]. In the flip well structure, the N-well is placed under the NMOS

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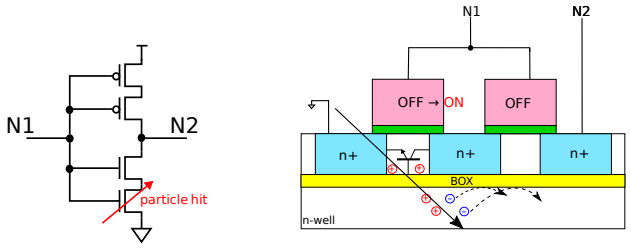


(a) Schematic of stacked structure (b) Cross section of stacked structure

Fig. 3: PBE suppression mechanism by stacked structure.

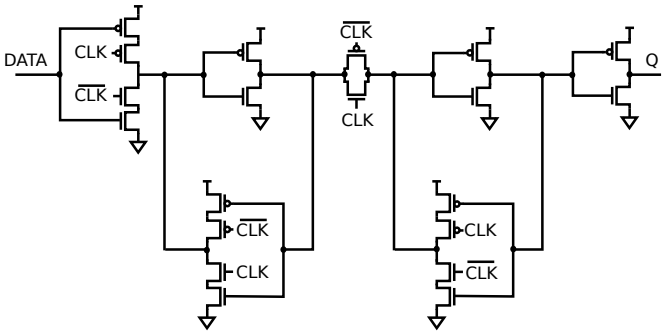


Fig. 4: standard FF (STDFF)

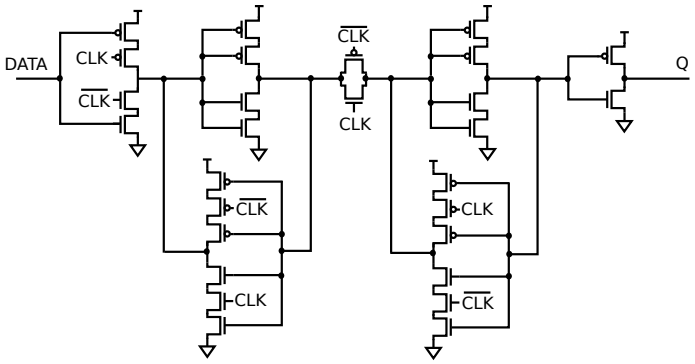
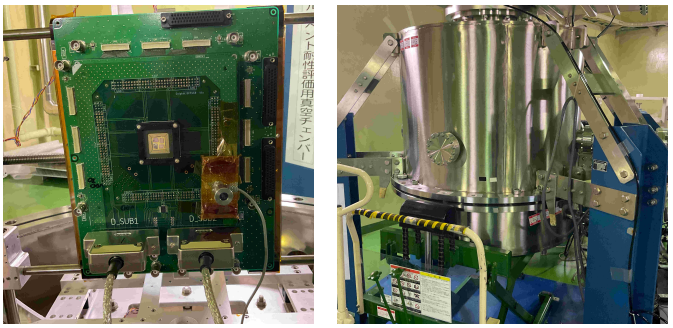


Fig. 5: STACKEDFF



(a) Test chip (b) Vacuum chamber

Fig. 6: Measurement setup. We use a vacuum chamber to prevent attenuation of the heavy ion beam by air.

transistor and the P-well is placed under the PMOS transistor. The flip well structure allows for higher drive strength and lower threshold voltage.

The stacked structure in FDSOI has higher soft error tolerance than in bulk [7]. The main cause of soft errors in FDSOI is the parasitic bipolar effects (PBE) [12]. The stacked structure can suppress PBE in FDSOI. Fig. 3 shows a stacked inverter composed of two series-connected nMOS and pMOS transistors. When a particle hits close to nMOS transistors, only one of the stacked transistors turns on. In this way, the stacked structure is very effective in FDSOI. However, errors occur when a particle passes through the two stacked MOSFETs. In the 65nm FDSOI process, a stacked latch has been reported to have significantly improved soft-error tolerance compared to a typical latch [13]. In this study, we investigated whether soft-error tolerance can be maintained in the stacked structure even with process scaling and the flip-well structure.

We designed two types of FFs, STDFF and STACKEDFF in the 22 nm thin BOX FDSOI process as shown in Figs. 4 and 5. These FFs have reset and scan input pins. In the tri-state inverter, the MOSFETs with CLK and $\overline{\text{CLK}}$ are placed between the stacked MOSFETs. It prevents a radiation particle from hitting at the two off-state transistors simultaneously. However, STACKEDFF has larger performance overheads than STDFF. Table I shows the simulation results of area, C-Q delay, setup/hold time and static/dynamic power of STDFF and STACKEDFF. The nominal supply voltage (V_{dd}) is 0.8 V. Power consumption is estimated at 10% data activity. As shown in Table I, the delay time and area overheads are very large.

III. Experimental Setup

The test chip was fabricated in the 22 nm FDSOI. All FFs are connected in series to form a shift register. Heavy-ion irradiation tests were conducted by Ar and Kr at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA). These heavy ions are often used to evaluate soft error tolerance [14] [15]. Table II shows linear energy transfer (LET) and energy of irradiated heavy ions. Fig. 7 shows the existence probability of heavy ions in outer space [16]. The number of particles with over 40 MeV-cm^2/mg is much less than that of particles with less than 40 MeV-cm^2/mg in outer space. Secondary ions by a neutron the hit to Si is mainly less than 18 MeV-cm^2/mg which is close to the LET of Ar [17]. This LET value is higher than secondary charged particles produced by a nuclear interaction between an Si atom and a high-energy neutron. Therefore, if no error occurs in Ar irradiation, it is assumed that no error occurs on the terrestrial region.

The irradiation tests were conducted as follows.

1) Initialize all series-connected FFs by 0 or 1.
2) Stabilize CLK to 0 or 1.
3) Expose heavy-ions to FFs for 30 seconds.
4) Read out stored data of FFs and count the number of upsets.

TABLE I: Simulation results of area, C-Q delay, Setup time, Hold time, Static power and Dynamic of the STDFF and STACKEDFF at V_{dd} = 0.8 V(standard voltage). These values are normalized to STDFF.

Circuit structure	Area	C-Q Delay	Setup time	Hold time	Static power	Dynamic power
STDFF	1.00	1.00	1.00	-1.00	1.00	1.00
STACKEDFF	1.89	2.78	2.77	12.5	1.00	1.07

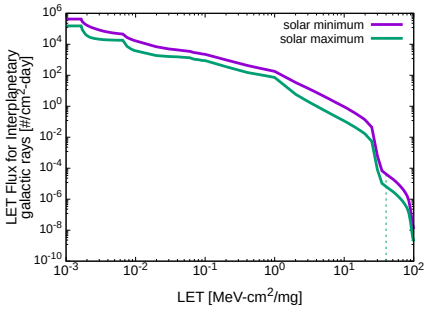


Fig. 7: LET distribution of heavy ions in outer space [16].

TABLE II: LET and energy of irradiated heavy ions.

	Ar	Kr
LET [MeV-cm^2/mg]	15.8	40.3
Energy [MeV]	137	289

Irradiation tests were done at the static conditions of (Q, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). V_{dd} was 0.8 V and 0.5 V at heavy-ion irradiation.

Cross Section (CS) is used in order to evaluate soft-error tolerance, which means an area of upsets when a particle passes a circuit block. The soft-error tolerance becomes stronger if CS becomes smaller. CS is calculated by Eq. (1) using the number errors (N_{error}), the number of FFs (N_{FF}), the effective heavy-ion fluence per cm^2 (N_{ion}), and the angle of heavy-ion to the chips (θ) [18]. In this measurement, heavy-ions were irradiated to the chip perpendicularly ($\theta = 0^\circ$).

$$CS\,[\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}} \cos\theta}. \quad (1)$$

IV. Experimental results and discussion

Figs. 8 and 9 show the CS by Ar and Kr irradiation when V_{dd} is set to 0.8 V and 0.5 V, respectively. In STACKEDFF, no error occurred at V_{dd} = 0.8 and 0.5 V under Ar irradiation as shown in Fig. 8 (a) and Fig. 9 (a). Under Kr irradiation, only one error was observed at (Q, CLK) = (0, 1) when V_{dd} = 0.8 V as shown in Fig. 8 (b). In (Q, CLK) = (0, 0), (1, 0), and (1, 1), no error occurred. In the (Q, CLK) = (0, 1) condition, the number of errors is almost zero and does not differ significantly from the other (Q, CLK) conditions. Therefore, when the supply voltage is nominal at 0.8 V, STACKEDFF is much stronger than STDFF in the flip-well structure. In [19], the soft error tolerance of FFs in the 22-nm FDSOI process using the conventional well structure are evaluated while the FDSOI process used in this study is the flip-well structure. Table III shows the differences in CSs of STDFF by the well structures. The results of conventional well are based on [19] and estimated from actual measurement results. Both structures show CSs around 10^{-10} $\mathrm{cm}^2/\mathrm{bit}$. Therefore, there is no significant difference in the CS of STDFF between the flip-well and conventional structures.

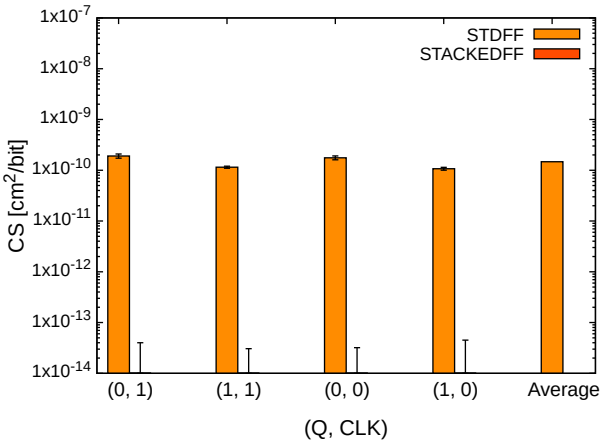
TABLE III: Differences in CSs of STDFF due to differences in well structure. Supply voltage is 0.8 V. The results of conventional well are based on [19] and estimated from actual measurement results.

	Ar (15.8 [MeV-cm^2/mg])	Kr (40.3 [MeV-cm^2/mg])
conventional well [19]	$1 \sim 2 \times 10^{-10}$	4.5×10^{-10}
flip well	1.47×10^{-10}	2.36×10^{-10}

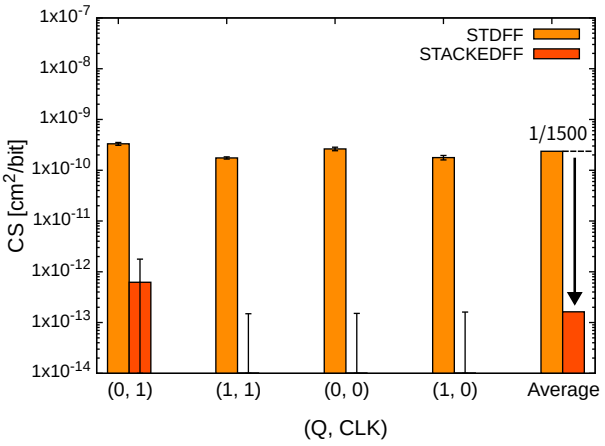
However, the CS at (Q, CLK) = (1, 0) increases significantly by lowering V_{dd} under Kr irradiation as shown in Fig. 9 (b). Fig. 10 shows the secondary latch (SL) of STACKEDFF. We consider these errors are generated by pMOS transistors. When (Q, CLK) = (1, 0), an error occurs in the two pMOS transistors indicated by the arrow. Since the four nMOS transistors are stacked, the amount of current flowing to the output node is small. Therefore, if an SET pulse is generated from pMOS transistors, it is unlikely to return to the correct value. These results indicated that errors are likely to occur in pMOS transistors in the flip-well structure. It has been reported that soft errors are more likely to occur in nMOS transistors than pMOS transistors in conventional structures [13]. However, in the flip-well structure, the performance of pMOS transistors is higher than the conventional well and soft errors are likely to occur in pMOS transistors as well. The overall soft error tolerance of STACKEDFF is only 39x higher than that of STDFF at V_{dd} = 0.5 V by Kr irradiation. Fig. 11 shows experimental CSs depending on V_{dd}. Each CS is the average of all four (Q, CLK) conditions. The CSs of STDFF was approximately constant regardless of the supply voltage. However, the CSs of STACKEDFF increased significantly as the supply voltage decreases. Therefore, the soft error tolerance of STACKEDFF become worse at lower voltage.

V. Conclusion

We evaluated soft-error tolerance of STDFF and STACKEDFF fabricated in 22 nm FDSOI using the flip-well structure by heavy-ion irradiation tests. Under Ar irradiation, no error occurred at all (Q, CLK) conditions even if supply voltage decreases. Under Kr irradiation, the CS of STACKEDFF is almost 0. Therefore, when the supply voltage is nominal at 0.8 V, the stacked structure is an effective countermeasure against soft errors even in

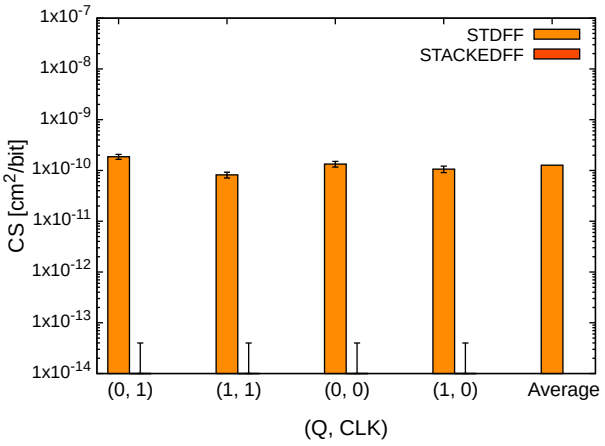


(a) Ar

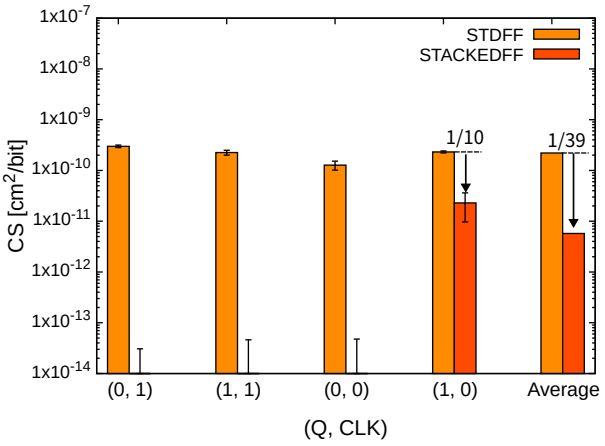


(b) Kr

Fig. 8: Results of the CS by Ar and Kr irradiation tests at V_{dd} = 0.8 V. Error bars are within 95% confidence.



(a) Ar



(b) Kr

Fig. 9: Results of the CS by Ar and Kr irradiation tests at V_{dd} = 0.5 V. Error bars are within 95% confidence.

the flip-well structure. We investigated soft-error tolerance of different well structures. CSs in STDFF of both well structures were around 10^{-10} $\mathrm{cm}^2/\mathrm{bit}$. Therefore, there is no significant difference in the CS of STDFF between the flip-well and conventional structures. While CSs of STDFF were almost constant, CS of STACKEDFF significantly increased as supply voltage decreases. This result shows that the pMOS transistors are vulnerable to soft errors when the supply voltage is low in the flip-well structure. This effect may become dominant as the substrate potential is changed under low supply voltage. Therefore, additional soft-error countermeasures are required for low-voltage operation.

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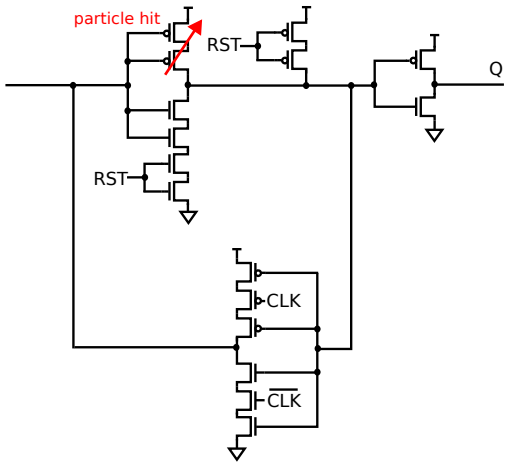

Fig. 10: SL of STACKEDFF. When (Q, CLK) = (1,0), an error occurs in the PMOS indicated by the arrow.

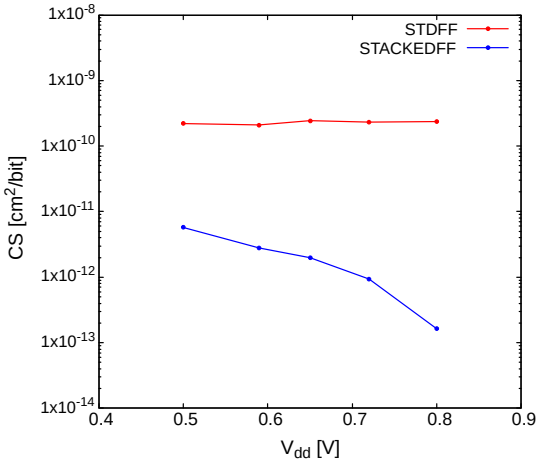

Fig. 11: Experimental CSs depending on V_{dd}. Each CS is the average of four (Q, CLK) conditions.

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