Radiation Hardened Flip-Flops Minimizing Area, Power, and Delay Overheads with 1/100 Lower α-SER in a 130 nm Bulk Process

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***Abstract*—We examined the radiation hardness of the several types of flip-flops fabricated in a 130 nm bulk process by alpha-ray irradiation tests and circuit simulation. The simulated α-SER of FFs with the critical charge larger than 14 fC becomes 1/100 of that with the critical charge of 10 fC. We propose a radiation-hardened flip-flop minimizing area, delay, and power overheads with 1/100 lower α-SER in a 130 nm bulk process. The radiation hardness is achieved by adding series transistors and wires with only less than 14% area, 7% delay, and 12% power overheads in order to increase the critical charge. Alpha-ray irradiation tests revealed that the proposed method can reduce soft error rates to 1/100.**

***Index Terms*—single event effects, soft error, alpha-ray, bulk process, radiation hard**

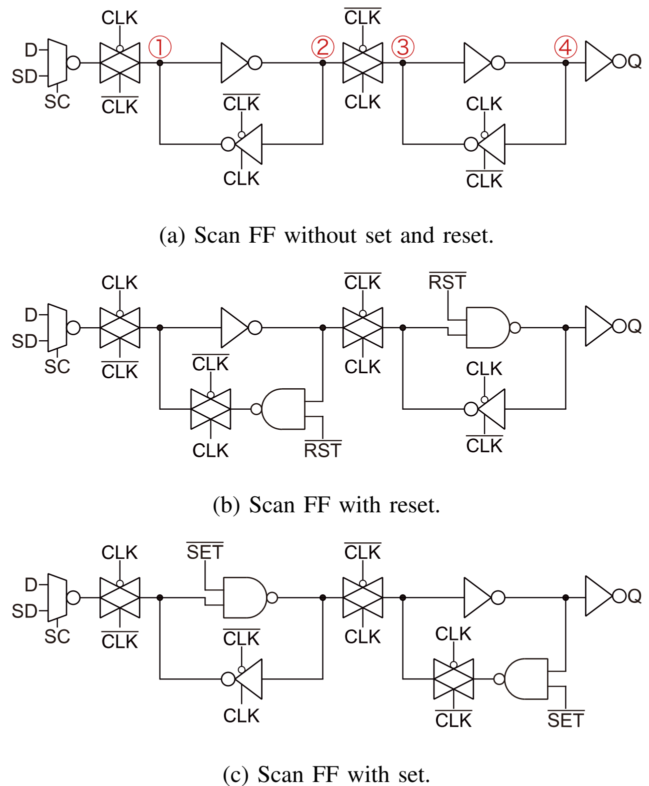
I. Introduction

Reliability issues are a key concern due to soft errors caused by process scaling [1]. Soft errors are temporary failures that flip stored values of storage elements such as flip-flops (FFs) and SRAMs by radiation particles. Soft errors are one of the important reliability issues. To improve the soft error tolerance of latches, several redundant circuits such as triple modular redundancy (TMR) [2] and the dual interlocked storage cell (DICE) [3][4] have been proposed. However, they have larger area, delay, and power than conventional circuits. A countermeasure is mandatory to improve soft errors with small overheads.

If an SULA (Super Ultra Low Alpha) package ($0.001\,\mathrm{cph/cm^2}$) is used, the α-soft error rate (SER) becomes 1/8 of the neutron-SER of an SRAM in a 65 nm process [5]. However, if a LA (Low Alpha) package ($0.02\,\mathrm{cph/cm^2}$) is used, the α-SER becomes 6x higher than the neutron-SER.

In this paper, we propose a radiation-hardened FF that can effectively reduce α-SER by increasing critical charge (Q_{crit}). An FF-array chip fabricated in a 130 nm bulk process was exposed to an alpha-ray source. The measurement results in this work reveal that the α-SER of the proposed FF is around 1/100 of conventional FFs. Therefore, a cheaper LA package is sufficient to decrease α-SER lower than neutron-SER.

This paper is organized as follows. Section II explains the FFs evaluated the soft error tolerance and their performance evaluation. Section III explains the proposed method to improve the soft error tolerance. Section IV explains the effectiveness of the proposed method by circuit simulation and alpha irradiation test. We conclude this paper in Section V.



(a) Scan FF without set and reset.

(b) Scan FF with reset.

(c) Scan FF with set.

Fig. 1: Conventional scan FFs.

II. Correlation between soft error tolerance and critical charge

In order to increase the radiation hardness of FFs, we investigate the correlation between Q_{crit} and soft error rates by circuit simulations. Q_{crit} represents the minimum amount of charge at which the stored value is flipped. Fig. 1 shows standard scan FFs without set and reset (a), with reset (b), and with set (c). Those three types FFs are implemented in three

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different standard-cell libraries, which are named "Library A, B, and C".

A. Alpha-ray Irradiation Test

The alpha-ray irradiation tests were performed using a $3\,\mathrm{MBq}$ $^{241}\mathrm{Am}$. The irradiation tests were conducted as follows.

(1) Initialize serially-connected FFs by all 0 or all 1.
(2) Stabilize CLK to 0 or 1.
(3) Expose alpha-ray to FFs for 5 minutes.
(4) Read out stored data of FFs.
(5) Count the number of upsets.
(6) Repeat (1) - (5) for four (Q, CLK) conditions.

Figure 2 shows the SER of the FFs with error bars of 95% confidence at $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$ (standard voltage). SEUs are more likely to occur under the conditions of (Q, CLK) = (0, 1) and (1, 0). Soft errors occur due to electrons in nMOS transistors and holes in pMOS transistors. Soft errors are more likely to occur on nMOS transistors than on pMOS transistors because the mobility of electrons is larger than that of holes [6]. Therefore, the SER in pMOS is small and is not considered in this paper. SEU occurs on the nMOS transistors of the tri-state inverter in the primary latch (PL) at (Q, CLK) = (0, 1) and in the secondary latch (SL) at (Q, CLK) = (1, 0). One of the reasons why SEU are more likely to occur in the tri-state inverters than in the inverters is the difference in the gate width of the pMOS transistors. If the gate width is narrower, the output is more likely to be flipped by alpha-induced charges because the current is reduced.

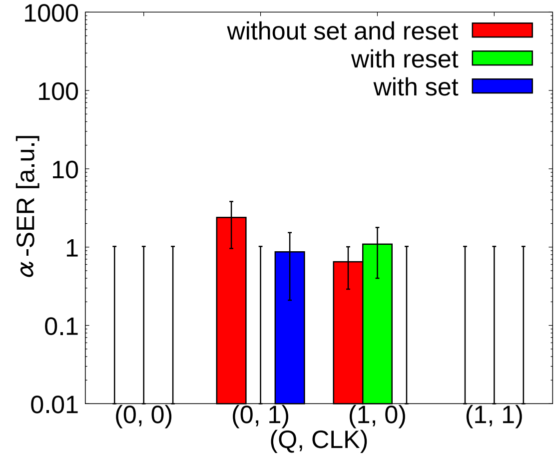
B. Circuit Simulations

Q_{crit} is calculated by circuit simulations. Fig. 3 shows the schematic to obtain Q_{crit} of the nMOS transistor. Table I shows the correspondence between the circuit nodes in Fig. 1 and the states of Q and CLK. The current source used for the simulation is the single exponential model in Eq. (1)[7].

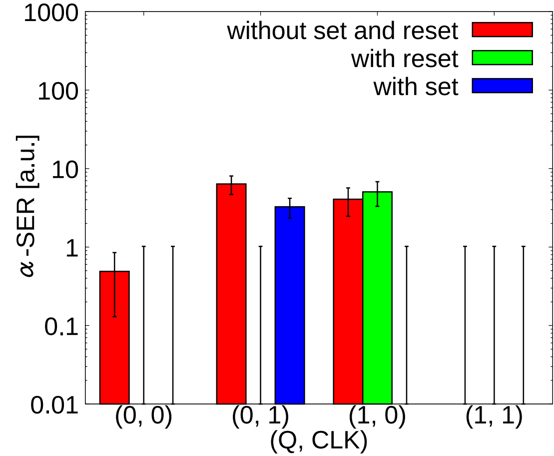
$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right). \tag{1}$$

T in Eq. (1) refers to the time constant that is determined by a process node. T is set to $40\,\mathrm{ps}$, corresponding to a $130\,\mathrm{nm}$ process[6].

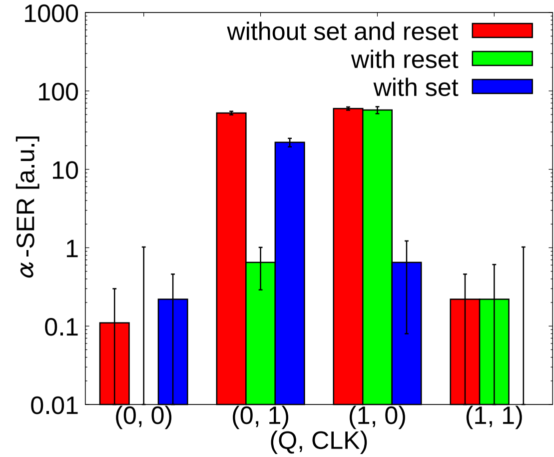
Table II and Fig. 4 show the Q_{crit} of all FFs and their comparison with the mesurement results. The Q_{crit} is smaller at node 1 and 3, where the conditions (Q, CLK) = (0, 1) and (1, 0) as shown in Table II. SER decreases as Q_{crit} increases as shown in Fig. 4. Therefore, Simulation and measurement results are correlated. According to Fig. 4, the α-SER of the FFs where the Q_{crit} is larger than 14 fC are less than 1/100 of the FF with the largest α-SER. It reveals that the soft error tolerance can be improved approximately 100x by setting the Q_{crit} of nMOS transistors more than 14 fC.



(a) Library A.



(b) Library B.



(c) Library C.

Fig. 2: The SEU rates calculated from alpha irradiation results.

III. Proposed Method to Improve Soft Error Tolerance

In this section, we explain the method to increase the Q_{crit} of nMOS transistors more than 14 fC for approximately 100x soft error tolerance.

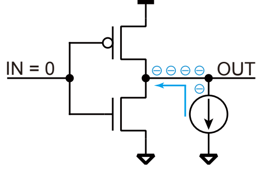


Fig. 3: Schematic to obtain Q_{crit} of nMOS transistor.

TABLE I: Correspondence between the measurement nodes and the input values.

Node number	Q	CLK
①	0	1
②	1	1
③	1	0
④	0	0

TABLE II: Q_{crit} of nMOS transistors in all FFs.

Library	FF Types	Q_{crit} [fC]			
		①	②	③	④
A	without set and reset	13	47	14	42
	with reset	23	40	14	42
	with set	13	49	23	43
B	without set and reset	12	24	12	20
	with reset	15	23	12	21
	with set	12	25	15	20
C	without set and reset	10	27	10	18
	with reset	13	27	10	16
	with set	10	27	12	18

A. Increased gate width of pMOS transistor

The gate width of the pMOS transistors depicted in blue that constitute the feedback gate is increased as shown in Fig. 5. By increasing the gate width, the number of holes that capture the electrons collected in the diffusion region can be increased. However, increasing the gate width increases the load capacitance on node 2 and 4, resulting in increased delay time. Therefore, the gate width of the pMOS transistors must be kept to as small as possible.

B. Changing the structure of the feedback gates

According to the measurement results, the set-scan FFs are highly tolerant under the condition (Q, CLK)=(1, 0),

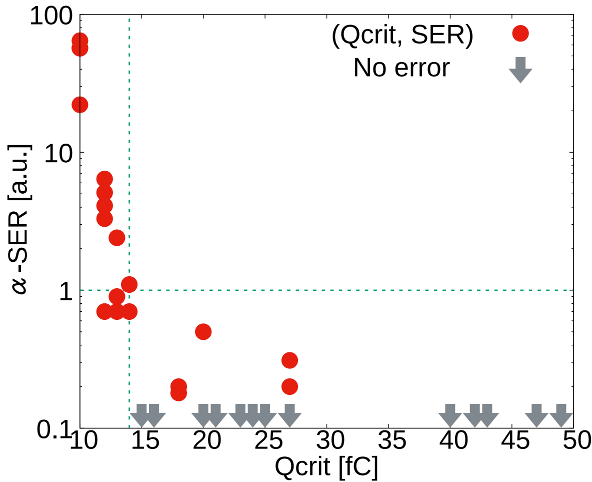


Fig. 4: Comparison between Q_{crit} and α-SER. The α-SER where Q_{crit} is larger than 14 fC are smaller than 1/100 of the largest rate. Down arrow means no error.

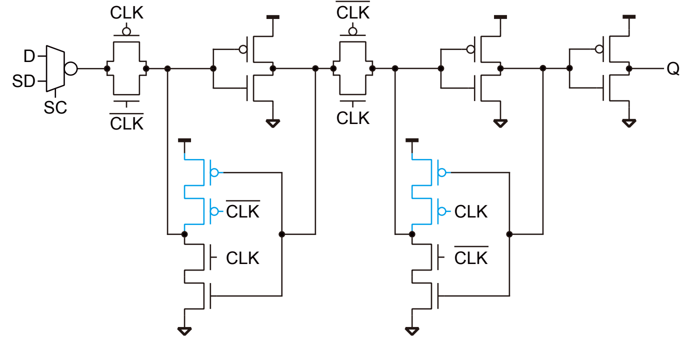


Fig. 5: Scan FF. The gate width of the blue pMOS transistors are increased.

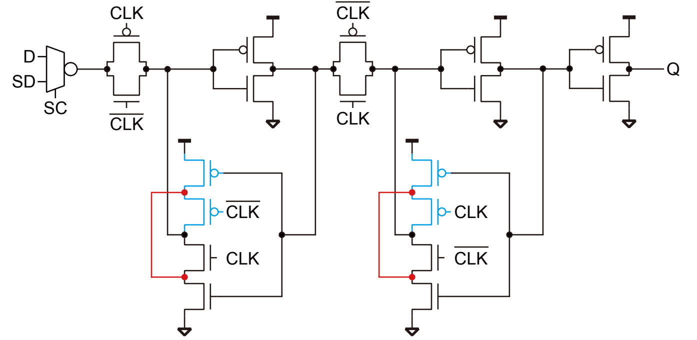
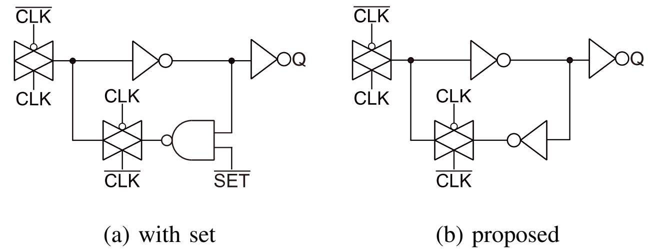


Fig. 6: Scan FF added wires.

regardless of the library. Therefore, the structure of the SL of the set-scan FF is used as a reference.

As shown in Fig. 6, the tri-state inverter is divided into an inverter and a transmission gate by adding wires between pMOS and nMOS connected in series. The transistors with clock signal inputs, which were connected in series before the modification, are now connected in parallel by the additional wires. The parallel connection lowers the overall resistance of the feedback gate and increases the amount of current flowing to the output, resulting in increase of Q_{crit}.

Fig. 7 shows the SLs of the modified FF and the set-scan FF. The NAND gate in Fig. 7(a) is replaced by the inverter in Fig. 7(b). The Q_{crit} of the inverter is 1 fC less than that of the



(a) with set (b) proposed

Fig. 7: Structure of SLs. The feedback gate shown in (a), which consists of NAND and transmission gates, has high soft-error tolerance. (b) is implemented an inverter instead of a NAND because the target FF is scan FF without set/reset.

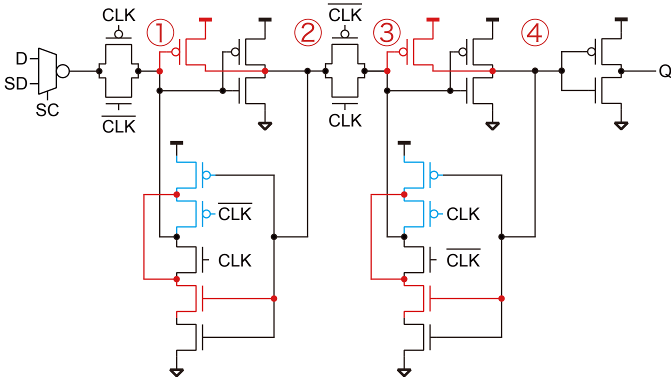
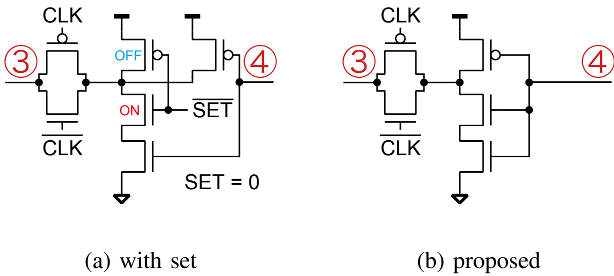


Fig. 8: Proposed circuit schematic. The gate width of the blue pMOS transistors are increased. The red pMOS transistors and wires are added.



(a) with set (b) proposed

Fig. 9: Structure of the feedback gates in the SLs. The pMOS transistors whose input is SET is in the OFF state, and (a) and (b) have the same operation.

NAND gate, however satisfies the target of 14 fC. Therefore the soft error tolerance is expected to be improved. However, the extra nMOS transistors and wires increase $Q_{\rm crit}$ at the feedback gate outputs (nodes 1 and 3) but decrease $Q_{\rm crit}$ at the feedback gate front (nodes 2 and 4).

C. Adding the transistors

In addition to the changes described in the previous section, transistors were added as shown in Fig. 8 . The gate width of the pMOS in the inverter for the PLs and SLs are not the minimum size, as same as the feedback gate pMOS. To increase the gate width, the height of the cell must be increased, but the library specifications do not allow for further expansion. Therefore pMOS are added in parallel. The addition of pMOS increases the number of holes that capture the electrons collected in the diffusion region, thus improving $Q_{\rm crit}$, which is reduced by the additional wires.

According to the measurement results, the set-scan FFs are highly tolerant under the condition (Q, CLK)=(1,0), regardless of the library. As shown in the Fig. 9, the tri-state inverter is divided into the inverter and the transmission gate and connected the nMOS transistors in series. By connecting the nMOS transistors in series with the feedback gate, the latch structure becomes equal to that of the SL of the set-scan flip-flop as shown in Fig. 9(a).

TABLE III: $Q_{\rm crit}$ of nMOS transistors in conventional or proposed FFs.

Circuit structure	Gate width of pMOS	$Q_{\rm crit}$ [fC] ①	②	③	④
Fig. 1(a)	1.00	10(±0)	27(±0)	10(±0)	18(±0)
Proposed	1.00	12(+2)	37(+10)	11(+1)	25(+7)
	1.50	14(+4)	36(+9)	13(+3)	25(+7)
	2.00	17(+7)	36(+9)	15(+5)	25(+7)

TABLE IV: Comparison of Area, Delay, and Power.

Circuit structure	Gate width of pMOS	Area	Delay	Power	ADP
Fig. 1(a)	1.00	1.00	1.00	1.00	1.00
Proposed	1.00	1.14	1.01	1.06	1.22
	1.50	1.14	1.04	1.09	1.29
	2.00	1.14	1.07	1.12	1.37

IV. Effectiveness of the Proposed Method

In this study, we applied the proposed method to scan FF without set/reset implemented in Library C, which is the most vulnerable. The $Q_{\rm crit}$ of the nMOS transistors in the conventional or proposed circuits are shown in Table III. The $Q_{\rm crit}$ are improved on all nodes. The comparison of area, delay, and power (ADP) is shown in Table IV. The proposed FFs have the area, delay, and power overheads by only less than 14%, 7%, and 12% respectively. The delay and the power of the proposed FF in Fig. 8 are increased proportionally by the gate width of the pMOS transistors.

Fig. 10 shows α-SER of the proposed FF at $V_{\rm DD}=1.5\,$V (standard voltage) measured by an accelerated test using a $3\,$MBq ^{241}Am. The test chips were fabricated in the 130 nm process. All FFs are implemented in shift registers. The test chip contains 15,400 bit of each FF. Note that all tests were performed in the static condition where the clock signal is fixed during alpha-ray irradiation. Fig. 10 shows that the soft error tolerance of the proposed FFs at (Q, CLK) = (0, 1) and

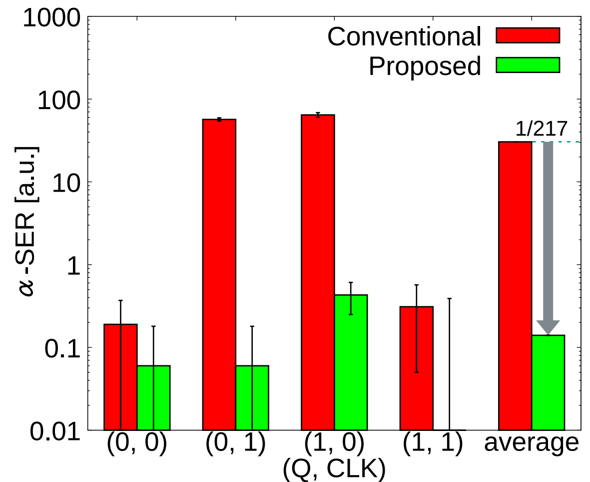


Fig. 10: α-SER. The conventional FF refers to Fig. 1 (a). The proposed FF refers to Fig. 8 with 2x gate width of pMOS transistors. The FFs are implemented in Library C.

(1, 0) are improved. In particular, in the proposed one with 2x gate width of the pMOS transistors, the α-SER at (Q, CLK) = (0, 1) and (1, 0) are reduced to approximately less than 1/100 compared to the conventional FF.

V. Conclusion

In this work, we clarify the vulnerability of FFs in a 130 nm process by accelerated test using an alpha-ray source and circuit simulations. From the measurement results and Q_{crit} calculated by circuit simulations, it was found that SER becomes less than 1/100 of the maximum value at locations where Q_{crit} is larger than 14 fC. We proposed the radiation-hard FF to improve the soft error tolerance with small overheads and confirmed that the proposed method can improve the soft error tolerance by accelerated testing to the proposed circuit using the $3\,\mathrm{MBq}$ alpha-ray source. The α-SER of the proposed FFs is 1/100 of the conventional FF. Thus a cheaper LA package is sufficient to reduce α-SER lower than neutron-SER.

VI. Acknowledgment

This study was conducted in collaboration with ROHM Co. Ltd and the TEG chip and PDK used in this study were provided by ROHM Co., Ltd. EDA tools used for simulations and layout design were provided by Synopsys Japan Ltd, Cadence Design Systems Japan Ltd, and Siemens EDA Japan Ltd through d.lab-VDEC of the University of Tokyo.

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