Total Ionizing Dose Effects by alpha irradiation on circuit performance and SEU tolerance in thin BOX FDSOI process

Takashi Yoshida, Kazutoshi Kobayashi, Jun Furuta
Kyoto Institute of Technology, Kyoto, Japan
Phone, Fax +81-75-724-7410, E-mail tyoshida@vlsi.es.kit.ac.jp

***Abstract*—Total ionizing dose (TID) effect is a phenomenon that threatens the reliability of transistors under high-radiation environments. TID is caused by radiation-induced trapped holes in oxide insulator. We evaluated the effects of TID on fully-depleted silicon on insulator (FDSOI) and bulk processes by measuring frequency of a ring oscillator (RO) and single event upset tolerance of flip flops (FFs). On the bulk process, TID induced Vth shift of nMOSFET, leads to increase of the RO frequency. On the FDSOI process, IR drop induced by large amount of leakage current flowing above buried oxide (BOX) layer decreases RO frequency. We also demonstrated that TID effects recovers by thermal annealing.**

***Index Terms*—TID, FDSOI, alpha-ray, leakage-current, annealing**

I. Introduction

Total Ionizing Dose (TID) effect is one of the major concerns for semiconductor devices in outer space, where high and low energy particles penetrate to space crafts. When a radiated particle hits a transistor, electron-hole pairs are generated by the ionization effect. The generated electrons rapidly diffuse out from the devices. However, some amount of holes are captured in pre-existing trap sites of SiO_2 insulator in gate oxide and shallow trench isolation (STI). These holes increase leakage current or prevent channel generation. It causes negative Vth shift in both of nMOSFET and pMOSFET as shown in Fig. 1 [1], [2]. Trapped holes in gate oxide can be ignored because its thickness has been reducing by scaling, and then, trapped holes in STI become dominant [3], [4].

Soft errors induced by the single event effect (SEE) threaten the reliability of semiconductor devices. A stored value in flip-flops (FFs) or SRAMs upsets by radiation effects, which is called single event upset (SEU). It is known that TID gives some amount of impact on SEU tolerance [3], [5].

In this paper, we measured TID effects on transistor performance degradation and SEU tolerance. This paper is organized as follows. Section Ⅱ explains details of experiments by alpha irradiation. Section Ⅲ explains and discusses results. We conclude this paper in section Ⅳ.

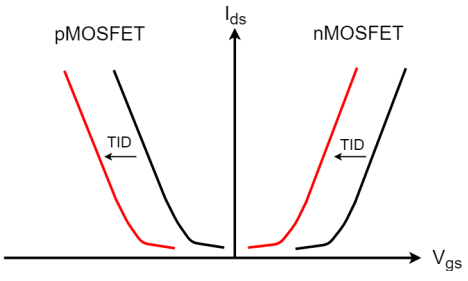


Fig. 1. Vth shift of nMOSFET and pMOSFET by TID.

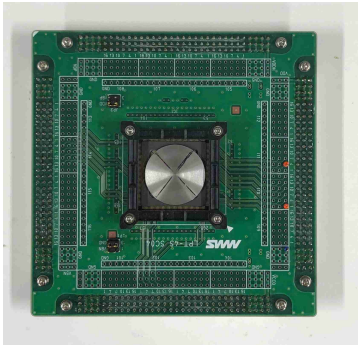


Fig. 2. Alpha-ray irradiation setup.

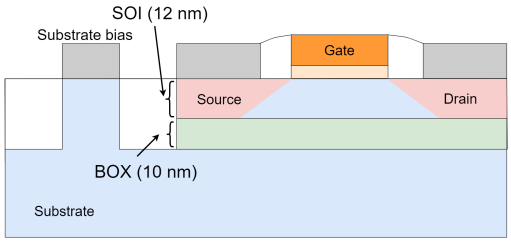


Fig. 3. Cross sectional view of thin BOX FDSOI.

II. Experimental Details

A. Alpha Irradiation

TID irradiation was carried out using alpha-ray from a ^{241}Am source (3.0 MBq) as shown in Fig. 2. The dose rate is 12.4 rad/s. It is calculated by Eq. (1) [6].

$$\begin{aligned} D &= F\,[\,\mathrm{cm}^{-2}\,] \times E_{\mathrm{LET}}\,[\,\mathrm{MeV}\cdot\mathrm{cm}^{2}\cdot\mathrm{mg}^{-1}\,] \\ &= 1.6\times10^{-1}\times F\times E_{\mathrm{LET}}\,[\,\mathrm{MGy}\,] \\ &= 1.6\times10^{1}\times F\times E_{\mathrm{LET}}\,[\,\mathrm{Mrad}\,] \end{aligned} \tag{1}$$

Where F is fluence of particles and E_{LET} is energy of a particle in LET (Linear Energy Transfer). The values of F and E_{LET} refer to [6] A test chip was fabricated in 65 nm bulk and 65 nm thin BOX FDSOI processes with 12 nm SOI and 10 nm BOX layers [7]. Note that those chips were fabricated from the same layout pattern except the BOX layer. Fig. 3 shows the cross section of an nMOSFET in the 65 nm thin BOX FDSOI process.

B. Measurement of Ring Oscillator Frequency

We compared ring oscillator (RO) frequency of the thin BOX FDSOI and bulk chips. The RO is composed of a CMOS NAND gate and 6 CMOS inverters (Fig. 4). Active and leakage

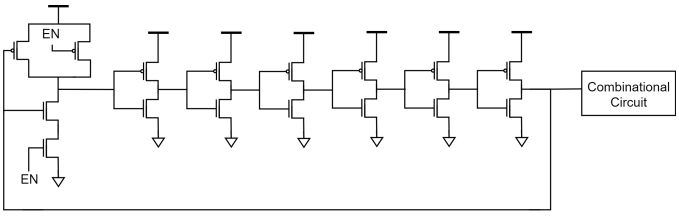


Fig. 4. Ring oscillator schematic.

current flowing through the whole LSI chip was also measured. The RO is attached at the first stage of combinational circuits that are operating by an oscillation signal from the RO.

C. Measurement of SEUs in FFs

We measured TID effects on SEUs in FFs by putting the same alpha source on a chip. All FFs are connected in series to form a shift register. The measurement procedure for SEUs is as follows.

1) Initialize serially-connected FFs by all 0
2) Stabilize clock signal to 0
3) Put the alpha source on a chip for 30 sec.
4) Read out stored data of FFs
5) Repeat 1) - 5) for 20 times

D. Thermal Annealing Behavior

It has been reported that the TID effect can be recovered by thermal annealing [8][9]. This is because thermal energy allows radiation-induced trapped holes in SiO_2 to be emitted. We verified the recovery phenomenon. The target is only the thin BOX FDSOI chip after irradiation since its leakage current was increasing after irradiation as shown later. First, the chip was left at room temperature. Then the chip was annealed at 100 °C and 125 °C.

III. Experimental Results and Discussion

A. Ring Oscillator Frequency

Fig. 5 shows the experimental results of RO frequency. Measured frequencies are normalized by pre-radiation frequency. RO frequency of the bulk chip increases by 1.1% at 1.9 Mrad, 1.5% at 3.6 Mrad respectively. On the other hand, RO frequency of the thin BOX FDSOI chip decreases by 14.6% at 1.9 Mrad. RO stopped oscillating after 1.9 Mrad irradiation.

Fig. 6 shows the current flowing through the whole LSI chip when the RO was oscillating. The current through the bulk chip was almost constant after irradiation, whereas the current through the thin BOX FDSOI chip increased by over 10x at 1.9 Mrad.

TID causes negative Vth shift both of n- and p- MOSFETs. Negative Vth of nMOSFET leads to increase of RO frequency. while those of pMOSFET leads to decrease of RO frequency.

The trapped holes induced by irradiation attract electrons. These electrons form an inversion layer that increase leakage current on nMOSFET. Electrons prevent p-channel formulation on pMOSFET along both sides of the channel. However, current can flow in the middle of the channel. Therefore,

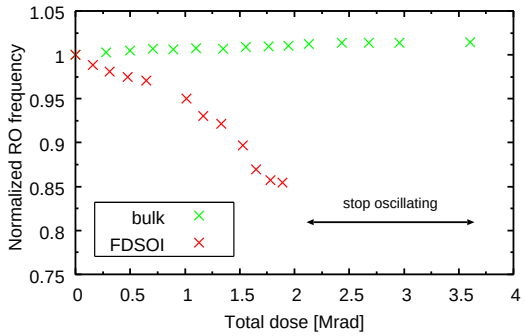


Fig. 5. Measurement results of RO frequency.

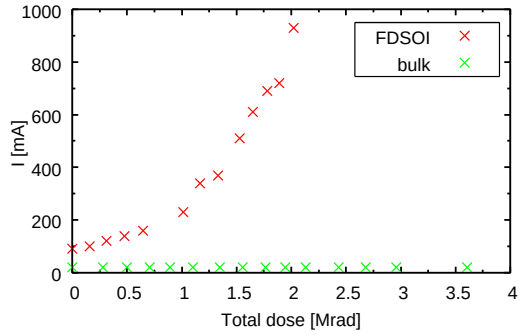


Fig. 6. Measurement results of leakage current through the LSI chip.

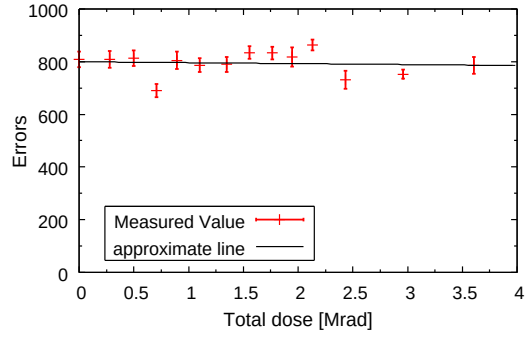
effects of the negative Vth shift of pMOSFET is negligible compared with nMOSFET. This increases RO frequency on the bulk chip.

In contrast, RO frequency decreases on the thin BOX FDSOI chip. Moreover, the current through the thin BOX FDSOI chip increased by over 10x while the current through the bulk chip was almost constant after irradiation. The trapped holes in the BOX attract electrons and they form another inversion layer that increase leakage current drastically. The large leakage current causes IR drop. It decreases supply voltage on the RO, therefore its oscillation speed becomes slow. SPICE simulations show that 0.12 V decrease of the supply voltage decreases the oscillatory frequency by 15%.

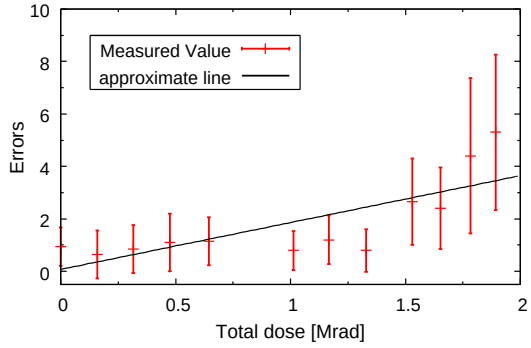
B. Measurement of SEUs in FFs

Fig. 7 shows that the experimental results of SEU tolerance of the bulk and thin BOX FDSOI chips. On the bulk chip, the number of SEUs was almost constant after TID irradiation. The number of SEUs of the the FDSOI chip is 1/800 of the bulk chip before TID irradiation. This is because the BOX layer prevents charge from being collected from substrate [10]. However, the number of SEUs increases by over 5x after TID irradiaton.

This increase of the number of SEUs can also be explained by the IR drop due to the increase of leakage current. TID increases leakage current, and decreases supply voltage of FFs. The amount of charge to invert a stored value is proportional to supply voltage [11]. Thus the IR drop promotes SEUs.

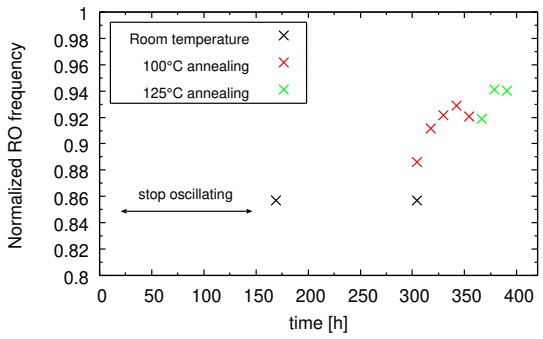


(a) bulk

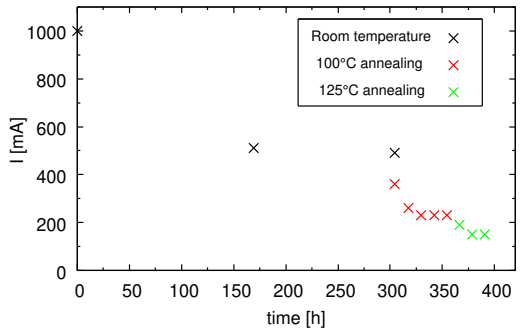


(b) FDSOI

Fig. 7. Measurement results of the number of SEUs.



(a) RO frequency



(b) Leakage current through the FDSOI chip

Fig. 8. Annealing effects.

C. Thermal Annealing Behavior

Fig. 8 shows recovery of RO frequency and current flowing through the whole chip after thermal annealing. After irradiation, the RO in the FDSOI chip stopped oscillation, but it started to oscillate by leaving it at room temperature for 169 hours. 100 °C annealing recovered the oscillation frequency of RO to 92.1% of the the initial frequency before irradiation and 125 °C annealing recovered the frequency to 94.0%. It is found that the recovery depends on the ambient temperature.

IV. Conclusion

We evaluated the TID effects on the thin BOX FDSOI and bulk processes through the measurement of the RO frequency and SEUs by alpha-ray irradiation. RO frequency of the bulk chip increases by 1.5% at 3.6 Mrad, while that of the thin BOX FDSOI decreases by 14.6% at 1.9 Mrad. The trapped holes in the BOX layer by irradiation promotes the leakage current and IR drop. As a result, the RO frequency decreases by supply voltage drop on the FDSOI chip. In the bulk chip, however, leakage current was almost constant after irradiation and the RO frequency increases due to the negative V_{th} shift on nMOSFET.

SEU tolerance of the thin BOX FDSOI chip is much higher than the bulk chip. However, it is degraded by TID. It is also due to the IR drop by leakage current. It is confirmed that thermal annealing recovers TID effects. The recovery rate depends on the ambient temperature.

References

[1] H. J. Barnaby. Total-ionizing-dose effects in modern cmos technologies. IEEE Transactions on Nuclear Science, 53(6):3103–3121, Dec 2006.

[2] M. Gaillardin, M. Martinez, P. Paillet, M. Raine, F. Andrieu, O. Faynot, and O. Thomas. Total ionizing dose effects mitigation strategy for nanoscaled fdsoi technologies. IEEE Transactions on Nuclear Science, 61(6):3023–3029, Dec 2014.

[3] R. M. Chen, Z. J. Diggins, N. N. Mahatme, L. Wang, E. X. Zhang, Y. P. Chen, Y. N. Liu, B. Narasimham, A. F. Witulski, B. L. Bhuva, and D. M. Fleetwood. Effects of total-ionizing-dose irradiation on seu- and set-induced soft errors in bulk 40-nm sequential circuits. IEEE Transactions on Nuclear Science, 64(1):471–476, Jan 2017.

[4] F. Faccio and G. Cervelli. Radiation-induced edge effects in deep submicron cmos transistors. IEEE Transactions on Nuclear Science, 52(6):2413–2420, Dec 2005.

[5] H. Zhang, H. Jiang, X. Fan, J. S. Kauppila, I. Chatterjee, B. L. Bhuva, and L. W. Massengill. Effects of total-ionizing-dose irradiation on single-event response for flip-flop designs at a 14-/16-nm bulk finfet technology node. IEEE Transactions on Nuclear Science, 65(8):1928–1934, Aug 2018.

[6] A. Haran, M. Murat, and J. Barak. Charge yield and track structure effects on total ionizing dose measurements. IEEE Transactions on Nuclear Science, 55(4):2098–2105, Aug 2008.

[7] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura. Local Vth variability and scalability in silicon-on-thin-box (SOTB) CMOS with small random-dopant fluctuation. IEEE Transactions on Electron Devices, 57(4):835–845, Apr. 2010.

[8] J. Park, D. Moon, H. Bae, Y. T. Roh, M. Seol, B. Lee, C. Jeon, H. C. Lee, and Y. Choi. Local electro-thermal annealing for repair of total ionizing dose-induced damage in gate-all-around mosfets. IEEE Electron Device Letters, 37(7):843–846, July 2016.

[9] S. Dhombres, A. Michez, J. Boch, F. Saigne, S. Beauvivre, D. Kraehenbuehl, J.Vaille, P.C.Adell, E.Lorfevre, R.Ecoffet, and F.Roig. Study of a thermal annealing approach for very high total dose environments. IEEE Transactions on Nuclear Science, 61(6):2923–2929, Dec 2014.

[10] P. Roche, J. L. Autran, G. Gasiot, and D. Munteanu. Technology downscaling worsening radiation effects in bulk: SOI to the rescue. In IEEE International Electron Devices Meeting, pages 31.1.1–31.1.4, Dec. 2013.

[11] S. Hirokawa, R. Harada, M. Hashimoto, and T. Onoye. Characterizing alpha- and neutron-induced seu and mcu on sotb and bulk 0.4-v srams. IEEE Transactions on Nuclear Science, 62(2):420–427, April 2015.