Comparison of Radiation Hardness of Stacked Transmission-Gate Flip Flop and Stacked Tristate-Inverter Flip Flop in a 65 nm Thin BOX FDSOI Process

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***Abstract*—We examined radiation hardness of a stacked transmission-gate flip flop and a stacked tristate-inverter flip flop, which are called STACKEDTGFF and STACKEDTIFF respectively. Stacked flip flops fabricated in FDSOI are stronger against soft errors than in bulk because all transistor channels are isolated by a BOX layer. We evaluated soft-error tolerance by neutron and heavy-ion irradiation. STACKEDTIFF is faster than STACKEDTGFF because of the difference of the number of gates along the data path. Those FFs did not flip by neutrons and the normal incidence of heavy ions with LET of less than 40 MeV-cm^2/mg. They are stronger against soft errors than a standard TGFF by two order of magnitude. We also investigated incident angle dependence of those FFs by heavy ions.**

***Index Terms*—single event effect, soft error, heavy ion, FDSOI, stacked flip flop, radiation hard.**

I. Introduction

Reliability issues have become a significant concern due to soft errors with technology downscaling [1]. Soft errors are one of temporal failures that flip stored values in storage elements such as flip flops (FFs) or SRAMs by radiated particles. A flipped storage cell can be recovered by rebooting or rewriting. However, it is a serious issue especially for critical devices dealing with human life or social infrastructures. To improve the tolerance of FFs against soft errors, several redundant FFs such as triple modular redundancy (TMR) [2] and dual interlocked storage cell (DICE) [3][4] have been proposed for effective countermeasures. However, they have longer delay time, larger area and power consumption than conventional standard FFs. Fully-depleted silicon on insulator (FDSOI) processes have 50-100x higher soft-error tolerance than conventional bulk processes without any performance overhead. It is because the buried oxide (BOX) layer prevents charge from being collected from substrate [5].

In this paper, we compared two types of FFs with stacked structure by neutron and heavy-ion irradiation.

Section Ⅱ explains related works. We explain about flip flops evaluated soft-error tolerance in the 65 nm FDSOI process in section Ⅲ. Section Ⅳ explains experimental setups at the research center for nuclear physics (RCNP) and at Takasaki Ion accelerators for Advanced Radiation Application (TIARA), Japan. Section Ⅴ explains experimental results by neutron and heavy-ion irradiation. We conclude this paper in Section Ⅵ.

II. Related Work

Prior to explaining our works, a related work is introduced to figure out our motivations. Reference [6] evaluates soft-error tolerance of a 6T SRAM and a DICE latch (Fig. 1). The 6T SRAM has no tolerance against soft errors. The SRAM test chip was fabricated in a 65 nm bulk process and irradiated by heavy ions at different supply voltages. Table I shows linear energy transfer (LET), energy, range and flux of heavy ions. LET is the amount of energy that an ionizing particle transfers to the material traversed per unit distance. Figure 2 shows the existence probability of heavy ions in outer space [7].

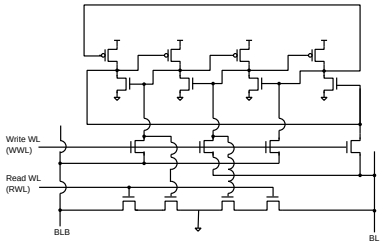


Fig. 1. DICE latch

TABLE I
LET, ENERGY, RANGE AND FLUX OF HEAVY IONS.

Ion	LET [MeV-cm^2/mg]	Energy [MeV]	Range [um]	Flux [n/cm^2/s]
Li	0.44	45	259.6	1.0×10^6
C	1.73	80	127	4.3×10^5
F	4.2	110	82.7	3.4×10^4
Si	9.1	140	53	2.9×10^5
Ti	22	165	33.9	5.2×10^5

Cross-Section (CS) is used in order to evaluate soft-error tolerance, which is an area of upsets when a particle passes a circuit block. The soft-error tolerance become stronger if CS becomes smaller. Equation (1) is used in order to calculate CS [8].

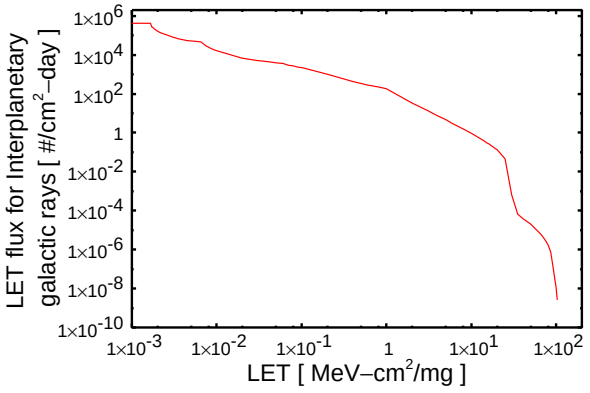


Fig. 2. LET distribution of heavy ions in outer space [7]

TABLE II
CSs ON 6T AND DICE BY LI, C, F, SI AND TI IRRADIATION.

LET [MeV-cm^2/mg]	6T	DICE
0.44	3.61×10^{-10}	0
1.73	2.64×10^{-9}	0
4.2	4.77×10^{-9}	0
9.1	7.66×10^{-9}	4.88×10^{-10}
22	1.00×10^{-8}	2.24×10^{-9}

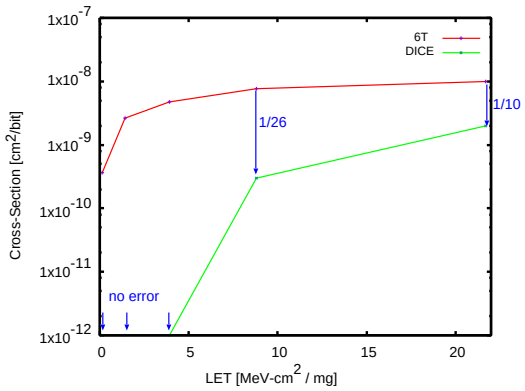


Fig. 3. CSs by Li, C, F, Si and Ti irradiation [6].

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \cos\theta\ N_{\mathrm{FF}}} \quad (1)$$

N_{error} is the number of errors, $N_{\mathrm{ion}} \cos\theta$ is the effective heavy-ion fluence at θ (cm^2), and N_{FF} is the number of FFs (bit).

Table II and Fig. 3 show CSs at Vdd = 0.8 V by Li, C, F, Si and Ti irradiation. There was no error on the DICE latch by heavy ions with LET less than 4.2 MeV-cm^2/mg. The DICE latch is 5X stronger against soft errors than the 6T SRAM by heavy ion with LET of 22 MeV-cm^2/mg.

III. Flip Flops evaluated soft-error tolerance in FDSOI

The parasitic bipolar effect (PBE) significantly promotes soft errors on SOI devices [5]. PBE is a phenomenon in which generated holes in body region rise the potential of the body layer. Then, a parasitic bipolar transistor composed of the drain, body and source terminals turns on. Figure 4 shows a standard FF called the transmission gate FF (TGFF). There can be two structures to contrast a stacked FF called STACKEDTGFF and STACKEDTIFF. A stacked inverter is proposed for SOI to prevent soft errors, which is composed of series-connected NMOS and PMOS transistors in Fig. 5 [9][10]. The series-connected NMOS and PMOS transistors are rarely flipped by PBE at the same time because they are fully separated by the shallow trench isolation (STI) and the BOX layer. However, the delay time of the stacked TGFF is longer than a standard FF since gate capacitance and output impedance of the stacked inverter are 2x larger than those of the inverter.

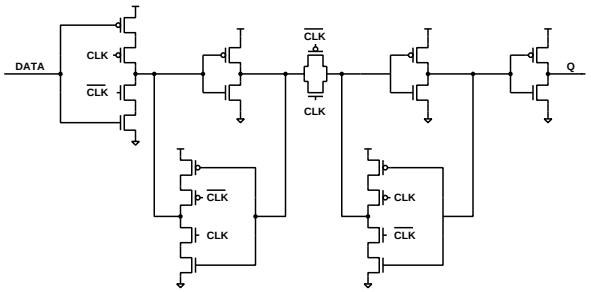


Fig. 4. Standard TGFF.

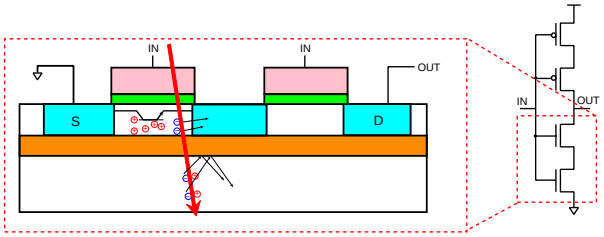


Fig. 5. Cross section and schematic of NMOS transistors in a stacked inverter.

STACKEDTGFF
: Figure 6 shows STACKEDTGFF consisting of stacked transistors. STACKEDTGFF has stacked inverters and tristate inverters in the master and slave latches to reduce SEU rates in the 65 nm thin BOX FDSOI process.

STACKEDTIFF
: Figure 7 shows STACKEDTIFF, in which the transmission gate in STACKEDTGFF is replaced by the tristate inverter. The output inverter (Mout) is connected to the tristate inverter between the master and slave latches.

We measured area, D-Q delay time, power consumption and energy area (EA) product of those FFs using circuit simulations at supply voltage ($\mathrm{V_{dd}}$) of 1.2 V. D-Q delay is the time taken from input to output in a FF. EA product is generally used as an index of performance (EA = D-Q delay time $\times$ power consumption $\times$ area). Table III and Fig. 8 show the simulation results of area, D-Q delay time, power consumption at 10% data activity and EA product of each FF. All values are normalized to those of TGFF. The values in parentheses are normalized to those of STACKEDTGFF. The performance of STACKEDTGFF is worse than that of TGFF. Especially, the D-Q delay time of STACKEDTGFF is 1.76x longer than that of the standard TGFF because the stacked inverters in master and slave latches prolong its delay time. The area and power consumption of STACKEDTIFF are 9% and 1% larger than that of STACKEDTGFF, while the delay time and EA product of STACKEDTIFF are 21% and 13% smaller than that of STACKEDTGFF. It is because the data path in STACKEDTIFF does not include Mslave in the slave latch. Figure 9 compares the data paths of STACKEDTIFF and STACKEDTGFF.

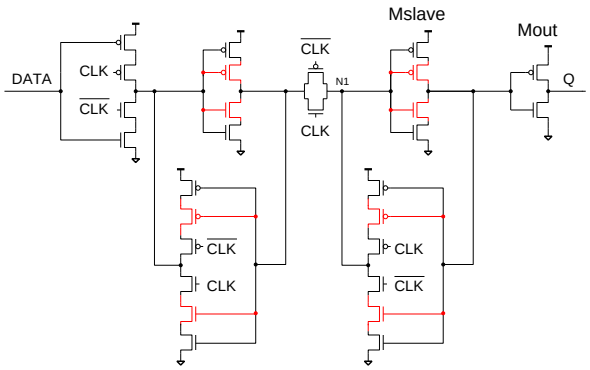


Fig. 6. STACKEDTGFF.

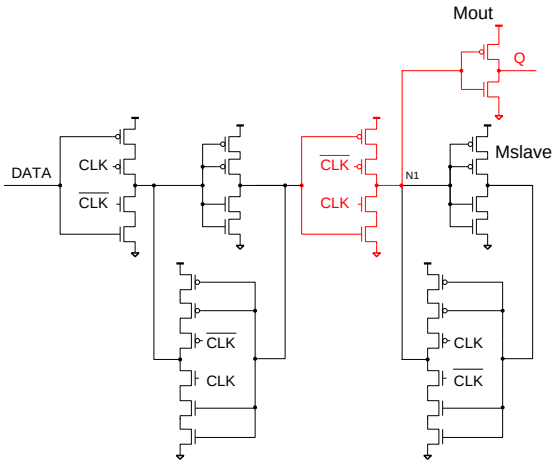


Fig. 7. STACKEDTIFF.

TABLE III
SIMULATION RESULTS OF AREA, D-Q DELAY, POWER CONSUMPTION, EA PRODUCT OF EACH FF. ALL VALUES ARE NORMALIZED TO THOSE OF STANDARD TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKEDTGFF.

FF	STACKEDTGFF	STACKEDTIFF
Area	1.24 (1)	1.35 (1.09)
D-Q Delay of FF	1.76 (1)	1.39 (0.79)
Power Consumption	1.05 (1)	1.06 (1.01)
EA product	2.99 (1)	1.99 (0.87)

IV. Experimental Setup

A test chip was fabricated in a 65 nm thin BOX FDSOI process in order to evaluate soft-error tolerance [11]. Figure 10 shows the cross section of an NMOS transistor in the 65 nm thin-BOX FDSOI process [11]. Figure 11 shows the chip micrograph that contains 22,680 bit TGFFs, 22,950 bit STACKEDTGFFs, and 22,680 bit STACKEDTIFFs. All FFs are connected in series to form a shift register. We evaluated soft-error tolerance by neutron and heavy-ion irradiation.

Spallation neutron tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [12]. Figure 12 shows the experimental setup of neutron irradiation tests. Figure 13 shows the normalized neutron beam spectrum in comparison with the terrestrial neutron spectrum at the sea

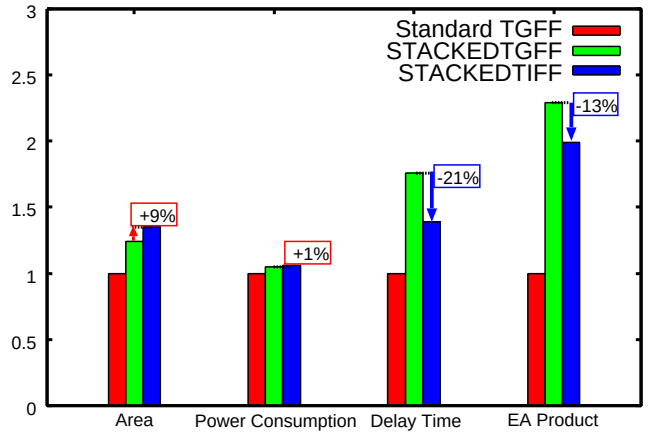


Fig. 8. Simulation Results of area, D-Q delay, power consumption, EA product of each FF. All values are normalized to those of standard TGFF.

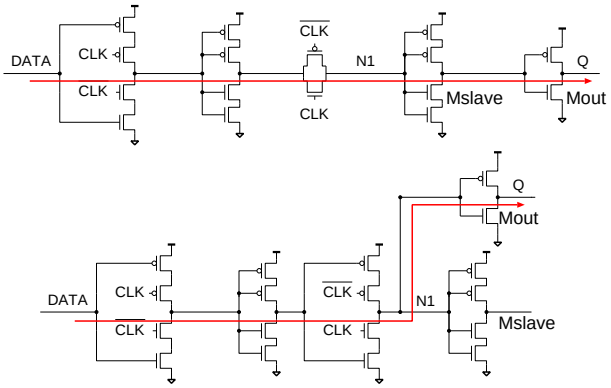


Fig. 9. Data path of STACKEDTGFF and STACKEDTIFF.

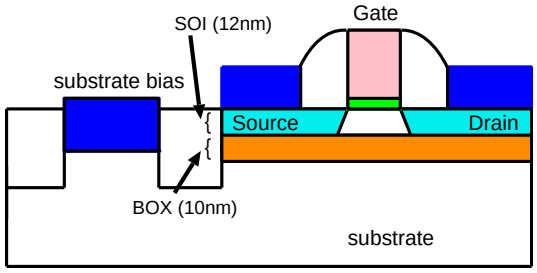


Fig. 10. Cross sectional view of Thin BOX FDSOI

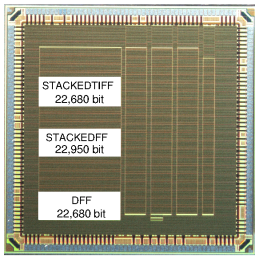


Fig. 11. Chip micrograph that contains 22,680 bit standard TGFFs, 22,950 bit STACKEDTGFFs, and 22,680 bit STACKEDTIFFs.

level in New York City (NYC). The average acceleration factor

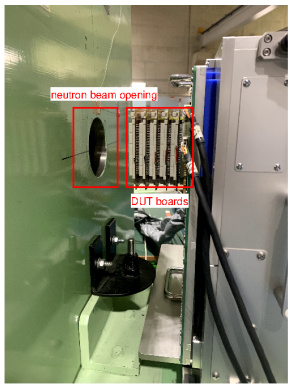


Fig. 12. Neutron irradiation setup

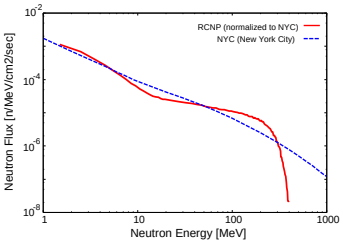


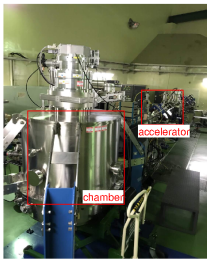
Fig. 13. Normalized energy spectrum of spallation neutron beam at RCNP and neutron at the sea level of NYC.

(AF) is 3.77×10^8 compared with the sea level in NYC. In order to increase the number of upset FFs within a limited time, five stacked DUT boards each of which includes two test chips were exposed to the neutron beam. As a result, 10 chips were measured simultaneously. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). The $V_{\rm dd}$ was 0.6 V at neutron irradiation and stored values were shifted every 300 sec. to count the number of upset FFs. Soft-error rates (SERs) are calculated using Eq. (2).

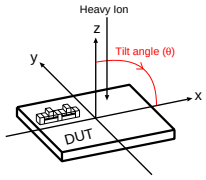
$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\rm error} \times 10^9\ \mathrm{h} \times 1024^2\ \mathrm{bit}}{300\ \mathrm{sec}/3600\ \mathrm{sec} \times AF \times N_{\rm FF}} \quad (2)$$

Failure in time (FIT) is the number of failures in 10^9 hours.

Heavy-ion irradiation tests were conducted by Ar, Kr and Xe at Takasaki Ion accelerators for Advanced Radiation Application (TIARA), Japan in order to investigate tolerance to soft errors in outer space and the terrestrial region. Figure 14(a) shows the experimental setup of the heavy-ion irradiation tests. Device under tests (DUTs) are sealed in the chamber in order to keep ion energy. Table IV shows LET, energy and average flux of heavy ions. Secondary ions by a neutron hit to Si is mainly less than 18 MeV-cm^2/mg which is close to LET of Ar [13]. In outer space, most of heavy ions have LET less than 60 MeV-cm^2/mg. Thus, we chose Ar for terrestrial regions and Xe for outer space. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). The $V_{\rm dd}$ was 0.8 V at heavy-ion irradiation. Each irradiation time was 30 sec. and irradiation was repeated for 5 times per



(a) Heavy-ion irradiation setup.



(b) Tilt angles of chip.

Fig. 14. Measurement setup.

TABLE IV
LET, ENERGY AND FLUENCE OF HEAVY IONS.

Ion	LET [MeV-cm^2/mg]	Energy [MeV]	Flux [n/cm^2/s]
Ar	17.5	107	3.59×10^6
Kr	40.9	230	3.16×10^6
Xe	67.2	350	1.82×10^6

condition.

The irradiation procedure was as follows.

1) Initialize serially-connected FFs by all 0 or all 1
2) Stabilize CLK to 0 or 1
3) Expose neutrons or heavy ions (Neutron beam keep on being exposed during measurement).
4) Read out stored data of FFs
5) Count the number of upsets
6) Repeat 1) - 5) for four (DATA, CLK) conditions

The test chip was irradiated from the normal angle (θ = 0°) under the four DATA and CLK states. In addition, we examined CSs depending on incident angles at $V_{\rm dd}$ = 0.8 V when (DATA, CLK) = (0, 1). We chose this condition because the number of errors at the condition is the largest of all conditions by measurement results. Experiments were carried out at 60° tilt angle by Ar irradiation and at 30° and 60° tilt angles by Kr and Xe irradiation. The tilt angle (θ) of the chip is defined as shown in Fig. 14(b).

V. Measurement Results

A. Neutron Results

Figure 15 shows SERs by neutrons irradiation with error bars of 95% (2σ) confidence. There was no error on STACKEDTGFF and STACKEDTIFF at all static conditions. It revealed that the stacked structure had sufficient soft-error tolerance in the terrestrial region.

B. Heavy-ion Results

Figure 16 shows the experimental result of the average CSs by Ar, Kr and Xe with error bars of 95% confidence. The experimental result of STACKEDTGFF by Xe irradiation is quoted from [14]. At the normal incident of Ar and Kr, there was no error on STACKEDTGFF and STACKEDTIFF. CS on the DICE latch is 2.24×10^{-9}cm^2/bit by heavy ion

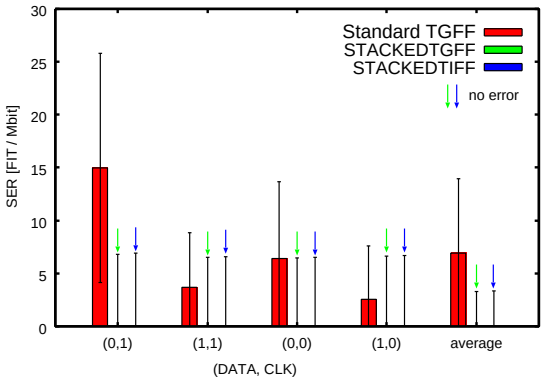


Fig. 15. SERs by neutrons irradiation with error bars of 95% (2σ) confidence.

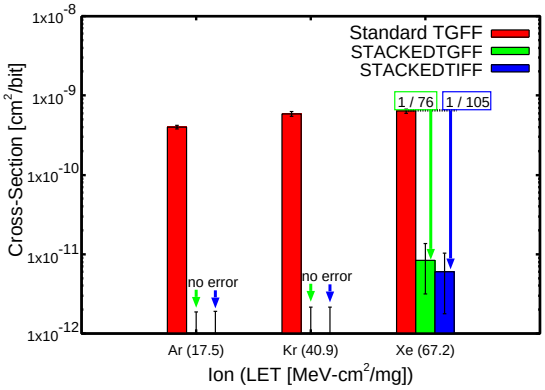


Fig. 16. Average CSs by Ar, Kr and Xe irradiation.

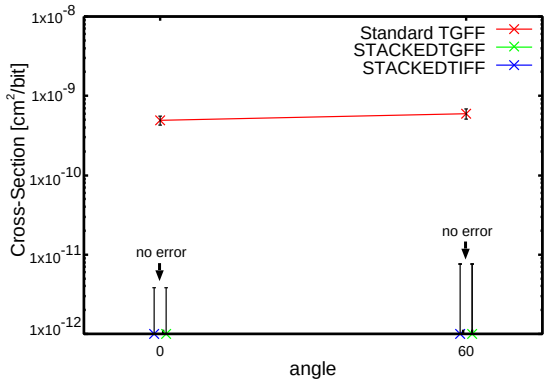
with LET = 22 MeV-cm^2/mg [6]. Therefore, STACKEDTGFF and STACKEDTIFF in the 65 nm thin BOX FDSOI process have higher soft-error tolerance than the DICE latch in the 65 nm bulk process. The average CSs of STACKEDTGFF and STACKEDTIFF are 1/76 and 1/105 of TGFF by Xe.

Figures 17 (a) - 17 (c) show the experimental CSs depending on the tilt angles by Ar, Kr and Xe with error bars of 95% confidence. There was no error on STACKEDTGFF and STACKEDTIFF at the tilt angle of 60° by Ar irradiation. The stacked structure has enough soft-error tolerance in the terrestrial region because Ar produced no soft error by neutrons and Ar ion. CSs of STACKEDTGFF at the tilt angle of 60° by Kr and Xe are 1/61 and 1/10 of TGFF, while CSs of STACKEDTIFF at the tilt angle of 60° by Kr and Xe are 1/120 and 1/18 of TGFF.

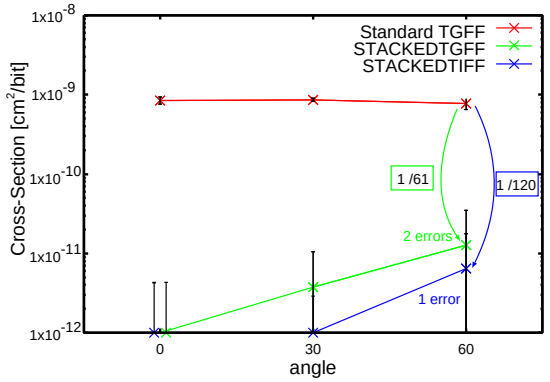
All the FFs become weaker against soft errors as the incident angle is higher, which can be explained by Fig. 18. The reason of the weakness is that a heavy ion passes the series-connected NMOS transistors in the stacked structure at the same time at higher incident angles [15].

VI. Conclusion

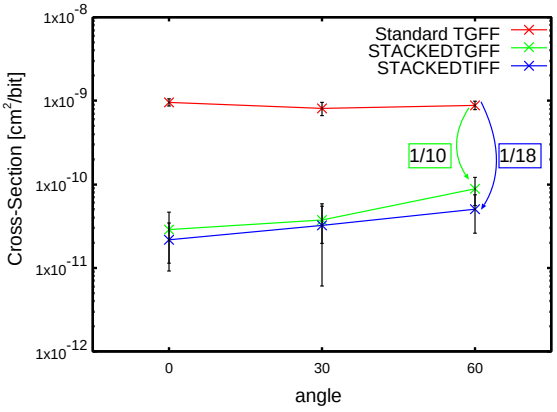
We examined radiation hardness of the standard TGFF, STACKEDTGFF and STACKEDTIFF in the 65 nm thin BOX FDSOI process. The D-Q delay time of STACKEDTIFF is 21% smaller than that of STACKEDTGFF. There was no error on STACKEDTGFF and STACKEDTIFF by neutron irradiation. There was no error on STACKEDTGFF and



(a)



(b)



(c)

Fig. 17. Experimental CSs depending on tilt angles when (DATA, CLK) = (0, 1). (a) Ar irradiation (b) Kr irradiation (c) Xe irradiation.

STACKEDTIFF at the tilt angles of 0° and 60° by Ar irradiation. Therefore, the stacked structure has enough soft-error tolerance in the terrestrial region in which secondary ions by neutrons have LET with less than 18 MeV-cm^2/mg. The stacked structure has over 60x and 10x stronger against soft errors than the standard TGFF at the tilt angles of 0° and 60° by Xe respectively.

STACKEDTIFF and STACKEDTGFF are strong against soft errors, while the D-Q delay of STACKEDTIFF is 21%

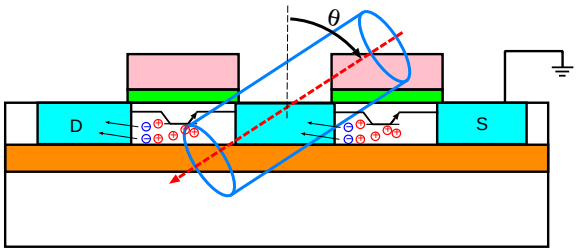


Fig. 18. Effect of two NMOS transistors as incident angle becomes higher.

smaller than that of STACKEDTGFF. STACKEDTIFF is better than STACKEDTGFF for high-speed applications with 9% area overhead.

Acknowledgment: The authors would like to thank to QST (National Institutes for Quantum and Radiological Science and Technology). The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC) in collaboration with Renesas Electronics Corporation, Cadence Corporation, Synopsys Corporation and Mentor Graphics Corporation. This work is supported by the Program on Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) from Japan Science and Technology Agency (JST).

REFERENCES

[1] R. Baumann. The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction. In Digest. International Electron Devices Meeting,, pages 329–332, Dec. 2002.

[2] D. G. Mavis and P. H. Eaton. Soft error rate mitigation techniques for modern microcircuits. In 2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320), pages 216–225, April 2002.

[3] T. Calin, M. Nicolaidis, and R. Velazco. Upset hardened memory design for submicron cmos technology. IEEE Transactions on Nuclear Science, 43(6):2874–2878, Dec 1996.

[4] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera. A low-power and area-efficient radiation-hard redundant flip-flop, dice acff, in a 65 nm thin-box fd-soi. IEEE Transactions on Nuclear Science, 61(4):1881–1888, Aug 2014.

[5] P. Roche, J. Autran, G. Gasiot, and D. Munteanu. Technology downscaling worsening radiation effects in bulk: Soi to the rescue. In 2013 IEEE International Electron Devices Meeting, pages 31.1.1–31.1.4, Dec 2013.

[6] Q. Wu, Y. Li, L. Chen, A. He, G. Guo, S. H. Baeg, H. Wang, R. Liu, L. Li, S. Wen, R. Wong, S. Allman, and R. Fung. Supply voltage dependence of heavy ion induced sees on 65 nm cmos bulk srams. IEEE Transactions on Nuclear Science, 62(4):1898–1904, Aug 2015.

[7] M. A. Xapsos, C. Stauffer, T. Jordan, J. L. Barth, and R. A. Mewaldt. Model for cumulative solar heavy ion energy and linear energy transfer spectra. IEEE Transactions on Nuclear Science, 54(6):1985–1989, Dec. 2007.

[8] J. S. Kauppila, T. D. Loveless, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. W. McCurdy, R. A. Reed, B. L. Bhuva, L. W. Massengill, and K. Lilja. Utilizing device stacking for area efficient hardened SOI flip-flop designs. In IEEE International Reliability Physics Symposium, pages SE.4.1–SE.4.7, June 2014.

[9] P. Oldiges, K. Rodbell, T. Ning, J. Cai, D. Heidel, H. Tang, L. Wissel, and M. Gordon. Stacked devices for seu immune design. In 2010 IEEE International SOI Conference (SOI), pages 1–2, Oct 2010.

[10] A. Makihara, M. Midorikawa, T. Yamaguchi, Y. Iide, T. Yokose, Y. Tsuchiya, T. Arimitsu, H. Asai, H. Shindou, S. Kuboyama, and S. Matsuda. Hardness-by-design approach for 0.15 um fully depleted CMOS/SOI digital logic devices with enhanced SEU/SET immunity. IEEE Trans. Nucl. Sci., 52(6):2524–2530, Dec. 2005.

[11] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura. Local$v_{\rm th}$variability and scalability in silicon-on-thin-box (sotb) cmos with small random-dopant fluctuation. IEEE Transactions on Electron Devices, 57(4):835–845, Apr. 2010.

[12] C. W. Slayman. Theoretical correlation of broad spectrum neutron sources for accelerated soft error testing. IEEE Transactions on Nuclear Science, 57(6):3163–3168, Dec. 2010.

[13] H. Asai, K. Sugimoto, I. Nashiyama, Y. Iide, K. Shiba, M. Matsuda, and Y. Miyazaki. Terrestrial neutron-induced single-event burnout in sic power diodes. In 2011 12th European Conference on Radiation and Its Effects on Components and Systems, pages 238–243, Sep. 2011.

[14] K. Yamada, M. Ebara, K. Kojima, Y. Tsukita, J. Furuta, and K. Kobayashi. Radiation-hardened structure to reduce sensitive range of a stacked structure for fdsoi. IEEE Transactions on Nuclear Science, pages 1–1, 2019.

[15] H. Maruoka, M. Hifumi, J. Furuta, and K. Kobayashi. A non-redundant low-power flip flop with stacked transistors in a 65 nm thin BOX FDSOI process. In 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS), pages 1–4, Sept. 2016.