Structure Dependence of Reduced Saturation Current Influenced by Source and Drain Resistances for 17 nm MOSFETs

Jong Chul Yoon, Akira Hiroki, and Kazutoshi Kobayashi
Graduate School of Science and Technology, Kyoto Institute of Technology,
Matsugasaki, Kyoto 606-8585 Japan
d0821005@edu.kit.ac.jp

Abstract— **In this work, we investigated the structure dependence of source and drain resistances on saturation currents for 17 nm bulk, SOI and Multi-Gate (MG) MOSFETs. An analytical saturation current model is proposed by considering with the higher order effects of source and drain resistances. For each structure, the saturation current (I_{Dsat}) were calculated by using the analytical current model. The reduction rates of the saturation currents for bulk, SOI and MG MOSFETs are 20.0, 21.6 and 19.7 %, respectively. It can be found that the reduction rate of SOI MOSFET is the largest. In order to find the physical reasons of the structure dependence, expansion components are analyzed. As a result, we found that the ratio of source resistance to channel resistance is the highly influential part.**

Keywords-MOSFETs; analytical model; series resistance.

I. INTRODUCTION

The electronic devices are required very high integration by huge data and high processing speed. In order to satisfy the requirement, CMOS has been scaled down in the sub-20 nm regime. In this region, SOI and Multi-Gate (MG) MOSFETs have been researched in order to improve the current capability [1][2]. In device design and development for the advanced structures, drain current reduction due to source and drain resistances becomes an important factor [3]. However, the effect of the resistances was considered by calculating 1st order approximation for saturation current [4].

In this work, we investigate the higher order effect of source and drain resistances for bulk, SOI and MG MOSFETs in the sub-20 nm regime. To investigate physical reason of structure dependences, the analytical model are analyzed including the effect.

II. ANALYTICAL MODEL

Fig. 1 shows an equivalent circuit of MOSFET with source and drain resistance. The circuit consists of an intrinsic MOSFET, a source resistance (R_S) and a drain resistance (R_D). From this circuit, the effective gate voltage (V'_{gs}) becomes ($V_{gs} - I_{Dsat}R_s$). The saturation current (I_{Dsat}) including an effect of the resistance by using the Taylor Expansion can be expressed as

$$I_{Dsat} = I_{Dsat0}\left[1 + A_1R_S + A_2R_S^2 + A_3R_S^3 + A_4R_S^4 + O_{(R_S^5)}\right] \quad (1)$$

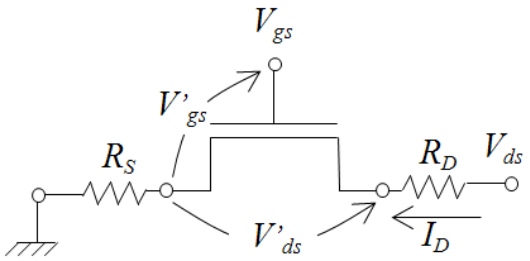

Figure 1. Equivalent circuit of MOSFET with source and drain resistances.

where A_1, A_2, A_3, and A_4 are the coefficients. We use the following Shichman and Hodges model [5] as the intrinsic MOSFET model.

$$I_{Dsat0} = \frac{1}{2}\mu_{eff}C_{ox}\frac{(V'_{gs}-V_{th})^2E_c}{(V'_{gs}-V_{th})+L_{el}E_c(1+d)}, \quad (2)$$

$$d = \frac{qN_{ch}\sqrt{2\varepsilon_S(2\varphi_F-V_b)/qN_{ch}}}{2C_{ox}(2\varphi_F-V_b)}. \quad (3)$$

Note that I_{Dsat0} is the saturation current when $R_S = R_D = 0$ Ω-μm, V_{th} is threshold voltage, μ_{eff} is effective mobility, C_{ox} is gate capacitance per unit area, L_{el} is effective channel length, E_c is critical electric field, N_{ch} is channel doping concentration, and V_b is applied substrate voltage. The 1st- and 2nd-order terms can be express as

$$A_1R_s = \frac{R_S}{R_{ch}}\cdot\frac{V_{dd}}{V_{gs}-V_{th}}\cdot\left[\frac{V_{gs}-V_{th}}{(V_{gs}-V_{th})+L_{el}E_c(1+d)} - 2\right] \quad (4)$$

$$A_2R_S^2 = \left[\frac{R_S}{R_{ch}}\right]^2\cdot\left[\frac{V_{dd}}{V_{gs}-V_{th}}\right]^2\cdot F \quad (5)$$

where F is function of V_{dd}, E_c, L_{el} and over-drive voltage, and R_{ch} is the channel resistance (V_{dd}/I_{Dsat0}). First part is a ratio of R_s to R_{ch}. The second part is a ratio of power supply voltage to over-drive voltage. The third part

TABLE I
USED PARAMETERS SUMMARY

The parameters	Device Structure		
	Bulk	SOI	MG
R_s [Ω-μm]	55	65	70
V_{dd} [V]	0.81		
μ_{eff} [cm²/Vs]	277	415	333
C_{ox} [μF/μm²]	4.33E-08	3.94E-08	3.25E-08
V_{th} [V]	0.229	0.184	0.164
E_c [MV/m]	7.93	5.31	6.61

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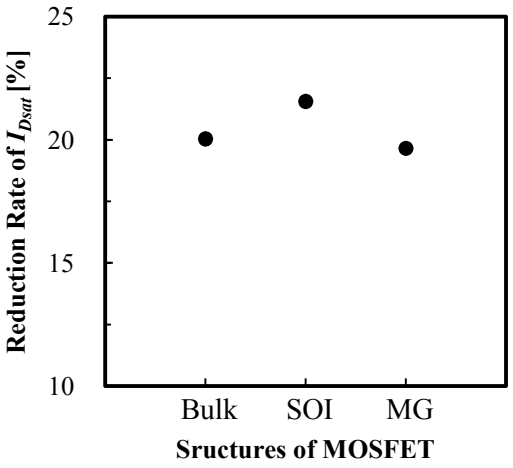

Figure 2. Reduction rates of saturation current as a function of the device structures.

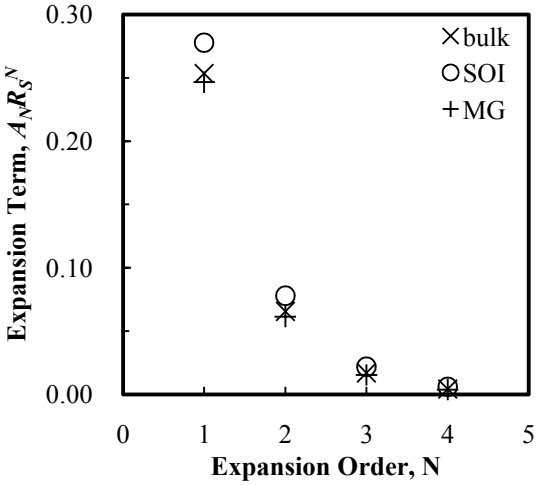

Figure 3. Expansion term ($A_N R_S^N$) vs. expansion order (N) for bulk, SOI and MG MOSFETs.

consists of over-drive voltage, effective gate length, and critical electric field.

Model parameters were extracted from ITRS data [6]. All transistor parameters are based on High Performance (HP) technology. Table 1 shows the parameters.

III. RESULTS

Fig. 2 shows reduction rates of saturation current as a function of device structures. The reduction rates are calculated as follows:

$$\text{Reduction Rate} = \left|\frac{I_{Dsat}-I_{Dsat0}}{I_{Dsat0}}\right| \quad . (6)$$

Reduction rates for bulk, SOI and MG MOSFET are 20.0, 21.6 and 19.7 %, respectively. In spite of the largest R_s, MG MOSFET shows the smallest reduction rate. In reduction rate of 17 nm MOSFETs, the effect of R_s for SOI MOSFET is largest than the others.

IV. DISCUSSIONS

In order to investigate the higher order terms, we compare 1st-order term with higher order terms. Fig. 3 shows expansion term ($A_N R_S^N$) vs. expansion order (N) for bulk, SOI and MG MOSFETs. For bulk, SOI and MG MOSFET, 1st-order terms are 0.25, 0.28 and 0.25, respectively. For bulk, SOI and MG MOSFET, 2nd-order terms are 0.07, 0.08 and 0.06, respectively. 1st-order terms of the I_{Dsat} are about 5 times larger than 2nd-order terms for all structures.

To investigate the physical reasons, 1st-order term is divided into three parts in (4). Fig. 4 shows normalized divided parts by bulk in 1st-order terms for bulk, SOI and MG MOSFETs. The ratios of R_s to R_{ch} (R_s/R_{ch}) are 1.25 and 1.14 for SOI and MG MOSFET, respectively.

In the SOI MOSFET, the largest reduction rate is caused by an increase of the ratio of R_s to R_{ch}. This increase is influenced by the suppressed R_{ch}. The suppression is induced by an enhancement of effective mobility because of smallest effective electronic field. In 2nd-order terms, first part is largest, too.

V. CONCLUSIONS

The influence of source and drain resistances to saturation current has been investigated for bulk, SOI and MG MOSFETs in 17 nm region. In this region, the reduction rate of I_{Dsat} for SOI MOSFET is the largest because of the higher mobility comparing with the other structures. It is found that reducing of the ratio of R_s to R_{ch} is essential in 17 nm MOSFETs design.

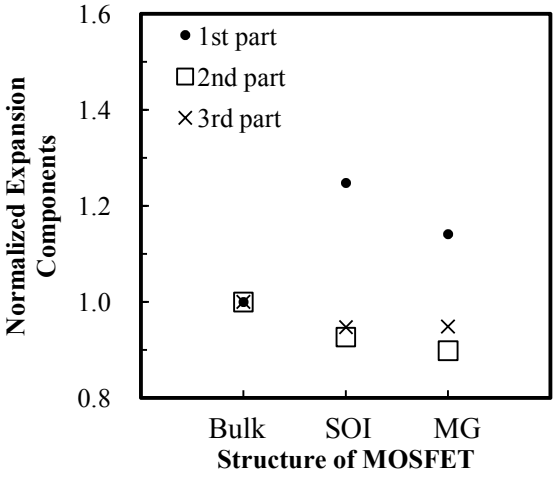

Figure 4. Normalized expansion components by components of bulk in the 1st-order terms for bulk, SOI and MG MOSFETs.

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