Circuit Characteristic Analysis Considering NBTI and PBTI-Induced Delay Degradation

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***Abstract*—Bias Temperature Instability (BTI) becomes one of the most important reliability issues for nanometer process devices. We focus on aging degradation by BTI because it is known as one of the dominant factor that determines life time of circuits. In this paper, we show circuit delay degradation characteristic of BTI using the circuit simulation. The delay increase 15% after 10 years stress.**

***Keywords*—BTI, aging degradation, reliability**

I. Introduction

Bias Temperature Instability (BTI) is an important reliability issue that causes threshold voltage ($V_{\rm th}$) shifts on scaled MOS transistors. BTI appears on PMOS transistors is called Negative BTI (NBTI) because $V_{\rm th}$ of PMOS transistors increases with time when gates are stressed by negative bias. BTI on NMOS transistors is called Positive BTI (PBTI). The defects generated in oxide capture and emit carriers which result in BTIs [1]. NBTI is known as one of dominant factors that determine life time of circuits after 65-nm process [2]. PBTI becomes the concern after 40-nm process. Therefore we should consider both BTIs as critical problems in the latest process.

In this paper, we analyze delay degradation of both BTIs on logic circuits. The degradation effects are different between the rising and falling edges of the signals. The rise and fall time delays are changed by the degradation and depend on the circuit conditions. We show the analysis results of the degradation in various conditions.

II. Simulation Setup

We evaluate delay degradation caused by both BTIs of an inverter (Fig. 1). The simulation conditions are as follows. Rectangle pulses with 1ns rise and 1ns fall time are applied to the circuits via two inverters. The output nodes of the circuits are connected to fan out 4 inverters. We apply $V_{\rm th}$ degradation to the parameters in the circuit netlists and they are changed through a device parameter $V_{\rm TH0}$ in the MOS model of BSIM4 [3]. The degradation time is from 1s to 10 years (3.15×10^8s).

We calculate $V_{\rm th}$ degradations with the Atomistic Approach model [4]. MOS transistors have N defects and each of them can be characterized by capture and emission time constants ($\tau_{\rm c}$ and $\tau_{\rm e}$). If the defect captures carriers, $V_{\rm th}$ of the device increases. The capture probability ($P_{\rm C}$) is a function of $\tau_{\rm c}$ and $\tau_{\rm e}$. The degradation ($\Delta V_{\rm th}$) at degradation time (t) can be calculated by Eq. (1).

$$\Delta V_{\rm th}(t) = \sum_{j=1}^{N} k_j(t)\cdot\mu_j \tag{1}$$

When the jth defect captures carriers, $k_j = 1$ and when carriers are emitted, $k_j = 0$. It is determined by $P_{\rm C}$. Parameter μ is $V_{\rm th}$ shift from a single defect. Each $\tau_{\rm c}$, $\tau_{\rm e}$ and μ is a statistical parameter. We use $\Delta V_{\rm th}$ of the average of 100 time calculations.

When the input signals are low, PMOS transistors are stressed and degraded by NBTI. When they are high, NMOS transistors are stressed and degraded by PBTI. Relationship between duty factor of the stress bias on PMOS transistors ($DF_{\rm p}$) and that on NMOS transistors ($DF_{\rm n}$) is as expressed $DF_{\rm p} = 1-DF_{\rm n}$. We evaluate the degradation of the condition $DF_{\rm p}/DF_{\rm n} = 0.0/1.0$ to $DF_{\rm p}/DF_{\rm n} = 1.0/0.0$. We assume the degradation rates of NBTI and PBTI are equivalent.

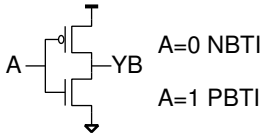

Fig. 1. NBTI and PBTI of a inverter circuit.

III. BTI-Induced Delay Degradation Analysis

The results of delay degradation analyses under both BTIs of an inverter are shown in Fig. 2 and Fig. 3. The results show the rise time delays ($T_{\rm dr}$) or the fall time delays ($T_{\rm df}$) increase with the degradation time and are degraded by 15% after 10 years in the condition of $DF_{\rm p} = 1.0$ or $DF_{\rm n} = 1.0$. In the condition of $DF_{\rm p} = 0.0$ or $DF_{\rm n} = 0.0$, the degradations affect a little on $T_{\rm dr}$ or $T_{\rm df}$.

The delays, $T_{\rm dr}$ and $T_{\rm df}$, increase due to the degradations. Because it becomes later for the gate voltage to exceed $V_{\rm th}$ than the initial condition when $V_{\rm th}$ increases. Those effect result in $T_{\rm dr}$ and $T_{\rm df}$ increases. In the condition of only NBTI effect ($DF_{\rm p}/DF_{\rm n} = 1.0/0.0$), $T_{\rm dr}$ increases and $T_{\rm df}$ slightly decreases. It shows the degradation of PMOS transistors has a large impact on $T_{\rm dr}$ but a small impact on $T_{\rm df}$ because $V_{\rm th}$ of PMOS transistors is only related to $T_{\rm dr}$. The result of the condition of only PBTI effect ($DF_{\rm p}/DF_{\rm n} = 0.0/1.0$) can be explained in a similar way.

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We show the duty factor characteristic in Fig. 4. The results show $T_{\rm dr}$ increases with $DF_{\rm p}$ and $T_{\rm df}$ increase with $DF_{\rm n}$. NBTI becomes dominant in the condition $DF_{\rm p} \geq 0.5$ and PBTI becomes dominant in the condition $DF_{\rm n} \geq 0.5$. Those can be explained in the same way as the preceding paragraph.

The average delay times of $T_{\rm dr}$ and $T_{\rm df}$ are shown in Fig. 5. The average delay times at a certain degradation time are almost constant as long as the circuits are caused by both BTIs. For example, the delay times are between 17.4ps and 17.6ps after 10 years. The average delay time degradations are bigger when both BTIs are effective ($0.1/0.9 < DF_{\rm p}/DF_{\rm n} < 0.9/0.1$) than when only NBTI or PBTI is effective ($DF_{\rm p}/DF_{\rm n} = 0.0/1.0$ or $1.0/0.0$).

IV. Conclusion

In this paper, we analyze NBTI and PBTI-induced delay degradation on CMOS inverters. The rise time delay or the fall time delay increase 15% after 10 years in the case that duty factor is 1. If the input signal is often low, NBTI becomes dominant on the delay degradation. If it is often high, PBTI becomes dominant on the delay degradation. The average of delay time degradations is almost constant except in the condition that the input signal is always high or low. In the condition, the delay degradation is smaller. Circuits can not avoid to degrade when we use it, but we can supress the degradation to consider the operating condition.

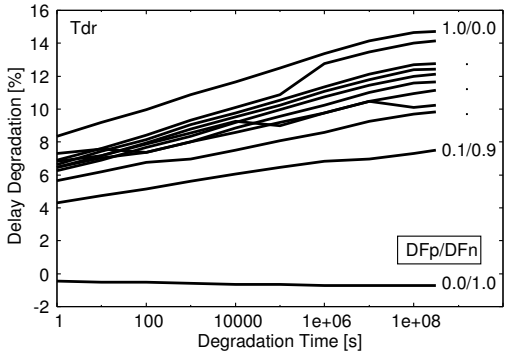

Fig. 2. Rise time delay degradation of CMOS inverters caused by both BTIs.

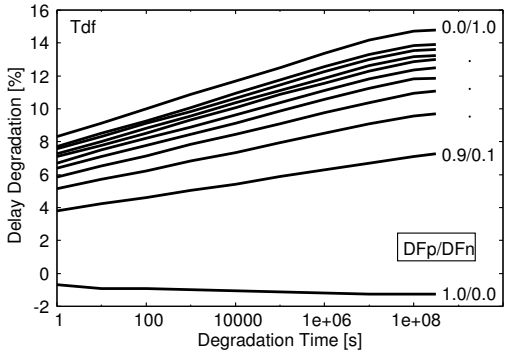

Fig. 3. Fall time delay degradation of CMOS inverters caused by both BTIs.

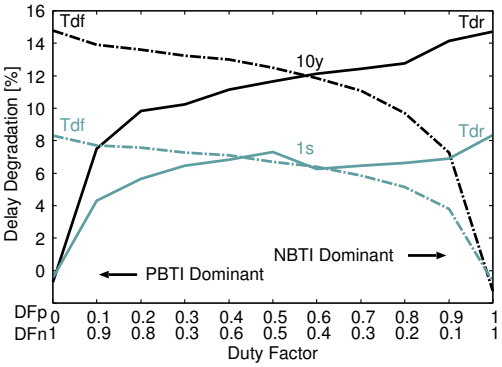

Fig. 4. Duty factor characteristic of rise and fall time delay degradation of CMOS inverters caused by both BTIs.

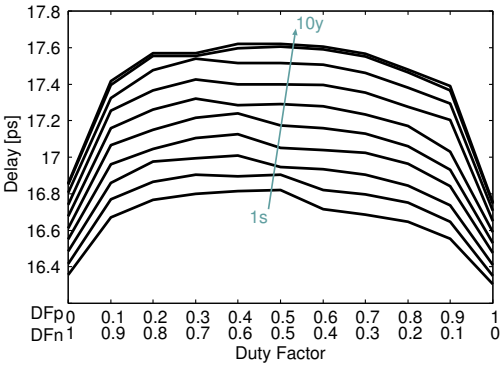

Fig. 5. Duty factor characteristic of average delay time degradation of CMOS inverters caused by both BTIs. The degradation times are from 1s to 10 years.

Acknowledgment

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