# An Estimation of Saturation Current Influenced by Source and Drain Resistances for Sub-20nm MOSFETs

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*Abstract*— **In this work, we investigate the influence of source and drain resistances to saturation currents for sub-20nm MOSFETs. New device structures such as Multi-gate and FinFET have been researched in sub-20nm regime. In design of the structures, it is necessary to consider the influence of source and drain resistances. In the ITRS report, saturation current has been estimated by using an analytical program: MASTAR. Therefore, it is necessary to evaluate an accuracy of MASTAR. The saturation currents calculated by MASTAR are compared with results of circuit simulations considering the source and drain resistances. The difference between MASTAR and circuit simulations increases from 4.23% to 5.97% as the gate lengths are scaled down to 18nm. Our results indicate that MASTAR overestimates the reduction of drain saturation currents due to the source and drain resistances.**

***Keywords- MOSFETs; circuit simulation; series resistances.***

## I. INTRODUCTION

With continued scaling of CMOS, drain current reduction due to source and drain resistances becomes an important factor for device design and development [1]. In the sub-20nm regime, Multi-Gate (MG) MOSFETs such as Double-Gate MOSFET and FinFET have been researched for the improvement of current driving capability [2]. The improvement is influenced by source and drain resistances. The influence has considered in ITRS report [3]. In ITRS report, the saturation currents are calculated by an analytical program: MASTAR. It calculates saturation current including the effects of source and drain resistances by using the 1st order Taylor expansion [4], [5]. The influence of resistances on drain current is increasing in the sub-20nm regime [6]. Therefore, it is necessary to evaluate an accuracy of MASTAR in this region. In this work, we investigate the influence of source and drain resistances to saturation current down to sub-20nm region. Saturation currents calculated by using MASTAR are compared with those of circuit simulations.

## II. CIRCUIT SIMULATIONS

We calculates the effect of source and drain resistances using circuit simulations solving the circuit equations numerically. Fig. 1 shows an equivalent circuit using the circuit simulations. The equivalent circuit consists of an intrinsic MOSFET, source resistance ($R_S$) and drain resistance ($R_D$). The intrinsic MOSFET was modeled using a

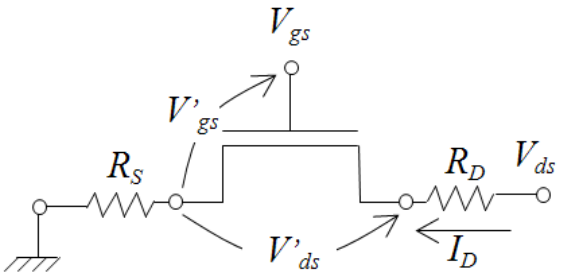


Figure 1. Equivalent circuit of MOSFET with source and drain resistances.

standard MOSFET model by Shichman and Hodges [7]. Model parameters were extracted from ITRS 2007 data [3]. $V'_{gs}$ and $V'_{ds}$ represent the gate and drain voltages for the intrinsic MOSFET, respectively. Test devices are based on Low Operating Power (LOP) technology and Low Standby Power (LSTP) technology. In LOP, $R_S$ and $R_D$ are 95 Ω-μm. In LSTP, $R_S$ and $R_D$ are 90 Ω-μm. Saturation currents ($I_{Dsat}$) are simulated at $V_{ds} = V_{gs} = V_{dd}$. Power supply voltages ($V_{dd}$) are 0.7–0.8 V for LOP and 1.0–1.1 V for LSTP. $I_{Dsat0}$ is defined saturation current when $R_S = R_D = 0$ Ω-μm. We compared $I_{Dsat}$ of circuit simulations with that of MASTAR.

## III. RESULTS AND DISCUSSION

Fig. 2 shows $I_{Dsat}$ normalized by $I_{Dsat0}$ for LOP. $I_{Dsat}$ was calculsted by using MASTAR and circuit simulator. Results of MASTAR are lower than those of circuit simulations in whole gate lengths. Fig. 3 shows reduction rates of $I_{Dsat}$ as a function of the gate length for LOP. Reduction rate of MASTAR increases from 27.2% to 38.7% as the gate length decreases. Reduction rate of circuit simulations increases from 22.5% to 33.7% as the gate length decreases. Differences between MASTAR and circuit simulations results are from 4.69% to 5.97%.

Fig. 4 shows $I_{Dsat}$ normalized by $I_{Dsat0}$ for LSTP. $I_{Dsat}$ using MASTAR are lower than those of circuit simulations in whole gate lengths. Fig. 5 shows reduction rates of $I_{Dsat}$ as a function of the gate length for LSTP. Reduction rate of MASTAR increases from 20.0% to 38.7% as the gate length decreases. Reduction rate of circuit simulations increases from 15.8% to 24.3% as the gate length decreases.

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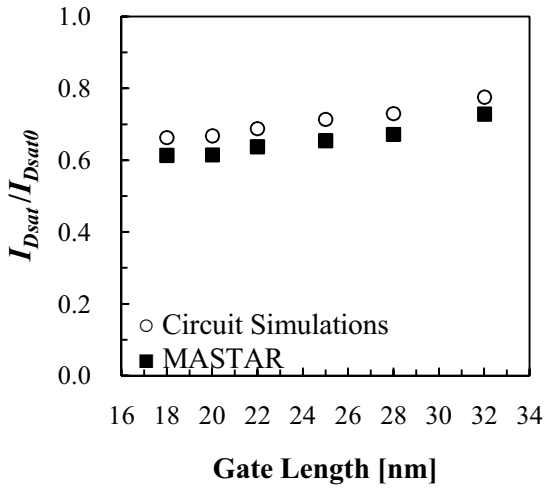


Figure 2. Saturation current $I_{Dsat}$ ($R_S$, $R_D$) normalized by saturation current $I_{Dsat0}$ ($R_S$ =$R_D$ = 0 Ω-μm) for LOP technology.

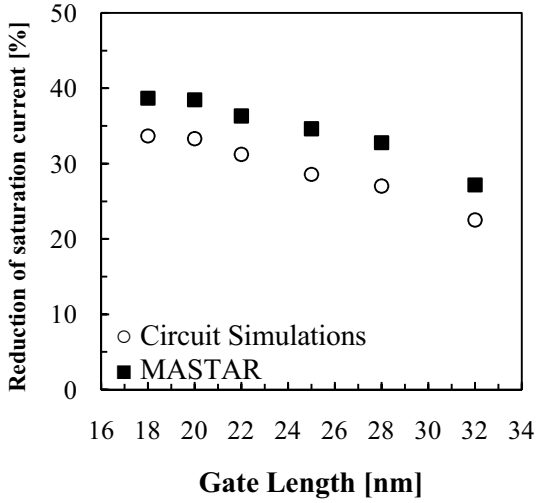


Figure 3. Reduction rates of saturation current vs. the gate length for LOP technology.

Differences between MASTAR and circuit simulations results are from 4.23% to 5.55%.

## IV. CONCLUSIONS

For evaluation an accuracy of MASTAR, we investigate influence of the source and drain resistances on saturation current by comparing $I_{Dsat}$ of circuit simulations with that of MASTAR. Reduction rates of $I_{Dsat}$ by using MASTAR are lower 4.23 % - 5.97 % than those by doing circuit simulations. Our results indicate that MASTAR overestimates the reduction of saturation currents by the source and drain resistances.

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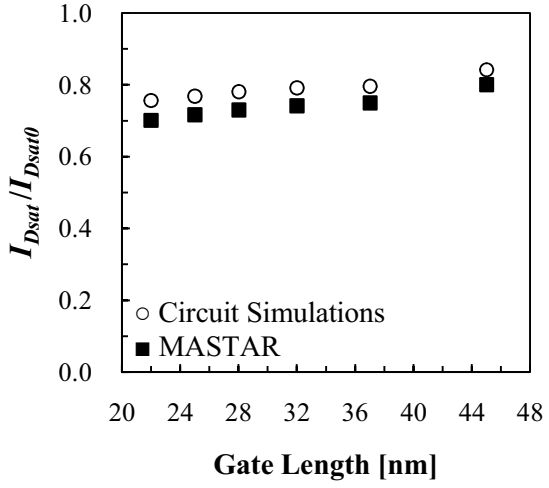


Figure 4. Saturation current $I_{Dsat}$ ($R_S$, $R_D$) normalized by saturation current $I_{Dsat0}$ ($R_S$ =$R_D$ = 0 Ω-μm) for LSTP technology.

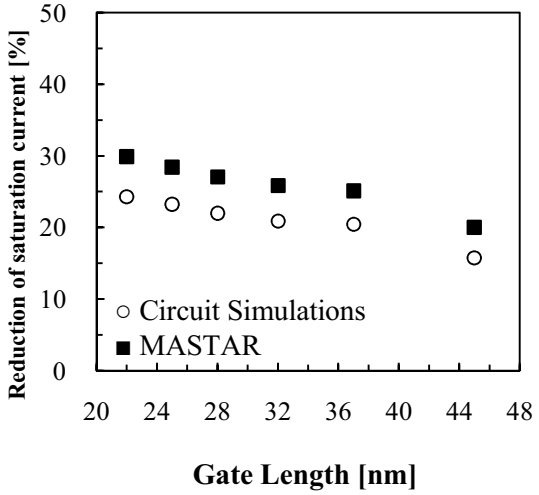


Figure 5. Reduction rates of saturation current vs. the gate length for LSTP technology.

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