Circuit-level Insight of Soft Errors and Aging Degradations

Kazutoshi Kobayashi
Kyoto Institute of Technology
Japan
kazutoshi.kobayashi@kit.ac.jp
Outline

• Reliability Issues in VLSIs
• My Experience of Reliability
• Soft Errors
  – What is soft error?
  – How to measure soft errors
  – Mitigation technique and our proposed radiation-hard flops
• Circuit Reliability
  – RO-based BTI-induced degradation measurement
  – VDD and VBB control to suppress BTI-induced degradation while keeping circuit performance.
  – How PID influences initial and aging degradation
Reliability Issues in VLSIs

- Infant Mortality failure
- Wear out failure
- Temporal failure

Bathtub Curve

Wear Out (Aging)

Infant Mortality

Temporal (Soft error)

Time

High-energy neutron

Particles

Nuclear Reaction

Wires or Gates

LER

voids

Wires or Gates

BTI

Thermal neutron

Alpha particle
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First Step to Reliability

- In 2007, Japanese funding agency starts a research project named “Dependable VLSI”.
  - Our project is “Dependable VLSI Platform using Robust Fabrics” managed by Prof. Onodera (Kyoto Univ.)
From Novice to Expert

- I was a novice researcher in the field of reliability in 2007.
  - In 2007, “FIT is the number of errors in $10^9$ hours” on my notebook.
  - I did not know the word “RTN”.
    • “What is telegraph?”

- First attendance of IRPS in 2008
- First soft error paper in VLSI symposium in 2010
- First soft error paper on IRPS in 2011
  - 15 papers + 1 tutorial on IRPS from 2011 to 2022. Best poster award in 2013

- IEDM RSD TPC member (2019–20), IRPS Circuit Reliability topic chair (2022)
Paper Lists of Reliability

- 138 papers (including international conferences) were published from 2009 to 2022.
- Most-cited papers (by Scopus)
  - J. Furuta, K. Kobayashi, and H. Onodera, “Impact of Cell Distance and Well-contact Density on Neutron-induced Multiple Cell Upsets”, IEEE IRPS, 2013 (23 citations)

Red: Soft errors        Blue: Circuit Reliability

Full List on  http://www-vlsi.es.kit.ac.jp/database/paper-e.php5
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What is Soft Error?

- Caused when a radiation particle penetrates in Si and generates e−h pairs
  - When neutron hits a Si atom (not always). Whenever α particle go through chip
- Upset storage cells such as SRAMs/FFs
- A pressing issue of semiconductor chips for automotive, aerospace and HPC
- Not so many companies / researchers knows well about soft errors. Unknown errors → Soft errors?
Scaling Trend of Soft Error Rate (SER)

- **Constant # of errors / area**
- **Decreasing # of errors / area**

### Process Node

- **65 nm**
- **45 nm**
- **32/28 nm**
- **22/20 nm**
- **14 nm**
- **10 nm**

### FinFET

- **0.5x / Gen [Intel 14nm]**
- **0.2x / Gen [Intel 14nm]**

### Bulk

- **Our Measurement Data [TNS11, 14]**
- **Scaled by [UemuraPhD]**
- **Scaled by [Intel 22nm]**
- **Scaled by [Intel 14nm]**
- **Scaled by [Samsung 10nm]**

### References

SEU Mitigation Techniques

- Dual lock-step on architecture level
  - For automotive and aerospace
- Parity and ECC on circuit/algorithm level
  - For SRAM and DRAM
- Majority voting on circuit level
  - For latches and flip flops
- SOI/FinFET on process/device level
  - For automotive and HPC

[12] Dual lock-step

[M. Baleani, et al., CASES, 2013]
Soft Error Mitigation Techniques

- **Circuit-level**
  - **Majority Voting** such as TMR, DICE, BCDMR FF and etc.
  - Large area, delay and power (ADP) overheads

- **Process-level**
  - SOI (Silicon on Insulator)
    - 10-100x stronger than bulk
    - No ADP overhead, but more expensive to fabricate
  - FinFET
    - Strong but huge cost (Only for iPhone, FPGA ⋯)
  - Circuit-level technique for SOI
    - Stacked Structure

[Diagram of TMR FF, DICE Latch, Stacked FF]

References:

- [A. Makihara, TNS 2004]
- [T. Calin et.al, TNS 1996]
BISER FF

- Built-in Soft-Error Resilience FF
  - Developed by Intel and Stanford
  - Two latches and a weak keeper hold data
  - C-element resolves SBU on latches
  - Area efficient but weak to an SET (Single event transient) pulse from the C-element

BCDMR FF [Furuta et.al, VLSI Cir. 2010]

• Bistable Cross–coupled Dual Modular Redundancy FF
  - Strong against an SET pulse from C–element
  - Duplicated C–elements **strongly** assists to keep correct data. No area–overhead because of smaller transistors on C–elements

<table>
<thead>
<tr>
<th></th>
<th>Area</th>
<th>Delay</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>BISER</td>
<td>3.00</td>
<td>1.47</td>
<td>2.15</td>
</tr>
<tr>
<td>BCDMR</td>
<td>3.00</td>
<td>1.45</td>
<td>2.20</td>
</tr>
</tbody>
</table>

Normalized by Standard FF

Drive strength  
Ce : Wk = **10 : 1**

Weak keeper(Wk)
C-element(Ce)

Assist

Strong keeper(Sk)

Drive strength  
Ce : Sk = **5 : 2**
Alpha and Neutron Results

- BCDMR is strong against soft errors at higher clock frequency
- Below 10 FIT at 100MHz. BISER in twin well is 50 FIT. BCDMR FF in twin well has no error

Fabricated in a 65 nm bulk
BCDMR FF in Scaled Technology

- Similar SERs b/w 65nm interleaved and 16nm not-interleaved BCDMR
  - Interleaved layout decreases SER

[K. Kobayashi, et. al. IRPS 2017]
Soft Errors in Bulk and SOI

**Bulk**

- Particle hit
- Gate
- Source
- Drain
- n+ on top
- p-Si on bottom

**SOI**

- Particle hit
- Gate
- Source
- Drain
- n+ on top
- BOX layer
- p-Si on bottom

- BOX layer prevents carriers from collecting from substrate
- SOI is resistant to soft errors. SER is 1/10–1/100 of bulk

[P. Roche, IEDM, 2013]
Experimental Results of Standard FF

All FDSOI chips were fabricated in a 65nm thin BOX FDSOI process


Soft-error Mitigation for SOI

• Stacked Transistor Structure on SOI

- No simultaneous turn-on
  – All transistors are isolated by BOX layer.
  – Not effective on bulk process

- With area and delay overheads

- 1/3 to 1/10 SER reduction on stacked FF

[Source: A. Makihara, TNS 2004]
Stacked Latch on HPC Processor

- 22nm IBM System z Microprocessor

- Additional transistors on latch
  - This figure was not included in the paper, but in slides

[J. Warnock ISSCC15, 4.1]
Guard–Gate Flip Flop (GGFF)

- 100x higher soft-error tolerance in 16 nm FinFET
  - Longer delay and 12 additional trs.

[A. Balasubramanian, IEEE TNS, vol. 52, no. 6, pp. 2531–2535, 2005.]
[H. Zhang et al., IRPS, pp. 5C–3–1–5C–3–5, 2016]
Filtering Out SET Pulse by Guard Gate

- Two inverters delay SET pulse
  - Output of C-element is stable if $\tau >$ SET pulse width
  - Delay time to flip latch becomes long (+$\tau$)
Feedback Recovery FF

- Construct guard gate by master and slave latches
  - FRFF
    - Only 2 additional transistors
    - Only master latch is strong
  - DFRFF
    - 6 additional transistors
    - Both of master/slave latches are strong

[K. Yamada et al, IEEE S3S, 2018]
## Circuit Performance in 65 nm FDSOI

<table>
<thead>
<tr>
<th>FF</th>
<th>Area</th>
<th>Delay</th>
<th>Power</th>
<th>ADP</th>
<th># Tr.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard FF</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>24</td>
</tr>
<tr>
<td>Guard-Gate FF</td>
<td>1.47 (1)</td>
<td>2.20 (1)</td>
<td>1.06 (1)</td>
<td>3.42</td>
<td>36</td>
</tr>
<tr>
<td>FRFF</td>
<td>1.06 (0.72)</td>
<td>1.06 (0.48)</td>
<td>1.03 (0.97)</td>
<td>1.16</td>
<td>26</td>
</tr>
<tr>
<td>DFRFF</td>
<td>1.18 (0.80)</td>
<td>1.08 (0.49)</td>
<td>1.02 (0.96)</td>
<td>1.29</td>
<td>30</td>
</tr>
</tbody>
</table>

FRFF is faster because of the number of inverters from input to output.
Neutron Irradiation Results

- Guard gate FF w/ 240% ADP o.v. is strongest, but FRFF w/ 16% o.v. and DFRFF w/ 30% o.v. have 3–4x radiation hardness than Standard FF
Heavy-ion Results

- **ML on FRFF is stronger against soft errors than SL because of delay time**
  - More delay is required on SL
- **Average CSs of DFRFF 1/20 and 1/6 smaller than those of TGFF by Ar and Kr**
  - Kr produces longer error pulse than Ar
DFRFF in 22 nm FDSOI

• DFRFF and DFFRFFLD (Long-Delay version) were designed and fabricated in 22 nm FDSOI with the collaboration of Dolphin Design since 2019 (Vincent Huard)

• Just presented in RADECS 2022 last week in Venice

• DFRFFLD 100x more radiation-harder than standard FF
  - Ready for automotive and aerospace applications.

• Another paper also designed and measured our DFRFF in the same 22 nm FDSOI
  - Authors stated “We designed 14 FFs. But DFRFF is strongest of all!” 😊
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**Bias Temperature Instability (BTI)**

- Aging degradation
  - NBTI (Negative BTI)
    - $V_{gs}$ of PMOS $< 0$ V
  - PBTI (Positive BTI)
    - $V_{gs}$ of NMOS $> 0$ V

- Dangling bonds in gate oxide or defects in gate oxide

- $V_{th}$ by trapping carriers

- Time constant to trap carrier distributed from $10^{-9}$ to $10^{9}$ s
ROs to Measure Aging Degradation

• Only NAND–gates Ring Oscillator
  - EN = 0 : RO stops and PBTI occurs.

• Only NOR–gates Ring Oscillator
  - ENB = 1 : RO stops and NBTI occurs.
NBTI–sensitive and –insensitive RO

NBTI–sensitive RO
- NBTI is accelerated
- $|V_{gs}| = VDD \gg Vth$

NBTI–insensitive RO
- NBTI is suppressed
- $|V_{gs}| = Vth$
PBTI-sensitive and -insensitive RO

PBTI-sensitive RO

- PBTI is accelerated
- $|V_{gs}| = VDD \gg Vth$

PBTI-insensitive RO

- PBTI is suppressed
- $|V_{gs}| = Vth$
Extract BTI w/o Fluctuations

- Temporal bias/temperature fluctuations for long-term measurement affect measurement results
- **Goal:** Extract BTI w/o fluctuations by subtraction b/w BTI-sensitive and -insensitive ROs
Test Chip & Measurement Setup

Fabricated in a 65 nm FDSOI technology

<table>
<thead>
<tr>
<th>Structure</th>
<th>Number of ROs</th>
</tr>
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<tbody>
<tr>
<td>PBTI-sensitive</td>
<td>840 in all ROs</td>
</tr>
<tr>
<td>PBTI-insensitive</td>
<td></td>
</tr>
<tr>
<td>NBTI-sensitive</td>
<td></td>
</tr>
<tr>
<td>NBTI-insensitive</td>
<td></td>
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Measurement system
Engineering Tester + Peltier Heater
Measurement Results (PBTI & NBTI)

- Osc. Freqs. of NBTI and PBTI ROs fluctuate around $5 \times 10^3$ second
  - May be due to temperature or voltage fluctuations
  - Can be removed by subtraction
Subtraction Results

- **Fluctuations are removed by subtraction!!**
  - Smoothly increase with time
- **PBTI**: logarithmic (slightly-power-law)
  - NBTI: power-law

\[ \text{PBTI (NAND) RO} \]
\[ \text{NBTI (NOR) RO} \]
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BTI Suppression to control $V_{DD}$ & $V_{BB}$

- BTI-induced Degradation $\propto t^n$
- NBTI can be suppressed to reduce $V_{DD}$
  - NBTI-induced degradation becomes $< 10\%$ at $V_{BB} = 0.20 \text{ V}$
- $V_{BB}$ (body bias) is controlled to compensate performance degradation
  - Pros: suppress BTI and dynamic power
  - Cons: increase static power
  - BTI Time exponent $x P_{\text{dynamic}} \times P_{\text{static}}$ is almost constant

[1. Suda et al, IRPS 2022, P4]
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Plasma Induced Damage (PID)

Charging damage from antenna during back-end-of-line (BEOL) metallization process

- **Generate defects**
  - gate oxide breakdown
  - threshold voltage ($V_{th}$)
  - oscillation frequency

- **Multilayer wiring**
- **Thin gate oxide**
- **PID** has become a serious reliability issue
Antenna Ratio (AR)

- Antenna Ratio (AR)
  \[ \frac{\text{Antenna area}}{\text{Gate area}} \]

- Strength of PID

- Upper limit: 500

- Difficult to stay below AR 500 in large scale circuits

How PID affects initial and aging degradation?
Ring Oscillators to measure PID

1. Current starved RO to measure initial degradation by PID
   – PMOS b/w VDD and RO VDD (virtual VDD)

2. Measure correlation b/w initial and aging degradation
   – Antennas on wires inside Ring Oscillators (ROs)

[R. Kishida et al, SSDM 2017]

[R. Kishida et al, JJAP, 2015]
PMOS Type Current Starved RO

- PMOS w/o antenna (Ref.Tr.) as reference
- PMOS w/ antenna (PID Tr.)
- $|V_{th}|$ of PID Tr. increases Virtual VDD voltage and frequency
NMOS Type Current Starved RO

- NMOS Trs. b/w GND and RO GND
- $|V_{th}|$ of PID Tr. increases
  Virtual GND voltage and frequency
- Compare frequencies w/ Ref. and PID Tr.
  to evaluate PID depending on antenna layers
Test Chip

- 65 nm FDSOI process
- 2 mm x 1.5 mm
- 70 ROs
- 2k \textit{antenna ratio}
  - Metal area / Gate area
  - 4x bigger than the upper limit

Measurement conditions
- 1.0 V (nominal)
- Room Temp.
Measurement Results of Initial Frequencies in PMOS and NMOS

- Freq. is decreased by increasing metal layers in PMOS
- **Higher** Freq. in NMOS Trs. than Ref. Tr.
  - $|V_{th}|$ decreases by PID
- Freq. become **lower** from M2 to M5.
  - Why? – Because of positive charging damage in high-k (HK)
Positive charging damage in HK dielectrics [6]

SiON and HK in fabricated process

$|V_{th}|$ by PID in SiON

$|V_{th}|$ by positive charge in HK of NMOS

[ K. Eriguchi et al., *ICICDT*, 2008]
RO to measure initial and aging degradation

- RO composed of NORs
  - Only the last NOR (N11) suffered from PID and NBTI

[R. Kishida et al, S3S, 2016]
Measurement Flow

• Initial frequency to evaluate PID
• Oscillation stop to induce NBTI
• Measure frequency after NBTI stress
  – Frequency decrease by NBTI.
Test Chip

- 65 nm process
- 1.8 V
- 80 °C
- AR: 100–1k every 100
- 576 ROs of each AR
- Bulk and thin-BOX FDSOI
NBTI Measurement

- Dots: average of measurements
- Fitting: $f(t) = S_{NBTI} \log(t + 1) + f_0$
  - $S_{NBTI}$: degradation factor
  - $f_0$: initial frequency
Degradation Factor $S_{NBTI}$

- Similar tendencies in bulk and FDSOI
  - NBTI caused by PID in FDSOI can be estimated to be the same as in bulk
- NBTI is accelerated by PID when $\leq AR=600$
  - Should consider NBTI caused by PID even within the AR limit
- $S_{NBTI}$ $\rightarrow$ (AR600) $\leftarrow$ NBTI correlates initial frequency?
Correlation b/w NBTI and Initial Frequency

- **Correlation coefficient** ($\rho$) = 0.24 *(weak)* in bulk
  - RDF (random dopant fluctuation) is dominant than gate oxide variation

- **$\rho = 0.68$ *(strong)* in FDSOI
  - Gate oxide variation is dominant than RDF
    - Slower ROs w/ higher $V_{th}$ have smaller electric fields
Conclusion

• We have been researching reliability issues in circuit level for 15 years. Over 100 papers were published.

• Our activities are mainly focused to soft errors and aging degradation

• Many radiation-hard flip-flops were proposed, fabricated and measured.
  - Recent work was done in 22-nm FDSOI with the collaboration of Dolphin Design

• BTI-induced aging degradation can be measured by BTI-sensitive and -insensitive ROs.

• BTI-suppression method to control VDD and VBB while keeping circuit performance

• PID-induced damage was measured by ROs.
  - Upper layer antenna damages gate dielectrics to decrease PMOS Vth and increase NMOS Vth.
  - Correlation b/w initial and aging degradation is strong in FDSOI but weak in bulk
Acknowledgement

• All members of our VLSI–system Lab. in KIT.

2009

• d.lab VDEC in Univ. of Tokyo for chip fabrication and EDA support

• All corporate collaborators

2022
Low power FF

- Adaptive Coupling FF (ACFF)
  - Low power w/o clock buffer

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</tr>
<tr>
<td>ACFF</td>
<td>1.00</td>
<td>1.46</td>
<td>0.55</td>
<td>22</td>
</tr>
</tbody>
</table>

AC element attenuates SET pulse to decrease critical charge ($Q_{crit}$)

[H. Maruoka et al, RADECS, 2016]

Low Power Radhard FFs

Both FFs achieve low power at low data activity and low SER.

Neutron SER [FIT/Mbit]

- Both FFs achieve low power at low data activity and low SER

Measurement Results of Initial Frequencies in PMOS

- Normalized Frequency (Freq.) = $f_{\text{PID}}/f_{\text{Ref}}$
  - How the initial frequency differs from that of Ref. Tr.
- Lower Freq. in PID Trs. than Ref. Tr.
- Degraded by PID as upper metal layers
  - 3.1% decreases from Ref. to M5