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Nonvolatile Storage Cells Using FiCC for IoT Processors with Intermittent Operations

Yuki ABE[†a)], ***Student Member***, **Kazutoshi KOBAYASHI**[†b)], ***Senior Member***, **Jun SHIOMI**[††c)], ***and*** **Hiroyuki OCHI**[†††d)], ***Members***

SUMMARY Energy harvesting has been widely investigated as a potential solution to supply power for Internet of Things (IoT) devices. Computing devices must operate intermittently rather than continuously, because harvested energy is unstable and some of IoT applications can be periodic. Therefore, processors for IoT devices with intermittent operation must feature a hibernation mode with zero-standby-power in addition to energy-efficient normal mode. In this paper, we describe the layout design and measurement results of a nonvolatile standard cell memory (NV-SCM) and nonvolatile flip-flops (NV-FF) with a nonvolatile memory using Fishbone-in-Cage Capacitor (FiCC) suitable for IoT processors with intermittent operations. They can be fabricated in any conventional CMOS process without any additional mask. NV-SCM and NV-FF are fabricated in a 180 nm CMOS process technology. The area overhead by nonvolatility of a bit cell are 74% in NV-SCM and 29% in NV-FF, respectively. We confirmed full functionality of the NV-SCM and NV-FF. The nonvolatile system using proposed NV-SCM and NV-FF can reduce the energy consumption by 24.3% compared to the volatile system when hibernation/normal operation time ratio is 500 as shown in the simulation.

key words: *Internet of Things (IoT), Energy harvesting, Standard Cell Memory (SCM), Flip-Flops, Metal fringe capacitor, Nonvolatile processor (NVP)*

1. Introduction

In recent years, Internet of Things (IoT), 5G, and other information and communication technologies have made significant progress [1]–[3]. In particular, IoT technologies provide great opportunities to monitor, analyze, and control the physical world we interact with, but power supply to these devices is a significant barrier to IoT adoption [4]. Today, batteries are embedded in most of mobile devices such as laptops and smartphones. However, in the future IoT applications, which are much more ubiquitous than current mobile systems, batteries face dimension, maintenance, and pollution issues [5]. Energy harvesting has been widely investigated as a potential substitute for batteries [6], [7]. Energy can be scavenged from the surrounding environment, such as mechanical vibration, thermal differences, ambient radio waves, and sunlight. Under these conditions, computing devices must operate intermittently rather than continuously, because surrounding energy is unstable [8]. Therefore, processors for IoT devices with intermittent operation must feature a hibernation mode with zero-standby-power in addition to energy-efficient normal mode [9].

One of the most effective ways to reduce the energy consumption of integrated circuits is to scale the power supply voltage. In [10], it was shown that scaling the supply voltage to near the transistor threshold voltage improved the energy efficiency of the processor by up to 4.7 times. However, in such a low-voltage region, the reliability issue of semiconductor chips due to process variations becomes prominent [11], [12]. On chip memories, such as SRAM, are vulnerable to process variations [13]–[15]. SRAM is hard to operate in the low voltage region due to process variations among millions of transistors. A standard cell memory (SCM) has been proposed as an alternative to SRAM [16]. D-latches or D flip-flops are used in the bit cells, and the peripheral circuits are implemented using random logic. The circuit is implemented using only CMOS digital circuits, which enables stable operation in the ultra low voltage region. In [17], a 4-kbit SCM operates at the supply voltage of 350 mV.

One of the most effective ways to achieve zero-standby-power, the nonvolatile power gating (NV-PG) technique has been widely adopted to cut off static leakage power [18], [19]. NV-PG architecture uses nonvolatile bistable circuits such as a nonvolatile SRAM (NV-SRAM) and a nonvolatile flip-flop (NV-FF). This architecture mainly has two modes: normal operation and shutdown modes. In the normal operation mode, nonvolatile data retention is disabled. Thus, the NV-SRAM and NV-FF circuits execute only the ordinary SRAM and FF operations in the normal operation mode. In the shutdown mode, circuit domains or systems are turned off after storing data in nonvolatile memory. Each data bit residing in the volatile SRAM or flip-flops is stored in the corresponding nonvolatile memory bit before turn-off. NV-SRAM and NV-FF enable a dramatic reduction of overheads in energy and latency during store/restore operations, unlike the conventional architecture using external backup storage which requires long-distance data transmission.

In previous studies, nonvolatile SCM (NV-SCM) using Magnetic Tunnel Junction (MTJ) element [20] and NV-FF using MTJ and ferroelectric element were proposed [21]–[26]. But they cannot be fabricated in a conventional stan-

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[†]The author is with Department of Electronics, Kyoto Institute of Technology, Matsugasaki, Sakyo, Kyoto, 606-8585 Japan
[††]The author is with Graduate School of Information Science and Technology, Osaka University, 1-5, Yamadaoka, Suita, Osaka, 565-0871 Japan
[†††]The author is with College of Information Science and Engineering, Ritsumeikan University, 1-1-1, Noji-higashi, Kusatsu, Shiga, 525-8577 Japan
a) E-mail: yabe@vlsi.es.kit.ac.jp
b) E-mail: kazutoshi.kobayashi@vlsi.es.kit.ac.jp
c) E-mail: shiomi-jun@ist.osaka-u.ac.jp
d) E-mail: ochi@cs.ritsumei.ac.jp
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dard CMOS process technology. It is compatible with a CMOS process but additional masks and semiconductor manufacturing equipment are required.

Inspired by the nonvolatile memory element using Fishbone-in-Cage Capacitor (FiCC) [27], a sort of metal fringe capacitor, this paper proposes to adopt it for an NV-SCM and an NV-FF, presents layout designs and measurement results in them, and shows the effectiveness of nonvolatile system using them. They can be fabricated in a conventional CMOS process without any additional mask. Therefore, it enables to design processors for IoT devices easily. The organization of this paper is the following. Section 2 gives a description of a nonvolatile memory using FiCC. The proposed D-latch for NV-SCM and NV-FF are described in Section 3. Section 4 presents some measurement results of an NV-SCM and an NV-FF. Section 5 describes simulation results of sequential circuits using the proposed NV-SCM and NV-FF. A brief conclusion is presented in Section 6.

2. Nonvolatile Memory Using FiCC

2.1 Fishbone-in-Cage Capacitor (FiCC)

The metal fringe capacitor (MFC) [28] is a capacitor that consists only of metal wire segments and utilizes the capacitance between them. Among capacitors that can be configured on an Application Specific Integrated Circuit (ASIC), MFCs have the advantages of (1) no additional mask in a standard CMOS process and (2) ideal linear characteristics. Thanks to the process technology scaling, thinner wire width and shorter distance between wires increase capacitance per area [29], [30]. However, since MFCs use fringe capacitance between metal wire segments, they are influenced by a crosstalk capacitance with neighboring wires and capacitors. Layout designers must consider them. In a previous study, a shielding metal wall was introduced for each capacitor to reduce the crosstalk capacitance by paying the cost of area overhead [31].

FiCC [27] was proposed to address those issues. FiCC is an MFC that consists of outer electrodes and inner electrodes. The 3D structure of FiCC is shown in Fig. 1. The electrodes in blue and red are the outer-side and inner-side electrodes, respectively, and the electrodes on the same side are connected vertically through vias. By connecting a noise-sensitive net to the inner electrode and a low-impedance net with a stable potential such as GND or VDD to the outer electrode, the former is shielded like a Faraday cage. This structure can suppress the crosstalk capacitance between the inner terminal and other neighbor wires or capacitors to 1/10.

2.2 Nonvolatile Memory Using FiCC

Nonvolatile memory using FiCC is a CMOS-compatible memory element composed of a FiCC and an NMOS transistor, forming a circuit equivalent to the Floating Gate (FG) structure of a flash memory element. A nonvolatile memory using FiCC is shown in Fig. 2. The node that consists of the gate terminal and the FiCC's inner electrode is isolated from the outer electrode by an insulator and acts as a floating gate. The back gate terminal of the NMOS transistor is connected to GND. The write and erase operations of the nonvolatile memory are shown in Figs. 3 and 4, respectively. The write operation is performed by applying 5.0 V to the Control Gate (CG) to induce Fowler-Nordheim (FN) tunneling and trap electrons in the FG. The erase operation is performed by pulling electrons out of the FG using FN-tunneling by applying an opposite voltage between CG and Drain. By applying the write voltage of 5.0 V for 5 seconds to the CG of a nonvolatile memory using FiCC, the threshold voltage can be increased to 4 V, and the threshold voltage shift can be observed for approximately 13 days [27]. It is also shown that the memory characteristics do not change significantly after 25,000 write and erase cycles. As for the influence of the environmental temperature, it is described that the threshold voltage of the nonvolatile memory at 80 °C is decreased by only 0.1 V compared with the case of 40 °C.

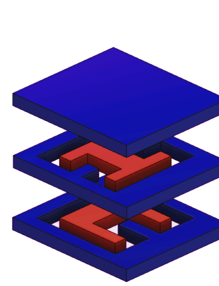

Fig. 1 3D structure of FiCC

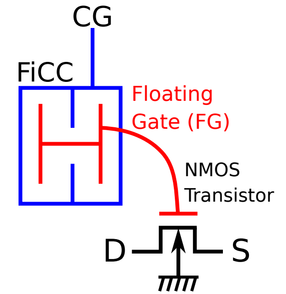

Fig. 2 Nonvolatile memory using FiCC

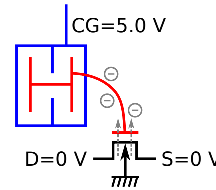

Fig. 3 Write operation

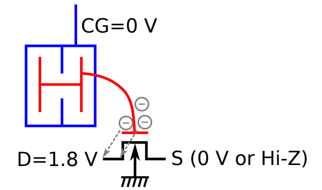

Fig. 4 Erase operation

3. Nonvolatile Storage Cells Using FiCC

3.1 D-latch for NV-SCM

The structure of the D-latch for NV-SCM (1-bit NV-SCM) is shown in Fig. 5. The 1-bit NV-SCM consists of the conventional volatile D-latch and the nonvolatile part highlighted in red. The nonvolatile part consists of a nonvolatile memory using FiCC and three NMOS transistors.

The 1-bit NV-SCM has four operation modes: latch, store data to the nonvolatile part, restore data from the nonvolatile part to the volatile latch, and data erase operation. The applied voltages to CK, DG_W, DG_R, CG, SG, and SL terminals, excluding the data restore operation, are shown in TABLE 1. During the latch operation, DG_W, DG_R, CG,

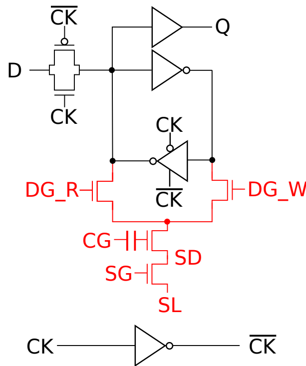

Fig. 5 1-bit NV-SCM

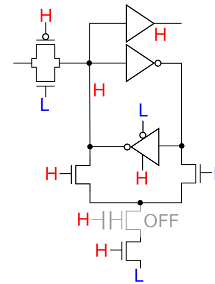

Fig. 6 Restore operation of NV-SCM (programmed)

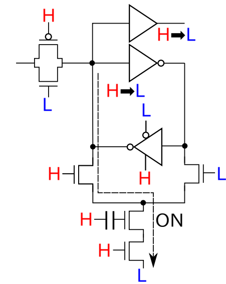

Fig. 7 Restore operation of NV-SCM (nonprogrammed)

Table 1 Operation mode of NV-SCM

	CK	DG_W	DG_R	CG	SG	SL
Latch	-	0 V	0 V	0 V	0 V	0 V
Store	0 V	1.8 V	0 V	5.0 V	0 V	0 V
Erase	-	0 V	0 V	0 V	1.8 V	1.8 V

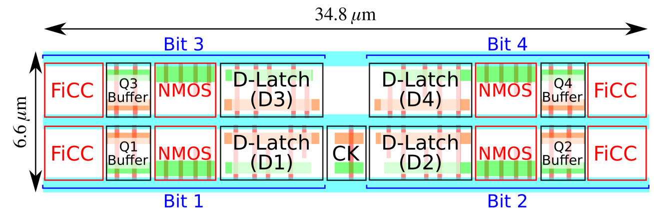

Fig. 8 Layout of the D-latch for the 4-bit NV-SCM

SG, and SL are all set to 0 V and then the D-latch for NV-SCM operates as a conventional D-latch. During the data store operation, DG_W = 1.8 V, CG = 5.0 V, CK = DG_R = SG = SL = 0 V, and data is stored to the nonvolatile memory using the FiCC. The amount of increase in the threshold voltage of the nonvolatile memory cell (NMOS transistor with the FiCC) by the data store operation is determined by the holding value of the D-latch. During the data erase operation, data is erased from the nonvolatile memory using the FiCC with DG_W = DG_R = CG = 0 V, SG = SL = 1.8 V. Electrons are pulled out from the FG by the voltage of 1.8 V−threshold voltage between the CG terminal and the SD node, since there is an NMOS transistor between the SD node and the SL terminal, which is turned on by the SG signal is applied. In the data restore operation, power is first turned on to the D-latch and then the D-latch stores 1 (high), followed by DG_R = CG = SG = 1.8 V, CK = DG_W = SL = 0 V. Thus, the data restore operation finishes within a few clock cycles. Figs. 6 and 7 show the behavior of the latch during the data restore operation when the threshold voltage of the nonvolatile memory cell is higher or lower than 1.8 V, respectively. When the threshold voltage of the nonvolatile memory cell is higher than 1.8 V, the NMOS transistor does not turn on even at CG = 1.8 V and the latch retention value remains high. When the threshold voltage is lower than 1.8 V, the NMOS transistor turns on, and then the latch retention value changes from high to low. Thus, depending on the threshold voltage of the nonvolatile memory cell, the high or low data is restored to the latch.

We designed the D-latch for 4-bit NV-SCM in a 180 nm CMOS process. The layout of the D-latch for the 4-bit NV-SCM in Fig. 8 consists of four D-latches described before. The black rectangles (Buffer, D-Latch, and CK) in Fig. 8 correspond to the black elements in Fig. 5, and the red rectangles (FiCC and NMOS) correspond to the red elements in Fig. 5. In the layout design of NV-SCM by logic synthesis and automatic placement and routing, the layout area of NV-SCM can be reduced by using the D-latch including 4-bit NV-SCM bit cells. Since the clock signal is common, there is only one clock inverter in the whole cell. DG_W, DG_R, CG, SG, and SL are short-circuited in the cell. The area of the D-latch for the 4-bit NV-SCM is 229.68 μm^2 (34.8 μm $\times$ 6.6 μm), with 74% area overhead due to the nonvolatility of the bit cell.

3.2 NV-FF

The structure of the NV-FF is shown in Fig. 9. The NV-FF is composed of the conventional volatile flip-flop and the nonvolatile section highlighted in red.

The NV-FF has four operation modes: flip-flop, store, restore, and erase operation. The applied voltages to CLK, DG_W, DG_R, CG, SG, SL, XS, and XR terminals besides the restore operation are shown in TABLE 2. In the flip-flop operation, DG_W, DG_R, CG, SG, and SL are all set to 0 V and then the NV-FF operates as a conventional flip-flop. In the store operation, DG_W = XS = XR = 1.8 V, CG = 5.0 V, CLK = DG_R = SG = SL = 0 V. In the erase operation, DG_W = DG_R = CG = 0 V, and SG = SL = 1.8 V. In the restore operation, power is first supplied to the flip-flop and then the control signals of the flip-flop is set to CLK = XS = 0 V, followed by DG_R = CG = SG = XS = XR = 1.8 V, CLK = DG_W = SL = 0 V. Figs. 10 and 11 show the behavior of the secondly latch in the restore operation when the threshold voltage of the nonvolatile memory cell is higher or lower than 1.8 V respectively. As the two figures show, high or low data is restored to the flip-flop depending on the threshold voltage of the nonvolatile memory cell.

We designed the layout of the 1-bit NV-FF using the 180 nm CMOS process technology. The layout of the 1-bit NV-FF is shown in Fig. 12. The layout size is 99.99

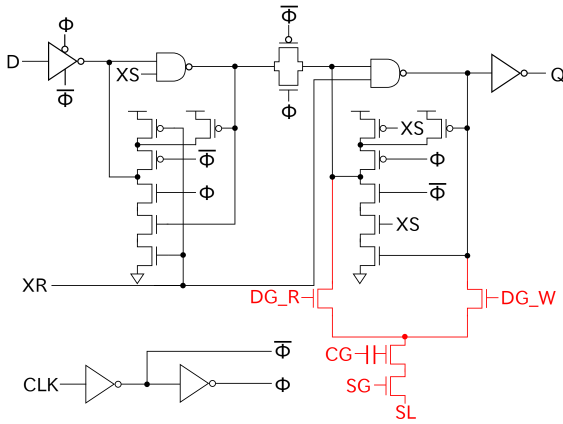

Fig. 9 Structure of NV-FF

Table 2 Operation mode of NV-FF

	CLK	DG_W	DG_R	CG
Flip-flop	-	0 V	0 V	0 V
Store	0 V	1.8 V	0 V	5.0 V
Erase	-	0 V	0 V	0 V
	SG	SL	XS	XR
Flip-flop	0 V	0 V	-	-
Store	0 V	0 V	1.8 V	1.8 V
Erase	1.8 V	1.8 V	-	-

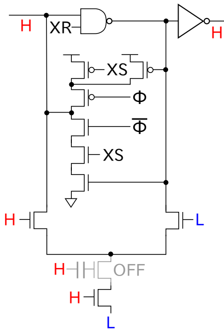

Fig. 10 Restore operation of NV-FF (programmed)

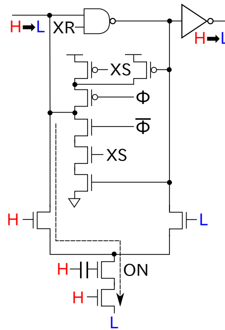

Fig. 11 Restore operation of NV-FF (nonprogrammed)

μm^2 (5.04 μm × 19.84 μm). The area overhead caused by nonvolatility of the flip-flop is 29%.

In order to compare the performance between FF and NV-FF, we performed a circuit simulation at 1.8 V, 27 °C, and 1 GHz using HSPICE. The netlist for this simulation includes parasitic resistance and capacitance extracted from the layout design. The simulation results are shown in TABLE 3. The CLK-to-Q delay and D-to-Q delay of the NV-FF are larger than the FF by 5.2% and 4.9%, respectively.

4. Measurement Results of NV-SCM and NV-FF

4.1 Macros on the Test Chip

We implemented the following macros on the test chip.

- 4-bit NV-SCM
- 16-word-8-bit NV-SCM
- 16-word-8-bit volatile SCM
- 1-bit NV-FF
- 16-bit nonvolatile counter

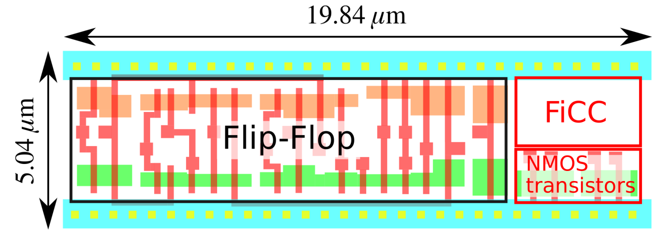

Fig. 12 Layout of the 1-bit NV-FF

Table 3 Performance comparison between FF and NV-FF

	Setup time	Hold time
FF	0.113 ns (1.0)	−0.0528 ns (1.0)
NV-FF	0.117 ns (1.035)	−0.0493 ns (0.9337)
	CLK-to-Q delay	D-to-Q delay
FF	0.524 ns (1.0)	0.637 ns (1.0)
NV-FF	0.551 ns (1.052)	0.668 ns (1.049)

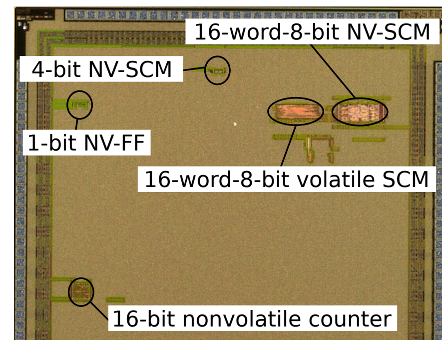

Fig. 13 Chip micrograph

Fig. 13 shows a chip micrograph. All macros are fabricated in the 180 nm CMOS process.

The 16-word-8-bit NV-SCM contains 16×2 4-bit NV-SCMs and the layout size is 0.0314 mm^2 (99.0 μm × 317.4 μm).

The 16-word-8-bit conventional volatile SCM is designed for comparison. The layout size is 0.0232 mm^2 (85.8 μm × 270.0 μm).

The 16-bit nonvolatile counter with the NV-FF as a bit cell is designed by a logic synthesis tool and an automatic placement-and-routing tool. The layout size is 0.006142 mm^2 (70.56 μm × 87.04 μm).

4.2 Measurement Results

All measurements were performed at room temperature.

4.2.1 NV-SCM

We confirmed that the latch, store, restore, and erase operations of the 4-bit NV-SCM were fully functional. 4-bit

NV-SCM can work up to 80 MHz in the latch and restore operation when the supply voltage is 1.8 V. The relationship between the store (write) time and the data retention time of the nonvolatile memory is shown in Fig. 14. Bit 3 had a shorter retention time than the other bits. When the voltage applied to the CG during the data restore operation is 1.8 V, the data retention time saturates to 35 minutes for the write time over 0.3 seconds. Based on this result, we changed the voltage applied to the CG during the restore operation to 1.4 V. The relationship between the store (write) time and the data retention time of the nonvolatile memory is shown in Fig. 15. In the case of 1.4 V, the data retention time of all bits was equivalent. The data retention time similarly saturates for the write time beyond 0.3 seconds, but the retention time successfully increased to 95 minutes.

The relationship between data retention time and threshold voltage of the nonvolatile memory is shown in Fig. 16. The red dashed line indicates the normal value of the threshold voltage of the nonvolatile memory. Writing to the nonvolatile memory increases the threshold voltage to about 3.0 V (at 0.3 seconds write time), and then it decreases to the normal value as time goes by. The data retention time is defined as the time until the threshold voltage of the nonvolatile memory is equal to the voltage applied to the CG during the restore operation. Therefore, the data retention time can be extended by lowering the voltage applied to the CG during the restore operation. This suggests that changing the voltage applied to the CG during the restore operation can shorten the time required to store (write) data to the nonvolatile memory using FiCC and extend its lifetime by suppressing the damage on the gate oxide of the NMOS transistor connected to the FiCC.

The retention time of the nonvolatile memory is much shorter than [27] because of these two reasons. First, the store (write) time to the nonvolatile memory is shorter. In [27], the write time is 5 seconds, but only 0.1 seconds in this measurement. When the write operation is over 1 second, the data is written to the nonvolatile memory even if the holding value of the latch is low. Therefore, the write time of the nonvolatile memories is limited to about 1 second. Second, the reading voltage of the nonvolatile memory is high. In [27], threshold voltage shift is observed around 0.5 V, whereas in this measurement, data is read out with 1.4 V.

We confirmed that the latch, store, restore, and erase operations of the 16-word-8-bit NV-SCM were also fully functional. The shmoo plot of the 16-word-8-bit SCM and NV-SCM is shown in Fig. 17. The dark green area shows the pass region for both NV-SCM and SCM, the light green area shows the additional pass region only for SCM, and the red area shows the fail region for both. The SCM and NV-SCM can operate up to 24 MHz and 21 MHz, respectively when the supply voltage is 1.8 V. This result indicates that there is a 12.5% operating speed overhead due to the nonvolatile part in the NV-SCM. Parasitic resistance and capacitance caused by the nonvolatile part decreases the operating speed. The retention time of the 16-word-8-bit NV-SCM is shown in Fig. 18. The voltage applied to the CG during the data

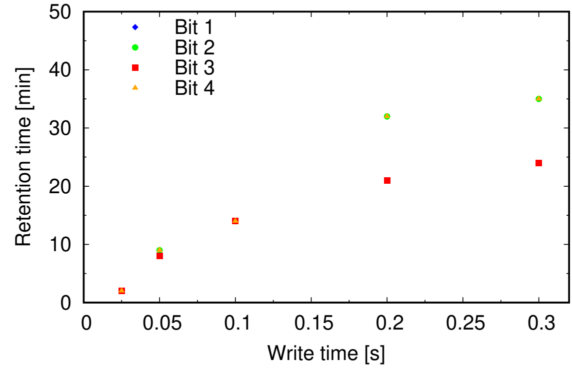

Fig. 14 Retention time of the nonvolatile memory (4-bit NV-SCM, CG=1.8 V)

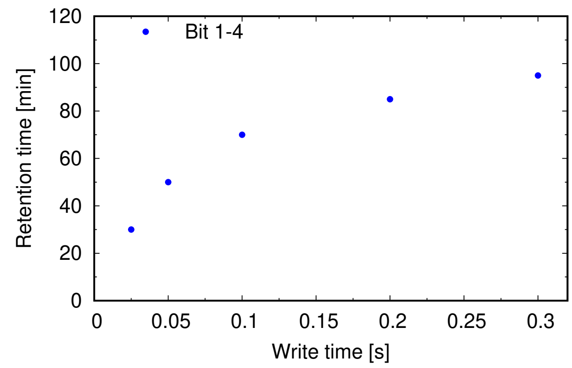

Fig. 15 Retention time of the nonvolatile memory (4-bit NV-SCM, CG=1.4 V, Retention time of all bits is the same value.)

restore operation is 1.4 V and write time is 0.05 seconds. The average of the data retention time is 258 minutes, and the standard deviation is 36 minutes (14%). Compared with the 4-bit NV-SCM, the data retention time differs bit by bit. The main reason can be explained that the variation of plasma-processing-induced damage (P^2ID) to the gate oxide of the NMOS transistor that consists of the nonvolatile memory due to the difference in the wire length of the CG. P^2ID to the gate oxide causes both leakage current increase and threshold voltage instability. In [32], the effect of the P^2ID on a transistor with its gate terminal connected to the metal-insulator-metal (MIM) capacitor which has the same structure as the nonvolatile memory is described. The gate oxide failure ratio from plasma damage depends on the ratio of the area of the capacitor and the area of the metal wire connected to the electrode which is not connected to the gate terminal. Therefore, it can be thought the data retention time varies due to differences in the gate oxide damage of the nonvolatile memory caused by the variation in the CG wire length.

4.2.2 NV-FF

We confirmed that the flip-flop, store, restore, and erase operations of the 1-bit NV-FF were fully functional. The 1-bit NV-FF can work up to 65 MHz in the flip-flop and restore

Fig. 16 Relationship between data retention time and threshold voltage of the nonvolatile memory

Fig. 17 Shmoo plot of the 16-word-8-bit SCM and NV-SCM

Fig. 18 Retention time of the nonvolatile memory (16-word-8-bit NV-SCM)

operations when the supply voltage is 1.8 V. The relationship between the store (write) time and the data retention time of the nonvolatile memory is shown in Fig. 19. When the voltage applied to the CG in the restore operation is 1.8 V and write time is 0.1 seconds, the retention time is 30 minutes. Based on this result, we changed the voltage applied to the CG in the restore operation is 1.4 V. In the case of 1.4 V, the retention time is successfully extended to 155 minutes at 0.1 seconds of writing time.

We confirmed that count, store, restore, and erase operations of the 16-bit counter were fully functional. The shmoo

Fig. 19 Retention time of the nonvolatile memory (1-bit NV-FF)

Fig. 20 Shmoo plot of the 16-bit counter

plot of the 16-bit counter is shown in Fig. 20. The 16-bit counter can work up to 29 MHz in the count and restore operations when the supply voltage is 1.8 V. The relationship between the store (write) time and the retention time of the nonvolatile memory measured by using lower 8-bit is shown in Fig. 21. The voltage applied to the CG in the restore operation is 1.4 V. Compared with the 1-bit NV-FF, the data retention time of the NV-FFs in the 16-bit counter became shorter and varied. The main reason can be explained that the variation of P^2ID to the gate oxide of the NMOS transistor that consists of the nonvolatile memory due to the difference in the wire length of the CG. Fig. 22 shows the relationship between the CG wire lengths and the data retention time at 0.25 seconds of writing time. The correlation coefficient between the CG wire length and the data retention time was −0.728, indicating a strong negative correlation. It is considered that as the CG wire length increases, the plasma damage to the gate oxide increases, and the data retention time becomes shorter. Therefore, the retention times of the NV-FFs in the 16-bit counter are predicted to be close to the retention time of the 1-bit NV-FF by shortening the CG wire lengths.

5. Performance Comparison of Sequential Circuits Using NV-SCM and NV-FF

We compare the performances of two sequential circuits. One is implemented with conventional storage cells, while

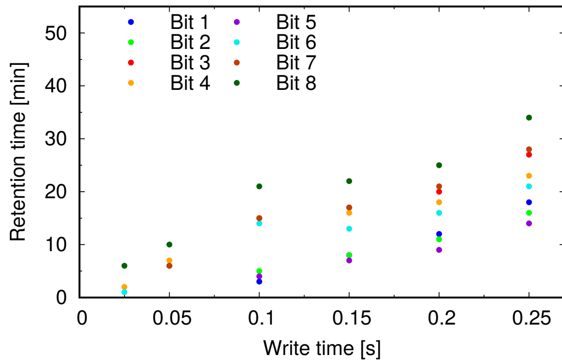

Fig. 21 Retention time of the nonvolatile memory (16-bit counter)

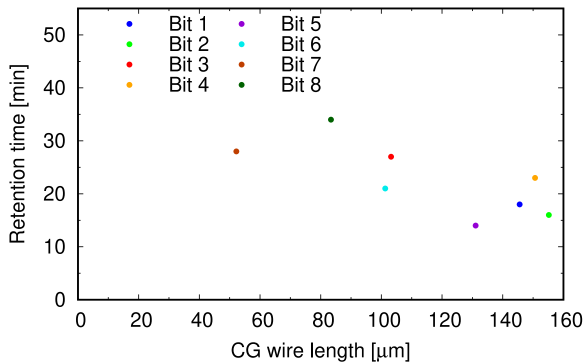

Fig. 22 Relationship between the CG wire length and the data retention time (write time=0.25 seconds)

the other is with nonvolatile storage cells.

5.1 Sequential Circuit Using Nonvolatile Storage Cells

The structure of a sequential circuit using SCM/NV-SCM and FF/NV-FF is shown in Fig. 23. This circuit imitates the structure of a RISC (reduced instruction set computer) processor. It consists of SCM/NV-SCM and MAC_RF. MAC_RF is composed of a multiply-accumulate unit (MAC) and a register file. The size of SCM/NV-SCM is the same that we confirmed to work in Section 4. To compare the energy consumption, we designed two implementations of this circuit, one with volatile SCM and FF (V-system) and the other with NV-SCM and NV-FF (NV-system). Due to the nonvolatility, temporal computed data can be kept even if the power supply is removed, and the system can instantly be restarted after power is turned on.

The operation flows of the sequential circuit is shown below.

- Read data from the 16-word-8-bit memory to the two FFs and feed them to MAC.
- Computation results are written to the register file.
- The above two cycles are executed in a pipeline manner and repeated.

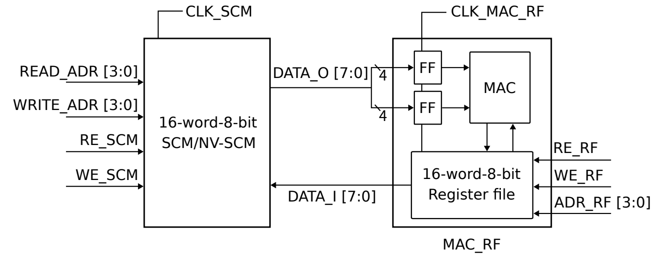

Fig. 23 Sequential circuit using SCM/NV-SCM and FF/NV-FF

- Finally, the data stored in the register file is written back to the 16-word-8-bit memory.

5.2 Comparison of Energy Consumption

To compare the energy consumption of V-system and NV-system as shown in Fig. 23, we performed circuit-level simulations at 1.8 V, 27 °C, and 10 MHz using HSPICE.

The energy consumption diagram of the V-system and the NV-system is shown in Fig. 24. The difference of energy consumption between V-system and NV-system in the normal operation is defined as E_{overhead} (=$P_{\text{overhead}} \times t_{\text{op}}$). The NV-system can be turned off in the standby operation, thus the energy consumption can be regarded as zero, while the V-system exhausts stand-by power. P_{sb} is defined as the amount of power consumption that can be reduced by the NV-system. Unlike the V-system, the NV-system completely turns off in the standby operation and consumes energy when it starts to operate again. Therefore, a certain amount of standby time (BET : Break Even Time) is required. BET is given by Eq. (1). E_{store} and E_{restore} are the energy consumed in the data store and restore operations, respectively. E_{store} is calculated by $I_{\text{store}} \times V_{\text{store}} \times t_{\text{store}}$, where I_{store} = 10 nA per bit [27] and V_{store} = 5.0 V, t_{store} = 200 ms. E_{restore} is calculated by $I_{\text{restore}} \times V_{\text{restore}} \times t_{\text{restore}}$.

$$BET = \frac{E_{\text{store}} + E_{\text{restore}} + P_{\text{overhead}} \times t_{\text{op}}}{P_{\text{sb}}}. \tag{1}$$

We derive the BET and the reduced energy. The power consumption of V-system and NV-system are shown in Table 4. The difference of power consumption between the V-system and the NV-system in the normal operation (P_{overhead}) is 1.29 μW (1.21%). We assume that a half of the number of the nonvolatile memory is written during the data store operation. The BET is shown in Eq. (2). The relationship between the ratio of standby/normal operation time and the reduced energy is shown in Fig. 25. At $t_{\text{sb}}/t_{\text{op}}$ = 500, the NV-system can reduce the energy consumption by 24.3% compared to the V-system. As the memory size in the systems increases, the energy decreases because the energy consumption in the standby operation of V-system (E_{sb}) becomes larger.

IoT devices that monitor the surrounding environment and send the data to a predefined IP address using Wi-Fi

Table 4 Power consumption of V-system and NV-system

	Normal operation	Standby operation
V-system	106.65 μW	72.03 nW
NV-system	107.94 μW	0

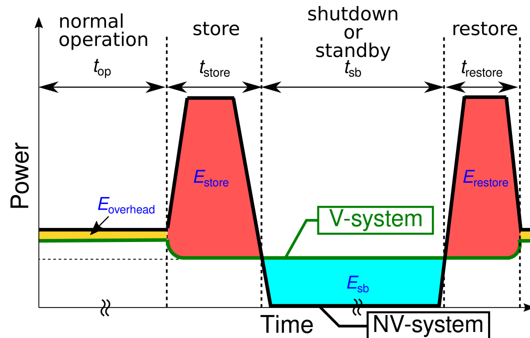

Fig. 24 Energy consumption diagram of V-system and NV-system

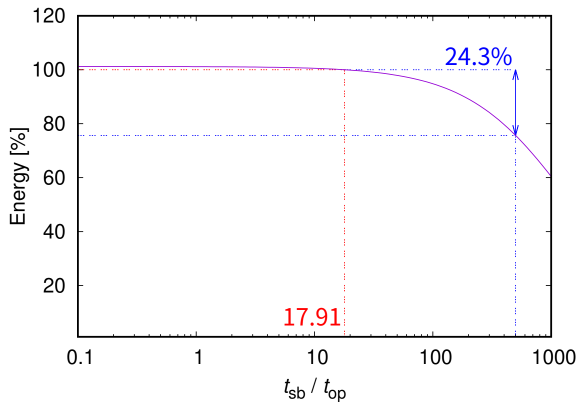

Fig. 25 Relationship between standby/normal operation time ratio and energy reduction

connectivity require about 10 seconds for a cycle of their operations and operating frequency is set to around 10 MHz to considerably reduce the power consumption [33]. Assume that the proposed NV-system is applied to the processors of the IoT devices. The normal operation time (for taking measurements and sending the data) is 10 seconds and the standby time is 83 minutes to fulfill the standby/normal operation time ratio is 500. We confirmed the retention time of 4-bit NV-SCM is 85 minutes (at 200 ms write time) and the average of the retention time of the 16-word-8-bit NV-SCM is 258 minutes (at 50 ms write time) in Section 4. Therefore, the proposed NV-system is adequate to use for the processors of IoT devices.

$$BET = 18.33\ \mathrm{s} + 17.91 \times \mathrm{t_{op}}. \quad (2)$$

6. Conclusion

In this paper, we describe the layout design and measurement results of an NV-SCM and an NV-FF with a nonvolatile memory using FiCC suitable for IoT processors with intermittent operations. NV-SCM and NV-FF are fabricated in a 180 nm CMOS process technology. The area overhead by nonvolatility of the bit cells are 74% and 29%, respectively. We confirmed full functionality of the NV-SCM and NV-FF at 80 MHz and 65 MHz, respectively on a fabricated chip in 180 nm. The data retention time is around 70 minutes (@NV-SCM) and 155 minutes (@NV-FF) when the write time to the nonvolatile memory is 0.1 seconds and the voltage applied to the CG in the restore operation is 1.4 V. The NV-system using the proposed NV-SCM and NV-FF can reduce the energy consumption by 24.3% compared to the V-system when hibernation/normal operation time ratio is 500 as shown in the simulation.

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Yuki Abe received the B.E. degree in Electronics from Kyoto Institute of Technology, Kyoto, Japan, in 2021, where he is currently pursuing the M.E. degree in Electronics. His current research is related to the nonvolatile memory for power gating and low voltage circuits.

Kazutoshi Kobayashi received his B.E., M.E. and Ph. D. in Electronic Engineering from Kyoto University, Japan in 1991, 1993, 1999, respectively. Starting as an Assistant Professor in 1993, he was promoted to associate professor in the Graduate School of Informatics, Kyoto University, and stayed in that position until 2009. For two years during this time, he acted as associate professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2009, he has been a professor at Kyoto Institute of Technology.
While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors, Bias Temperature Instability and Plasma Induced Damage) of current and future VLSIs. He started a research related to gate drivers for power transistors since 2013.
He was the recipient of the IEICE best paper award in 2009, the IRPS best poster award in 2013 and the IEICE Electronics Society award in 2021.

Jun Shiomi received the B.E. degree in electrical and electronics engineering, the M.E. degree in Informatics, and the Ph.D. degree in Informatics from Kyoto University, Kyoto, Japan, in 2014, 2016 and 2017, respectively. From 2016 to 2017, he was a Research Fellow of the Japan Society for the Promotion of Science. From December 2017 to March 2021, he was an Assistant Professor in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University, Japan. In April 2021, he joined Osaka University where he is currently an Associate Professor in the Graduate School of Information Science and Technology. His research interests include modeling and computer-aided design for low power and low voltage system-on-chips.

Hiroyuki Ochi received the B.E., M.E., and Ph.D degrees in Engineering from Kyoto University in 1989, 1991, and 1994, respectively. From 1994 to 2004, he was an Associate Professor with Hiroshima City University, and from 2004 to 2013, he was an Associate Professor with Kyoto University. Since 2013, he has been a Professor with the College of Information Science and Engineering, Ritsumeikan University. His research interests include reconfigurable architecture and low-power VLSI design. He is a member of IEEE, ACM, IEICE and IPSJ.