PAPER

Evaluation of Heavy-Ion-Induced Single Event Upset Cross Sections of a 65-nm Thin BOX FD-SOI Flip-Flops Composed of Stacked Inverters

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SUMMARY

Cross sections that cause single event upsets by heavy ions are sensitive to doping concentration in the source and drain regions, and the structure of the raised source and drain regions especially in FDSOI. Due to the parasitic bipolar effect (PBE), radiation-hardened flip flops with stacked transistors in FDSOI tend to have soft errors, which is consistent with measurement results by heavy-ion irradiation. Device-simulation results in this study show that the cross section is proportional to the silicon thickness of the raised layer and inversely proportional to the doping concentration in the drain. Increasing the doping concentration in the source and drain region enhance the Auger recombination of carriers there and suppresses the parasitic bipolar effect. PBE is also suppressed by decreasing the silicon thickness of the raised layer. C_{gg}-V_{gs} and I_{ds}-V_{gs} characteristics change smaller than soft error tolerance change. Soft error tolerance can be effectively optimized by using these two determinants with only a small impact on transistor characteristics.

key words: *single event effect, soft error, heavy ion irradiation, FDSOI, flip flop, device simulation.*

1. Introduction

Radiation-induced soft errors are significant concerns in medical devices, aerospace technologies, and high-performance super computers. Soft errors are particularly problematic for the continuous operation of super computers where hundreds of thousands of processors operating simultaneously [1]. Radiation-hardened designs tend to be more reliable since they are more resistant to soft errors and have small performance overhead. To improve the reliability, flip flops (FFs) or latches must be protected from soft errors [2], [3]. Redundant FFs are an effective design approach to mitigate soft errors, however they often incur a large area overhead and high-power dissipation. In addition, multiple node charge collection becomes a critical issue for redundant FFs in advanced technology nodes [4]–[6].

In devices with radiation-hardened technology, silicon on insulator (SOI) transistors have a smaller sensitive volume than bulk transistors, which is highly correlated with soft-error tolerance [7], [8]. SOI transistors have a buried oxide (BOX) layer inserted under the transistors that can block charge collection from a well by drift and funneling. Especially, fully-depleted SOI (FDSOI) technology adopts a thinner SOI layer for transistors and have a smaller sensitive volume than the partially-depleted SOI (PDSOI) technology. Radiation-induced current glitches of FDSOI transistors are fewer than those of bulk transistors. However, even the FD-SOI process does not mitigate the soft errors well enough to be used in the equipment under high total ionizing dose [9], [10]. This is because the floating body region in the transistor layer turns on parasitic bipolar transistors and this amplifies the charge collection induced by a radiation strike [11].

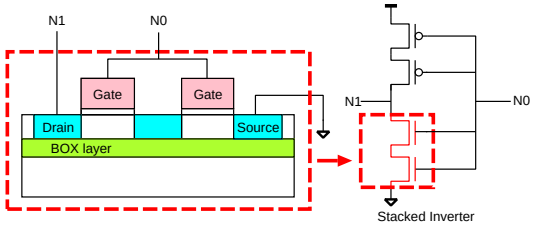

Fig. 1 Structure of the stacked inverter.

In this paper, the transistor stack which includes serially connected input transistors (Figure 1) is investigated. Stack transistors improve the soft error tolerance in FDSOI [12], [13]. Soft errors at the stacked latch in FDSOI only happen when both stacked transistors are simultaneously hit by a particle strike. Device models are ideal for investigating the sensitivity to soft errors because the device parameters or structures can be easily changed. If we can evaluate soft error tolerance before chip fabrication, it reduce time and cost. Therefore in this study, we used 3D device simulation where the device structure is created from the SPICE model of a 65 nm FDSOI Process Design Kit. Surface of the source and drain diffusion layers (the focus of this paper) is silicided to reduce parasitic resistance. When the silicide region reaches the boundary between the source and drain region and the channel, a Schottky contact is formed and this hampers current flow. The raised drain and source regions are formed by selective epitaxial growth of silicon to prevent the silicide region from reaching the channel as shown in Fig. 2. In this paper, we refer to the raised drain and source regions as the raised layer. The structure of the raised layer severely affects the amount of charge generated by a particle strike.

SEU cross section is the total of all the sensitive areas. In this paper, the sensitive areas of a standard flip-flop (FF)

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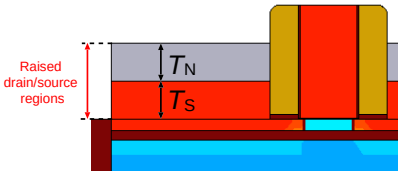


Fig. 2 Structure of raised layer, definition of thickness of silicon (T_S) and thickness of nickel silicide (T_N).

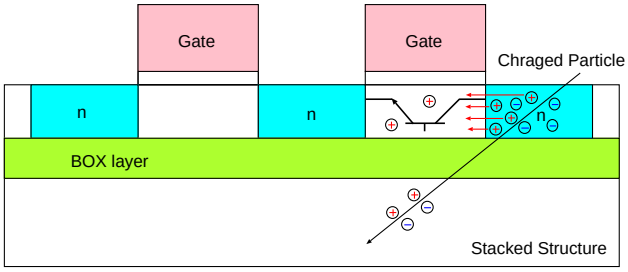


Fig. 3 Holes generated in the source and drain region are collected in the channel region and then the drain-body-source parasitic bipolar transistor turns on.

and a radiation-hardened FF based on a stacked inverter in a 65 nm FDSOI process [14] are estimated by device simulation. Then, the radiation hardness of the standard and stacked latches was measured by heavy-ion irradiation to confirm the simulation results.

This paper is organized as follows. Section 2 shows the device simulation results of sensitive areas in the 65 nm FDSOI process. In Section 3, the heavy-ion test results to FF are described in order to compare the simulation results with test results. Soft error mitigation techniques by controlling the doping concentration and the thickness of the raised layer is discussed in Section 4. Finally, we conclude this paper.

2. Evaluation of Sensitive Area in the 65 nm FDSOI Process by TCAD Simulations

In this section, the sensitive areas are evaluated using a commercial TCAD simulation tool, Synopsys Sentaurus (Version L-2016.03-SP2) in order to examine how soft errors occurs in a FDSOI process.

2.1 Soft Errors in FDSOI Process

In the bulk process, charge collection is the dominant cause of soft errors, while in the FDSOI process, the parasitic bipolar effect (PBE) is the dominant one [15]. PBE in NMOS arises due to an increase in hole density in the channel region. Fig. 3 shows how holes are generated in the diffusion region and collected to the channel region [16]. PBE turns on the parasitic bipolar transistor of source-channel-drain to cause a flip of memory storage cells such as an SRAM cell or a latch. In the FDSOI process, charges are collected only above the BOX layer. Charges generated in raised layer also cause a soft error.

The stacked structure in FDSOI is a good design to mitigate soft errors since it is difficult for the stacked transistors to be turned on simultaneously [13]. However, in the bulk process the charges generated in the well region is collected by both transistors. Therefore, the stacked structure is not effective at suppressing soft errors in the bulk processes.

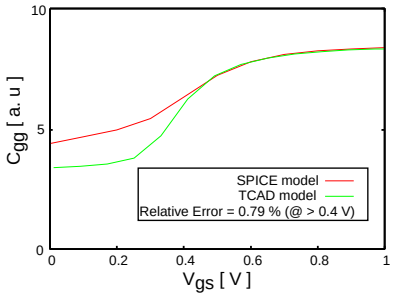
2.2 Simulation Setup

We use 3D NMOS models calibrated to match the SPICE models which are extracted from the real devices as explained in [17]. The TCAD model is created from the cross-sectional view of the chip. After that, some parameters such as the impurity density are adjusted to match the electrical characteristics of device models to those of the SPICE model. The capacitance-voltage (C_{gg}-V_{gs}) and current-voltage (I_{ds}-V_{gs}) of the transistor are shown in Fig. 4. Characteristics on TCAD simulations were optimized to decrease the relative error between TCAD simulations and SPICE simulation to less than 6.4% in the region of $|V_{gs}| > 0.4$ V.

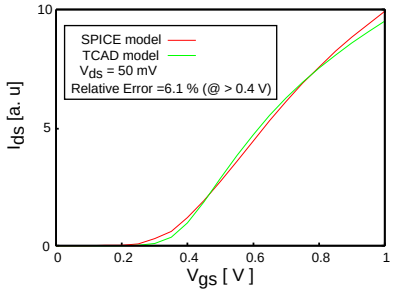
Two 3D models for TCAD simulations were constructed to evaluate the cross sections of FFs in the 65 nm FDSOI. Fig. 5 shows cross-sectional views of the 3D models and the schematic diagrams of a standard clocked latch and a radiation-hardened latch used in device- and transistor-level mixed-mode simulations. In both latches, one of stacked transistors turns on to keep a stored value. In the standard clocked latch one of stacked transistors turns off, while in the radiation-hardened latch both transistors of stacked transistors turn off. The radiation-hardened latch consists of three stacked inverters. The stacked structure drastically suppresses PBE caused by a radiation strike [18].

The supply voltage is fixed to 0.8 V. A normal-incident heavy ion with linear energy transfer (LET) of 15.8 MeV-cm^2/mg strikes the 3D-model transistor. 15.8MeV-cm^2/mg is simulating Ar used in actual measurement. Heavy ion strikes are modeled as charge generation with a Gaussian distribution along the ion track radius. Heavy ions are irradiated on a standard clocked latch and a radiation-hardened latch with the stacked structure in the 65 nm FDSOI process. In order to evaluate the sensitive areas, heavy ions are irradiated at every 20 nm grid as shown in Fig. 6. Simulations are performed with 50 nm track radius referencing [19]. 50 nm is 2.5 times wider than the grid width, so it is easier to evaluate the sensitive areas. Even with heavy ion irradiation of 50 nm track radius, it influences the volume of a cylinder with the radius over μm by the drift and diffusion of the charges. The drift and diffusion depend on the shape and the impurity density of the drain and source regions. The shape and area of sensitive areas are obtained from each ion strike similar to heavy-ion microbeam test [20]. In the initial state, CLK is 0 and the states of the transistors in the 3D model are shown in Fig. 5. Initially, the output node is 1. If the output node becomes 0 after heavy ion irradiation, it is considered that a soft error has occurred.

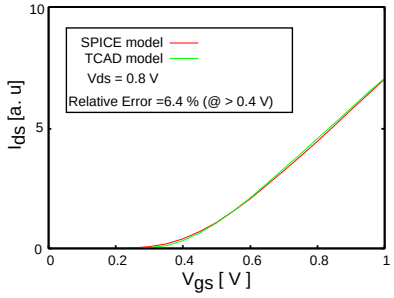
In this simulation, the following physical models were used. Mobility (Doping Dependence, High Field Satura-



(a) C_{gg}-V_{gs}



(b) I_{ds}-V_{gs} at V_{ds} = 50 mV.



(c) I_{ds}-V_{gs} at V_{ds} = 0.8 V

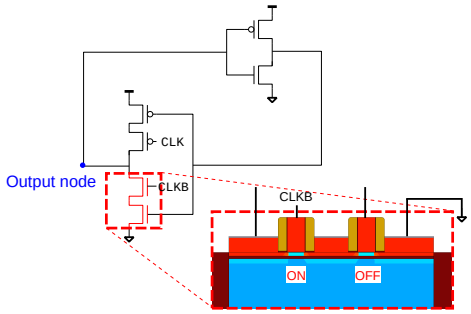
Fig. 4 (a) Simulated C_{gg}-V_{gs} characteristics at V_{ds} = 0 V. (b) Simulated I_{ds}-V_{gs} characteristics at V_{ds} = 50 mV. (c) Simulated I_{ds}-V_{gs} characteristics at V_{ds} = 0.8 V. Characteristics on TCAD simulations are optimized to decrease the relative error between TCAD simulations and SPICE simulation to less than 6.4% in region of $|V_{gs}| > 0.4$ V.

tion, Enormal), Fermi, Effective Intrinsic Density (Old Slotboom), Recombination (Shockley Read Hall, Auger).

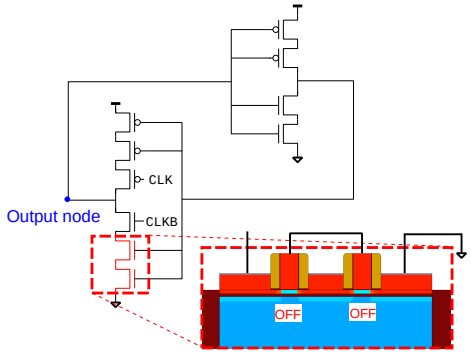
2.3 Simulation Results

Figure 7 shows the sensitive areas caused by a heavy ion from the normal angle with LET of 15.8 MeV-cm^2/mg. The sensitive area of the standard clocked latch covers the channel region and almost the entire drain region. Single event upsets (SEUs) also arise in the stacked clocked latch even for normal incidence irradiation. It is hard for particles from the normal incident to generate charge that affect both stacked transistors. Thus the sensitive area in the stacked clocked latch is mainly distributed in the source and drain region between two stacked transistors and does not fully cover the channel region.

In order to assess the error mechanism in the FDSOI process, hole density generated by a heavy ion strike was examined through device simulation. The generated holes



(a) Standard clocked latch



(b) Radiation hardened latch with stacked structure

Fig. 5 Schematic diagrams with the cross-sectional view of 3D models used for mixed-mode simulations. (a) Standard clocked latch, (b) Radiation-hard stacked clocked latch.

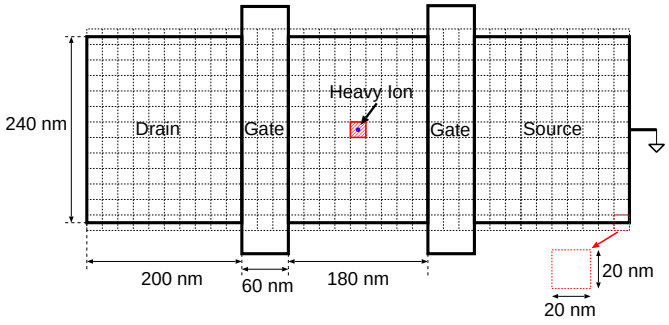


Fig. 6 Simulation setup to evaluate sensitive areas induced by a heavy ion with LET of 15.8 MeV-cm^2/mg. Radiation particles strike at the center of each grid.

elevate well potential and then activate the parasitic bipolar transistor. Fig. 8 shows the hole density variation in the SOI layer of the stacked clocked latch after a heavy ion strike. At 0 ps, a heavy ion incident occurs at the center of the two stacked NMOS transistors. As can be seen from the figure, most holes stay within 0.1 μm from the incident point at 10 ps. Then holes are diffused to the channel regions at 30 ps and 50 ps. In either state, the diffused hole concentrations in channel region seem to be relatively low due to the built-in potential between the channel and the source/drain regions. However, they are large enough to trigger the PBE. Both parasitic bipolar transistors in the stacked transistors simultaneously turn on when the hole concentrations reach

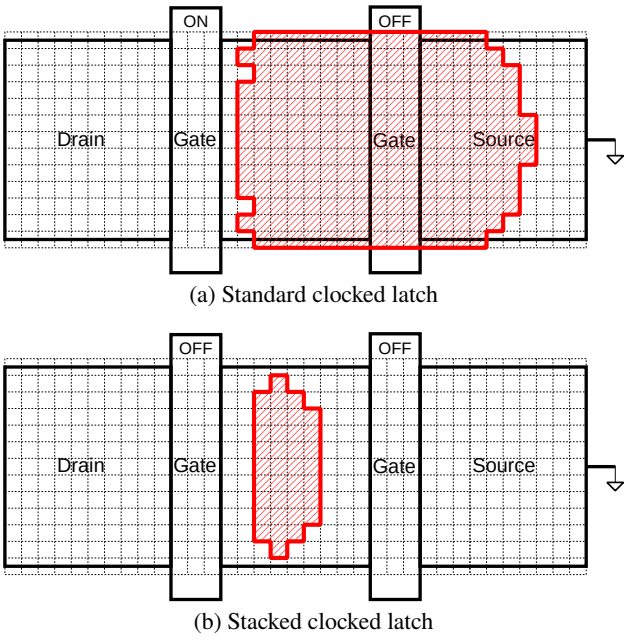


Fig. 7 Shape of sensitive areas in (a) Standard clocked latch (b) Stacked clocked latch by heavy ions with LET of 15.8 MeV-cm^2/mg.

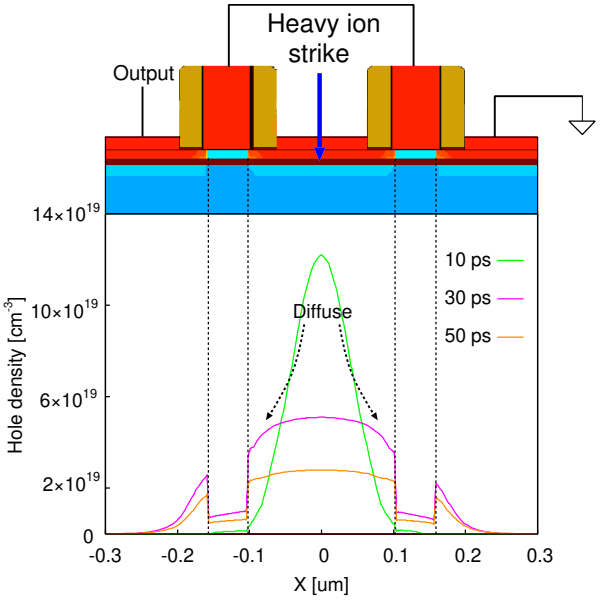


Fig. 8 Simulated transient distribution of holes in the body layer of stacked clocked latch when a heavy ion with LET of 15.8 MeV-cm^2/mg hit at the center of the stacked transistors at 0 ps.

the critical value and then the PBE can flip the stored values. These simulation results show that the hole diffusion in the drain region between the stacked transistors affects the soft error tolerance in the FDSOI process.

3. Soft Error Rates on FDSOI Process by Heavy Ion Test

Soft error rates (SERs) of the standard FF and the radiation-hardened FF with the stack structure were measured to obtain their sensitive areas by accelerated tests; results from the simulation were compared with actual measurements.

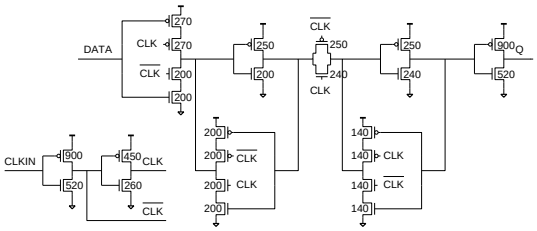


Fig. 9 Schematic diagram of a standard transmission gate FF (TGFF).

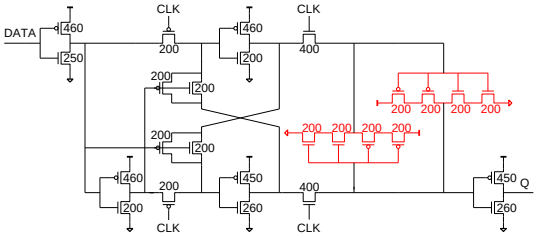


Fig. 10 Schematic diagram of the adaptive-coupling FF with stacked structure.

3.1 Test Chip Structure

To measure SERs by heavy ion tests, we implemented the standard transmission gate FF (TGFF) and the adaptive-coupling FF (ACFF) with the stacked structure named AC_SS FF [21]. Figures 9 and 10 show the schematic diagrams of TGFF and AC_SS FF, respectively. Slave latches of AC_SS FF are constructed by two stacked inverters. Test chips were fabricated in a 65 nm thin BOX FDSOI process and includes 23,976 TGFFs and 41,760 AC_SS FFs. The gate length of all the transistors are 60 nm and the width of the transistors are also shown in figures 9 and 10. The thicknesses of the BOX and SOI layers are 10 and 12 nm respectively.

3.2 Experimental Setup and Results

Heavy-ion tests were carried out at the National Institute for Quantum and Radiological Science and Technology (QST), Japan. All TGFFs and AC_SS FFs are tested in static mode and the supply voltage is fixed to 0.8 V. Ne, Ar and Kr ions hit the chip from a normal angle sequentially. Table 1 shows the specification of the heavy ions at QST. Although the heavy ions are attenuated while passing through the wiring layer, the wiring layer of the chip used in test chip is much thinner than the ranges of the incident ions. Thus, the wiring layer does not affect the attenuation of the heavy ions.

Here, soft error tolerance is evaluated by cross section (CS). CS is equal to an area of upsets when a particle passes a storage cell [22]. Equation (1) shows how to calculate CS. The smaller the CS becomes, the higher the soft error tolerance becomes.

Table 1 Specifications of heavy ions at QST.

Ion	Energy [MeV]	LET [MeV-cm^2/mg]	Range [μm]
$^{20}Ne^{4+}$	75	6.5	38.9
$^{40}Ar^{8+}$	150	15.8	36.1
$^{84}Kr^{17+}$	322	40.3	37.3

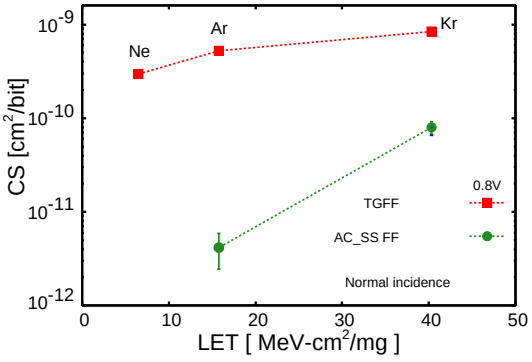


Fig. 11 Experimental results of sensitive areas of TGFF and AC_SS FF according to LET.

$$\mathrm{CS\ [cm^2/bit]} = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \times N_{\mathrm{FF}}} \tag{1}$$

Figure 11 shows the experimental results of the sensitive areas with respect to LET when all FFs stored 0 and the clock signal was fixed at 0. The CS of AC_SS FF is smaller than that of TGFF. However, there are still some SEUs in AC_SS FF with the stacked structure, which is consistent with the simulation results.

4. Efficient Soft-Error Mitigation Technique for FDSOI Process

In this section, we discuss how to optimize the fabrication process to enhance soft-errors tolerance for FDSOI using the stacked structure. In FDSOI NMOS, soft errors are caused by PBE triggered by the hole diffusion from the drain region as already mentioned in Sect. 2. To enhance soft error tolerance, doping concentration in the source and drain region is a key parameter. Higher concentration accelerates the Auger recombination that promotes carrier disappearance. The probability of the Auger recombination (R_{Aug}) depends on the carrier density from Eq. (2) [23].

$$R_{\mathrm{Aug}} = \begin{cases} \mathrm{B}n^2p & (n > p) \\ \mathrm{B}p^2n & (p > n) \end{cases} \tag{2}$$

Where B is the Auger coefficient, n is the electron density, and p is the hole density. If holes disappear before reaching the channel region, the soft error tolerance is improved. If the impurity of the drain and source regions is doped over 5×10^{20} cm^{-3}, clustering phenomenon occurs in which multiple dopants precipitate and become inactive. The upper limit to avoid this phenomenon is approximately 5×10^{20} cm^{-3}. If the impurity density is less than 1×10^{20} cm^{-3}, it prevents a high quality ohmic contact in the source and drain region but the Schottky contact component begins to appear and the contact resistance increases. Doping concentration of the drain and source regions is changed from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}.

Table 2 Sensitive areas of the standard latch according to doping concentration and the thickness of silicon in the raised layer

Doping concentration [cm^{-3}]	Sensitive area [cm^2/ion]		
	T_S = 50 nm	T_S = 60 nm	T_S = 70 nm
1×10^{20}	7.40×10^{-10}	8.12×10^{-10}	8.56×10^{-10}
3×10^{20}	7.08×10^{-10}	7.68×10^{-10}	8.00×10^{-10}
5×10^{20}	6.48×10^{-10}	6.64×10^{-10}	6.72×10^{-10}

Table 3 Sensitive areas of the stacked latch according to doping concentration and the thickness of silicon in the raised layer

Doping concentration [cm^{-3}]	Sensitive area [cm^2/ion]		
	T_S = 50 nm	T_S = 60 nm	T_S = 70 nm
1×10^{20}	0.20×10^{-10}	0.84×10^{-10}	1.44×10^{-10}
3×10^{20}	0	0.28×10^{-10}	0.64×10^{-10}
5×10^{20}	0	0	0

The shape of the raised layer also affects soft error tolerance. The raised layer is composed of silicon and silicide. Fig. 2 shows a cross-sectional view. The thickness of the silicon and the silicide are defined as T_S and T_N respectively. In FDSOI, charge generated above the BOX layer becomes a source of soft error. Thinning silicon in the raised layer lowers the amount of generated charge. We assume that nickel silicide is used as silicide, T_N is fixed to 5 nm and T_S is assigned to 50, 60, and 70 nm. Soft error does not occur in the stacked clocked latch when T_S is less than 40 nm.

The resistance of the source and drain region is inversely proportional to the impurity density meaning it becomes smaller as T_N becomes thicker and also as T_S becomes thinner [24].

4.1 Results of Standard Clocked Latch

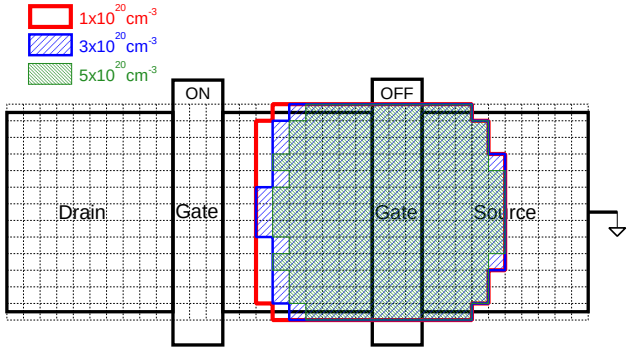
Figure 12 and Table 2 show the device simulation results of the sensitive areas of the standard clocked latch. The sensitive area decreases when the doping concentration of the source and drain region increases and the thickness of the silicon in the raised layer decreases.

When the doping concentration is increased from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}, the sensitive area decreases by at least 12.4%. When the silicon thickness is decreases from 70 nm to 50 nm, the sensitive area decreases at least 3.6%. The doping concentration and the silicon thickness in the raised layer impact the soft error tolerance.

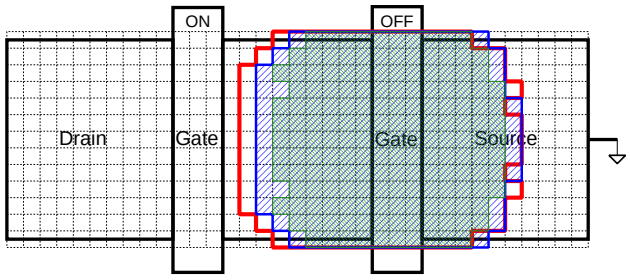
4.2 Results of Stacked Clocked Latch

Figure 13 and Table 3 show the device simulation results of the sensitive areas of the stacked clocked latch. The results are similar to those of the standard clocked latch; the sensitive area decreases with an increase in the doping concentration and thinning silicon.

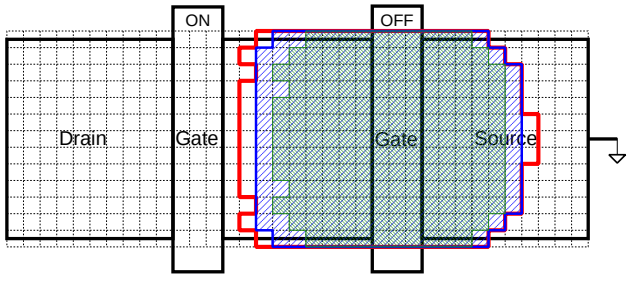
When the doping concentration is increased from 1×10^{20} cm^{-3} to 3×10^{20} cm^{-3}, the sensitive area changes



(a) T_S = 50 nm - standard clocked latch

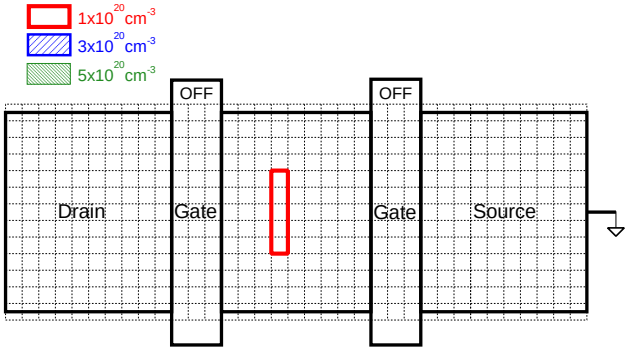


(b) T_S = 60 nm - standard clocked latch

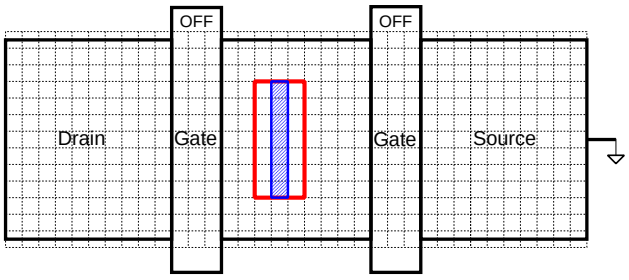


(c) T_S = 70 nm - standard clocked latch

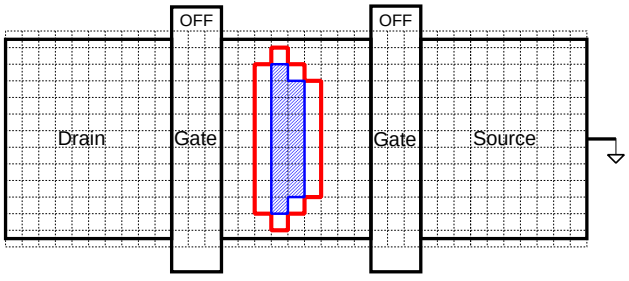
Fig. 12 Simulation results of sensitive areas according to the impurity density on the drain regions thickness silicon in raised layer.



(a) T_S = 50 nm - stacked clocked latch



(b) T_S = 60 nm - stacked clocked latch



(c) T_S = 70 nm - stacked clocked latch

Fig. 13 Simulation results of sensitive areas according to the impurity density on the drain regions thickness silicon in raised layer. when the doping concentration is 5×10^{20}, the sensitive area is 0 cm^2/ion.

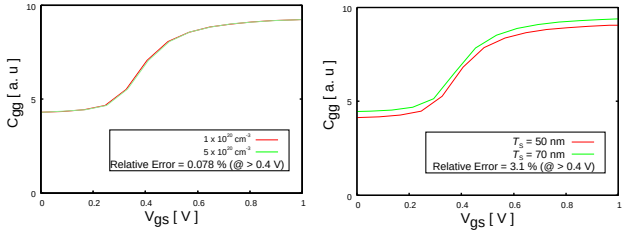
from 0.20×10^{-10} cm^2/ion to 0 cm^2/ion at T_S = 50 nm. At T_S = 60 nm and 70 nm, the sensitive area decreases by 66.7% and by 55.6% respectively. At all the silicon thickness, the sensitive area is 0 cm^2/ion when the doping concentration becomes 5×10^{20}. When the silicon thickness is decreases from 70 nm to 50 nm, the sensitive area decreases at least 86.1%.

When T_S was changed from 70 nm to 50 nm, the C_{gg}-V_{gs} curve changed up to 5%, and the I_{ds}-V_{gs} curve changed within 0.4%. When the doping concentration of the source and drain region is increased from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}, the C_{gg}-V_{gs} curve is changed within 2%, and the I_{ds}-V_{gs} curve differs within 0.1%. The simulation results show that the stacked structure with 5×10^{20} cm^{-3} doping concentration in the source and drain region eliminates soft errors with almost the same transistor performance as 1×10^{20} cm^{-3}. The soft error rate is more influenced by doping concentration and silicon thickness in the stacked clocked latch than in the standard clocked latch. Both of the doping concentration and the silicon thickness in the raised layer greatly affect the rate of soft error tolerance similarly in the stacked structure and the standard clocked latch.

4.3 Impact on Static Characteristics

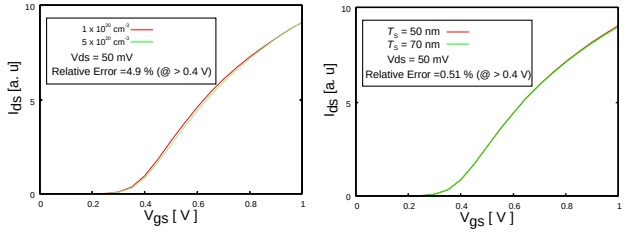
Figure 14 shows the static characteristics resulting from changing the doping concentration and the silicon thickness of the raised drain and source regions. The silicon thickness is fixed at 60 nm when the doping concentration is changed; when the silicon thickness is changed the doping concentration is fixed at 2×10^{20} cm^{-3}.

When the doping concentration is increased from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}, the static characteristics changes within 3.1%. At this time, the sensitive area of the standard latch changes by 18.2%. When changing the silicon thickness from 50 nm to 70 nm, the static characteristics and the sensitive area of the standard latch changes



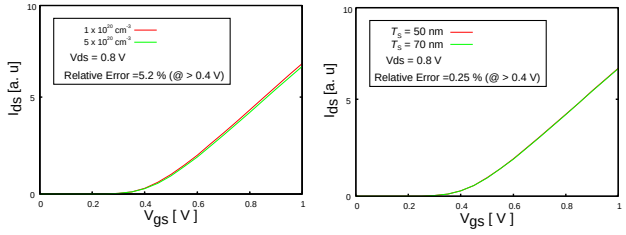
Doping concentration　　Silicon thickness

(a) C_{gg}-V_{gs}



Doping concentration　　Silicon thickness

(b) I_{ds}-V_{gs} at V_{ds} = 50 mV



Doping concentration　　Silicon thickness

(c) I_{ds}-V_{gs} at V_{ds} = 0.8 V

Fig. 14 (a) Simulated C_{gg}-V_{gs} characteristics at V_{ds} = 0 V. (b) Simulated I_{ds}-V_{gs} characteristics at V_{ds} = 50 mV. (c) Simulated I_{ds}-V_{gs} characteristics at V_{ds} = 0.8 V.

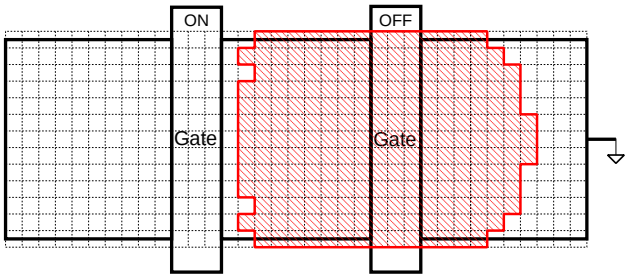
within 5.2% and 13.0% respectively. The sensitive area of the stacked latch is much more sensitive to the silicon thickness and doping concentration than the standard latch. These results show that a change in silicon thickness and doping concentration increases sensitive area by 14.8% or more even though the static characteristics changes by 5.2% at most.

4.4 Impact on Distance Between Two Gates

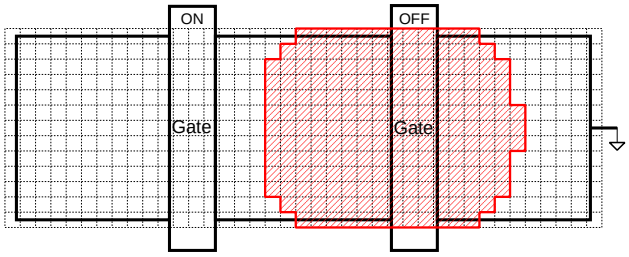
In the previous section, the simulation is performed 180 nm the gate-to-gate distance (D_{gg}), which is the minimum D_{gg} in the 65 nm FDSOI design process. Here D_{gg} is increased to 230 nm 280 nm to evaluate sensitive area at wider distances between series-connected transistors. Table 4 and Figures 15, 16 show the device simulation results of the sensitive areas according to D_{gg} . The sensitive area of the standard latch covers the channel region and almost the entire drain region. Even if D_{gg} changes from 180 nm to 280 nm, sensitive area changes only by 0.9%. This is considered to be an error due to the simulation accuracy. However the sensitive area in the stacked one decreases as D_{gg} become wider. When the D_{gg} is 280 nm, the sensitive area disappears. In the standard latch, soft error occurs by the PBE only in the

Table 4 Sensitive areas of the standard and stacked latch according to gate-to-gate distance.

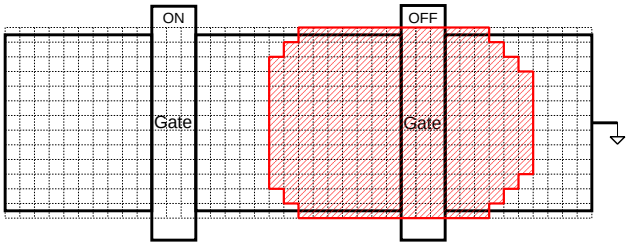
D_{gg} [nm]	Sensitive area [cm^2/ion]	
	Standard Latch	Stacked Latch
180	8.56×10^{-10}	1.44×10^{-10}
230	8.48×10^{-10}	0.28×10^{-10}
280	8.64×10^{-10}	0



(a) D_{gg} = 180 nm - standard clocked latch



(b) D_{gg} = 230 nm - standard clocked latch



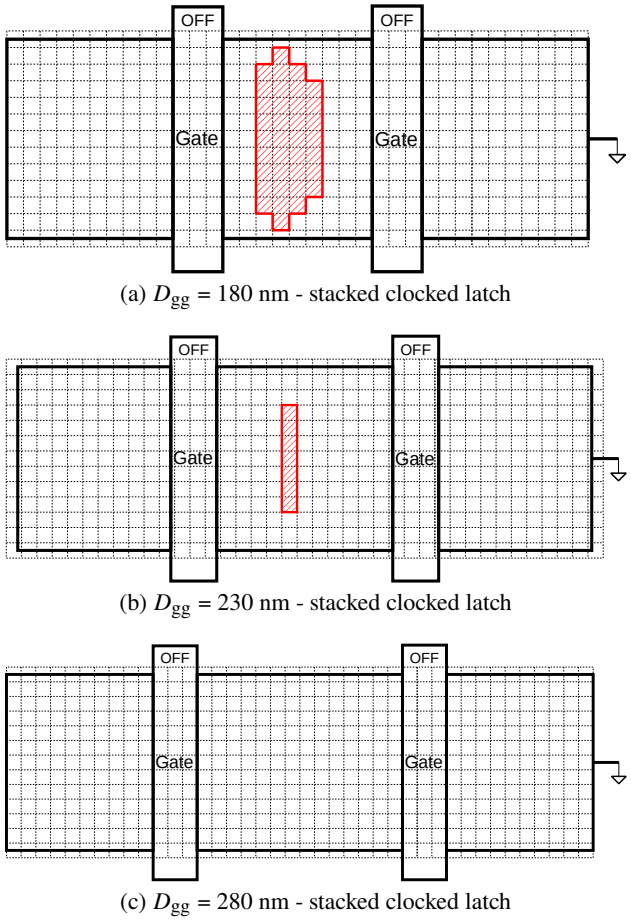
(c) D_{gg} = 280 nm - standard clocked latch

Fig. 15 Simulation results of sensitive areas of the standard latch according gate-to-gate distance.

off-state gate. The PBE must turn on both of the stacked transistors in order to flip the latch. As D_{gg} become wider, more charges generated by heavy ions recombine and disappear before reaching the body region. Therefore, the PBE become unlikely to occur and soft error tolerance improves. D_{gg} seems to affect soft error tolerance in the stacked latch, but not to affect in the standard latch. Wider D_{gg} is effective to improve the soft error tolerance in the stacked structure, but enlarges are and reduces performance.

5. Conclusion

Sensitive areas of a standard flip-flop (FF) and a radiation-hardened FF with the stacked structure in a 65 nm FDSOI process were investigated by device simulation. This was



(a) D_{gg} = 180 nm - stacked clocked latch

(b) D_{gg} = 230 nm - stacked clocked latch

(c) D_{gg} = 280 nm - stacked clocked latch

Fig. 16 Simulation results of sensitive areas of the standard latch according gate-to-gate distance. when the D_{gg} is 280 nm, the sensitive area is 0 cm^2/ion.

done through the process recipes such as doping concentration and the structure of the raised drain and source layers. The BOX layer prevents the generated carriers in the well from being collected by the transistors. Generally, a stacked FF is relatively resistant to soft errors because it is difficult to simultaneously turn on two stacked transistors by a particle strike. However, simulations in this study reveals that it is possible to turn on both stacked transistors by a heavy-ion strike in the FDSOI process. It is because the heavy-ion-induced holes in the drain region are diffused to the channel and this turns on the parasitic bipolar transistor between the drain and source.

In the stacked FDSOI structure, soft error rates become lower by the increasing doping concentration in the drain regions. Increasing the doping concentration in the source and drain region enhance the Auger recombination of carriers there and suppresses the parasitic bipolar effect (PBE). PBE is also suppressed by decreasing the silicon thickness of the raised layer. Simulation results show the sensitive area of the stacked FF is reduced by 55.6% or more when the doping concentration in the drain regions is increased from 1×10^{20} cm^{-3} to 3×10^{20} cm^{-3}. When the doping concentration in drain regions becomes 5×10^{20} cm^{-3}, the sensitive area disappears. C_{gg}-V_{gs} and I_{ds}-V_{gs} characteristics change by 5.2% or less. Soft error tolerance can be effectively optimized by using these two determinants with only a small impact on transistor characteristics.

Acknowledgment

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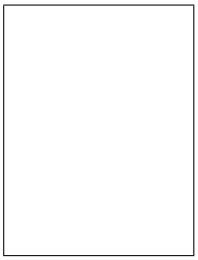

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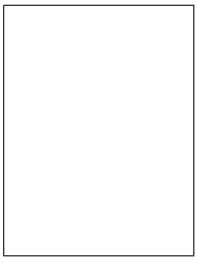

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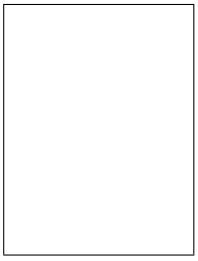

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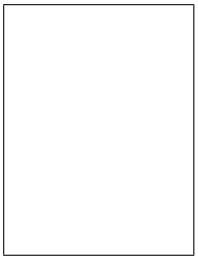

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While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors and Bias Temperature Instability) of current and future VLSIs.
He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.