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A Resource-shared VLIW Processor for Low-power On-chip Multiprocessing in the Nanometer Era

Kazutoshi KOBAYASHI[†a)], *Member*, **Masao ARAMOTO**[†*b)], *Nonmember*, *and* **Hidetoshi ONODERA**[†c)], *Member*

SUMMARY We propose a low-power resource-shared VLIW processor (RSVP) for future leaky nanometer process technologies. It consists of several single-way independent processor units (IPUs) that share parallel processor resources. Each IPU works as a variable-way VLIW processor sharing the parallel resources according to priorities of given tasks. RSVP allocates shared parallel resources to the IPUs cycle by cycle. It can minimize the number of NOPs that is wasting power. The performance per power (P^3) of a 4-parallel 4-way RSVP that corresponds to four 4way VLIWs is 3.7% better than a conventional 4-parallel 4-way VLIW multiprocessor in the current 90nm process. We estimate that the RSVP achieves 36% less leakage power and 28% better P^3 in the future 25nm process. We have fabricated an RSVP test chip that contains two IPU and a shared resource equivalent to two 2way VLIWs in a 180nm process. It is functional at 100MHz clock speed and its power is 130mW.

key words: *Parallel Processing, VLIW, SMT, Low Power, Nanometer, Leakage Power*

1. Introduction

In this paper, we propose a resource-shared VLIW processor (RSVP) for efficient on-chip multiprocessing. The RSVP architecture is based on the simultaneous multithreading technology (SMT) [1]. Conventional SMT architectures tend to be applied to high-performance microprocessors. We propose the RSVP architecture for embedded fields, in which area and power are limited.

The RSVP consists of several single-way independent processing Units (IPUs) that share parallel resources. Each IPU works as a variable-way VLIW processor with shared processing elements. In the conventional parallel processors, most of hardware resources for parallel processing are idle or execute NOPs almost all the time since the average IPC (instruction per clock) is much smaller than the prepared number of parallel resources. If more hardwares are prepared, the instantaneous IPC can be increased. But they are idle and wasting power at the rest of the time.

Wasting power can be minimized with the well-known power saving techniques. The gated-clock and

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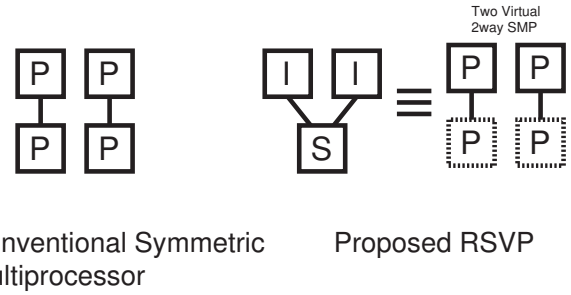
[†]Graduate School of Informatics, Kyoto University
[*]Presently, the author is with Renesas Technology
a) E-mail: kobayasi@i.kyoto-u.ac.jp
b) E-mail: masao@vlsi.kuee.kyoto-u.ac.jp
c) E-mail: onodera@i.kyoto-u.ac.jp



I	Independent Processor UNIT (IPU)
S	Shared Pipelined Processing Element (SPPE)

Fig. 1 Architectures of the proposed resource-shared VLIW processor (RSVP).

VT-CMOS technique is effective for active-power saving, while MT-CMOS reduces leakage power. The upcoming nanometer technology, however, makes these conventional power saving technologies insufficient because of leaky transistors. Leakage current is proportional to the chip area. Hardware solutions accelerate given tasks considerably when they have explicit data-level parallelism. But such kind of tasks (applications) are limited to multimedia ones. Software solutions on processors deal with any kind of tasks from highly-parallel multimedia ones to serial ones. But processors occupies large area and their performance is relatively slower than dedicated hardwares. Therefore, it is indispensable to reduce the area of processors for low-power on-chip multiprocessing. The RSVP increases the performance per area, which reduces leakage current dominant in the nanometer era.

This paper is organized as follows. Section 2 gives the architecture of the proposed resource-shared VLIW processor (RSVP). In Sect. 3, we evaluate efficiency of the RSVP in terms of performance, area and power compared with the conventional VLIW processors. Section 4 forecasts the total dissipating power including active and leakage power in the future nanometer era. We have fabricated an RSVP test chip in a 180nm process, which is explained in Sect. 5. We conclude this paper in Section 6.

2. Architecture and Behavior of RSVP

Fig. 1 shows the architecture of the resource-shared VLIW processor, RSVP. The left side shows a con-

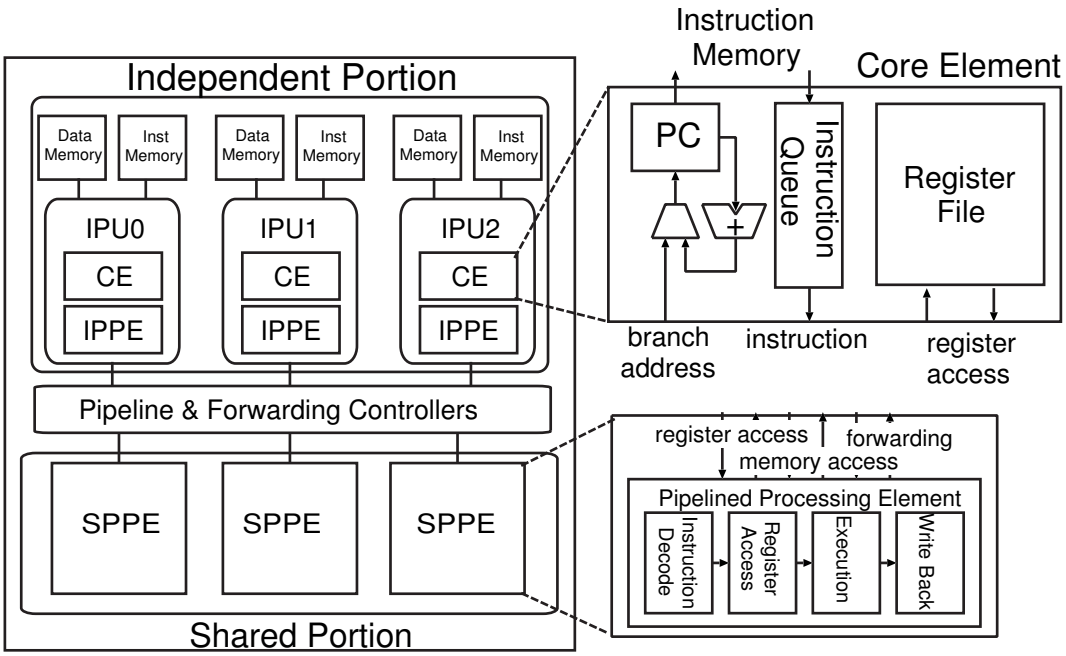


Fig. 2 Block diagram of resource-shared VLIW processor which contains 3 IPUs and 3 SPPEs. It has a capability to construct three virtual 4-way VLIW processors.

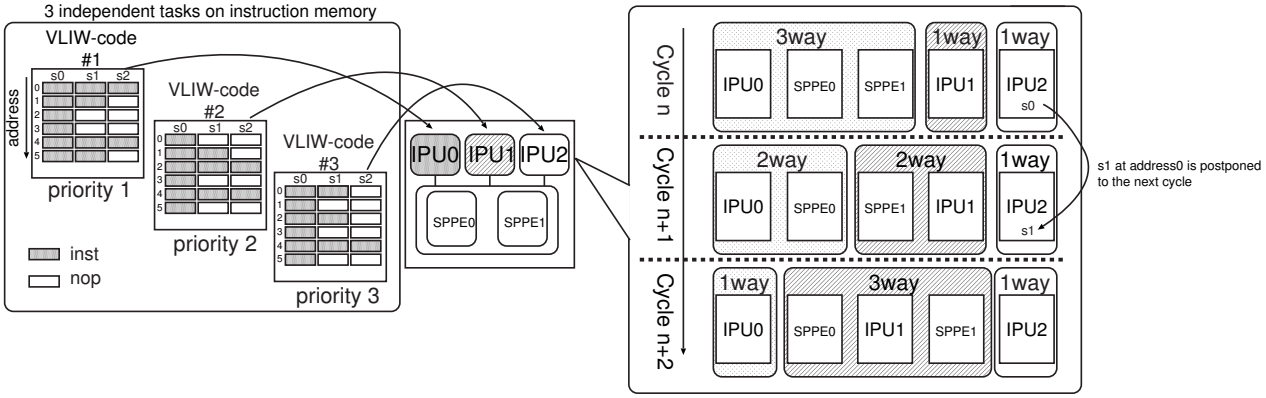


Fig. 3 Left: Three virtual VLIW codes for IPUs. Middle: An RSVP with three IPUs and two SPPEs. Right: The execution flow in three subsequent cycles.

ventional symmetric multiprocessor that contains two 2-way VLIWs. The right side shows an RSVP that contains two independent processor unit (IPU abbreviated as "I") and one shared pipelined processing element (SPPE abbreviated as "S"). It is correspond to two 2-way virtual VLIW processor cores that shares one SPPE. An IPU gets an SPPE if the priority of the given task is higher and it has a capability to issue two instructions at the same time. The number of ways of each IPU can be changed dynamically cycle by cycle. The IPU that runs the higher priority task always wins to get required number of hardware resources.

Fig. 2 shows a detailed block diagram of the RSVP. It consists of independent and shared portions. An IPU in the independent portion works as a scalar processor having a program counter, a register file, and an independent pipelined processing element (IPPE) executing instructions in the four-stage pipeline. An IPU executes a single instruction per cycle without SPPEs. But it obtains SPPEs when executing multiple instructions in one cycle. At that time, an IPU and and the assigned SPPEs form a VLIW processor. The number of ways can be changed dynamically cycle by cycle using the Pipeline & Forwarding Controller(PFC). Fig. 4 shows the structure of PFC. It consists of a priority encoder, shift registers, multiplexers and demultiplexers. Each stage of the shift registers holds the IPU number where the instruction of the stage is sent. The priority encoder chooses the instruction from the IPU which executes the highest priority task. According to the IPU number, the multiplexer receives forwarding data from other SPPEs and IPUs and the demultiplexer sends for-

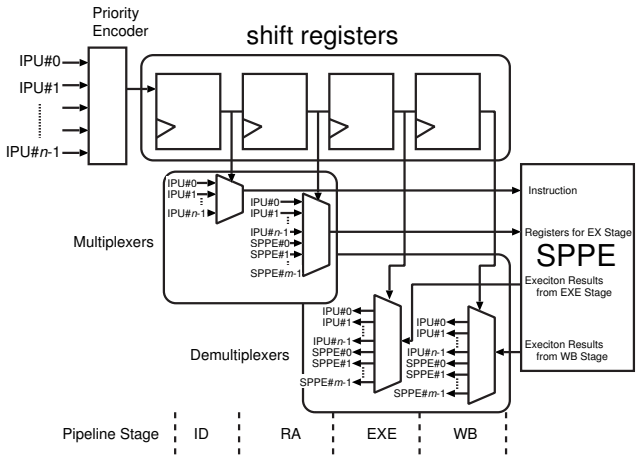


Fig. 4 Pipeline and forwarding controller (PFC) which sends and receives forwarding data. The parameters, n and m denote the number of IPUs and the number of SPPEs respectively.

warding data.

If the total number of instructions assigned to all IPUs exceeds the sum of IPUs and SPPEs, an IPU with the higher-priority task wins to obtain SPPEs. When the number of ways of an IPU with the lower-priority task is less than the number of parallel instructions, the possible number of instructions are executed in the current cycle. The rest of instructions are postponed to be executed in the successive cycles. In the conventional VLIW processors, a group of parallel instructions assigned to a single cycle cannot be ungrouped in order to be executed multiple cycles. It is because the execution results will be inconsistent if an instruction uses source registers which will be overwritten by the execution of another instruction at the same cycle. In the proposed RSVP, we prohibit to group the instructions that cannot be ungrouped for the multiple-cycle execution.

Fig. 3 shows a program execution scheme of the RSVP that contains three IPUs and two SPPEs. It can be configured as the following two structures.

1. one 3-way VLIW + two 1-way VLIWs (Cycle n and $n+2$ in Fig. 3)
2. two 2-way VLIWs + one 1-way VLIW (Cycle $n+1$ in Fig. 3)

Each IPU runs a statically scheduled 3-way VLIW codes with priorities. The IPU with the highest priority (IPU0) always wins to get required number of SPPEs. The rest IPUs can obtain SPPEs if the code in IPU0 contains NOPs. If an IPU with the lower priority fails to execute prepared VLIW instructions, they are postponed to the next cycle. In Fig. 3, IPU2 fails to execute the instruction in s1 at Cycle n, which is postponed to the next cycle (Cycle $n+1$).

Peak performance of parallel processors can be improved according to the number of ways. But it also increases the amount of idle hardware resources. For example, the IPC of an 8-way VLIW processor[3] is 3.14, which means 5 parallel resources are idle or execute NOP on the average. In the upcoming nanometer process, leakage current of transistors becomes dominant compared with the current submicron process in which dynamic and short-circuit current is dominant. Therefore, these idle parallel resources consume power that cannot be neglected in the future nm process. If they can be used from other processors, the total performance can be increased while reducing the circuit area. We propose the RSVP architecture to activate hardware resources as much as possible, while keeping the hardware size as small as possible to share rarely-used parallel resources. The RSVP keeps the peak performance compared with the multiple VLIW cores that contain the same number of processing elements since the IPU with the highest priority always wins to get the maximum number of shared processing elements.

3. Efficiency of Parallel Computation: Performance per Power or Area

It is a common sense that parallel computing increases performance per power (P^3). Here we evaluate P^3 among synthesizable VLIW processors and the proposed RSVP based on the MIPS architecture[4]. We use seven reference programs written in C as shown in Table 1 to obtain average IPC and MIPS (Mega Instruction Per Second) of each processor.

These reference programs are compiled through a GCC compiler for ordinal scalar processors and then manually converted to the VLIW codes. MIPS values are obtained by running these reference programs on instruction-set simulators (ISS).

3.1 Comparisons among single and multiple VLIW processors

Here, we evaluate performance per power and performance per area among three configurations, a 2-way VLIW processor (1X-2W), a double-speed 2-way VLIW processor (2X-2W) and a 2-parallel 2-way VLIW processor (2P-2W). First, a 2-way VLIW processor is synthesized at 100MHz clock frequency using a 180nm CMOS library characterized in 1.8V[6]. It is a MIPS-compatible VLIW processor described at the RTL. It is re-synthesized at 200MHz clock frequency using a 2.4V-characterized library. Dissipated power on VLIW processors consists of these two factors. One is pro-

Table 1 Seven reference programs.

avg	Computing averages
bubble	Bubble sort
heap	Heap sort
matrix	Calculating the product of matrixes
idct	Inverse discrete cosine transform
feal	Cipher program[5]
fir	FIR filter

Table 2 Comparison of performance per power in MIPS/W among a 2-way VLIW processor (1X-2W), a double-speed 2-way VLIW processor (2X-2W) and a 2-parallel 2-way VLIW processor (2P-2W) in a 180nm CMOS process.

Type	1X-2W	2X-2W	2P-2W
VDD(V)	1.8	2.4	1.8
Freq.(MHz)	100	200	100
Power(mW)	57.1	269.0	114.1
Area (mm^2)	1.65	1.79	3.31
# of Tr.	267k	289k	534k
IPC∗	1.23	1.23	2.46
MIPS	123	246	246
MIPS/W (P^3)	2156	918	2156
MIPS/mm^2 (P^2A)	74.1	137.4	74.1

∗: Instruction Per Clock.

portional to the number of ways $N_{\rm w}$ and the number of parallel processors $N_{\rm p}$, the other is proportional to the number of instructions per clock ($I_{\rm VLIW}$). Eq. (1) shows the equation of the dissipated power. From the netlist-level simulations, we have obtained the function $P_{\rm f}()$ and the parameter $P_{\rm I}$ as in Eq. (1). Eq. (2) is the equation used for 1.8V.

$$P_{\rm VLIW} = P_{\rm f}(N_{\rm w}) \times N_{\rm p} + P_{\rm I} \times I_{\rm VLIW} \quad (1)$$

$$P_{\rm VLIW,1.8V} = (5.27 + 1.54 \times (N_{\rm w} - 1)) \times N_p + 40.8 \times I_{\rm VLIW} \quad [mW] \quad (2)$$

Table 2 shows the results. The area of 2X-2W is just 8.4% larger than that of 1X-2W but its power is 4.7 times larger. On the other hand, the area and power of 2P-2W are twice larger than those of 1X-2W. As the result, the P^3 of 2P-2W is 2.3 times better than that of 2X-2W. As for the performance per area (P^2A), however, the multiprocessor (2P-2W) solution is inferior to 2X-2W. In the future leaky nanometer era, leakage power will be proportional to the area or the number of transistors. Therefore, it is indispensable to reduce the area while keeping performance. The proposed RSVP architecture reduces the area to share rarely-used parallel resources. Therefore performance per area of the RSVP becomes better than conventional VLIWs. These results are shown in the following section.

3.2 Comparison among VLIW processors and the proposed RSVP

Table 3 compares conventional VLIW multiprocessors and RSVPs in performancce(MIPS), P^3 (MIPS/W) and P^2A (MIPS/mm^2). Note that 3P-2W means 3-parallel 2-way VLIW multiprocessors. The areas are obtained from the results of the RTL-synthesis. The power dissipations of the VLIW processors are obtained from Eq. (2). Those of the RSVPs are computed from Eq. (3) and Eq. (4), which consists of power from the IPUs, SPPEs and PFC.

$$P_{\rm RSVP} = P_{\rm IPU} \times N_{\rm IPU} + P_{\rm SPPE} \times N_{\rm SPPE} + P_{\rm I} \times I_{RSVP} + P_{\rm PFC} \quad (3)$$

$$P_{\rm RSVP,1.8V} = 5.27 \times N_{\rm IPU} + 1.54 \times N_{\rm SPPE} + 40.8 \times I_{RSVP} + P_{\rm PFC} \quad [mW] \quad (4)$$

The performances of the RSVPs are a little bit inferior to those of VLIWs. The areas of the RSVPs, however, become much smaller and the P^3 are almost equivalent. The P^2A of the RSVPs are always better than those of VLIWs as shown in Fig. 5. The 2P-2W RSVP is 10% better in MIPS/mm^2 compared with the 2P-2W VLIW, while the 2P-3W RSVP becomes 14% better. The MIPS/mm^2 of the nP-4W RSVPs becomes better than that of VLIWs according to n, the number of independent parallel processors. The MIPS/mm^2 at the 4P-4W RSVP, for example, is 33% better than that of the 4P-4W conventional VLIW multiprocessors. Note that better P^3 will lead smaller leakage current in the future nanometer process as shown in the next section.

The area of the shared portion can be enlarged by migrating rarely-used instructions to SPPEs while keeping IPCs. Note that the above comparisons are estimated assuming that IPUs and SPPEs have the same execution units.

The areas in Table 3 includes the areas of PFCs, which becomes larger and larger according to the number of SPPEs and IPUs. However, the area of PFC of 4P-4W RSVP occpies just 4.2% (.34mm^2) of the total area (7.93mm^2). Even if the total number of processors is large, it is not mandatory to connect all IPUs and SPPEs by PFCs. It is because the number of concurrent instructions can be eliminated to four at most in general. The wider connection by the PFC will just increase area and power but give a little contribution to performance.

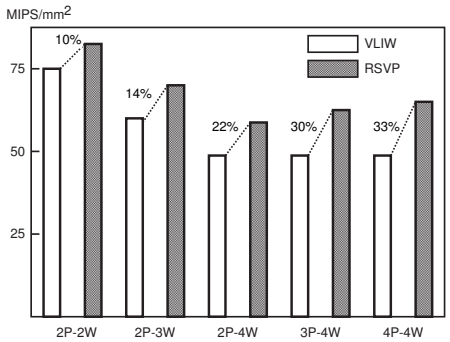


Fig. 5 MIPS/mm^2 of RSVPs and VLIWs according to the number of parallel processors(P) and the number of way (W).

4. Perspectives of Total Dissipating Power in the Nanometer Era

Estimations in the last section is done using a 180nm

Table 3 Comparison of MIPS/W and MIPS/mm^2 among conventional VLIW processors (top) and the proposed RSVP (bottom) in a 180nm CMOS process. (VDD=1.8V, clock freq=100MHz)

Type	2P-2W VLIW	2P-3W VLIW	2P-4W VLIW	3P-4W VLIW	4P-4W VLIW
Power(mW)	114.1	134.3	141.5	212.2	282.9
# of Tr	534K	758K	986K	1,479K	1,972K
Area(mm^2)	3.31	4.73	6.17	9.26	12.34
IPC	2.46	2.88	2.98	4.47	5.96
MIPS	246	288	298	447	596
MIPS/W	2156	2144	2106	2106	2106
MIPS/mm^2	74.1	60.7	48.2	48.2	48.2
Type	2P-2W RSVP	2P-3W RSVP	2P-4W RSVP	3P-4W RSVP	4P-4W RSVP
Power(mW)	108.3	126.1	134.0	190.2	242.9
# of Tr	461K	620K	775K	1,037K	1,299K
Area(mm^2)	2.82	3.80	4.75	6.35	7.93
PFC Area	0.06	0.16	0.21	0.29	0.34
IPC	2.31	2.64	2.78	3.97	5.09
MIPS	231	264	278	397	509
MIPS/W	2133	2094	2075	2087	2096
MIPS/mm^2	81.6	69.4	58.6	62.5	64.2

4P-4W means 4-parallel 4-way VLIW processors.

process in which leakage current can be ignored. In the nanometer era, subthreshold and gate leakage currents become dominant. Dissipated power of an integrated circuit is described as Eq. (5).

$$\begin{aligned} P_{\text{Total}} &= P_{\text{Dynamic}} + P_{\text{Leak}} \\ &= \alpha f C V_{\text{dd}}^2 + I_{\text{Leak}} V_{\text{dd}} \end{aligned} \tag{5}$$

The factor, I_{Leak} increases according to the number of transistors, i.e. the circuit area. Table 4 summarizes several features of the 4P-4W RSVP and VLIW according to the process minimization. The values in the 90nm process are obtained from a 90nm actual high-speed library. They are scaled using the ITRS 2001 high performance model[7].

Figure 4 shows dynamic and leakage power of the 4P-4W VLIW and RSVP. From 180nm to 90nm, power decreases very drastically since the active power decreases according to the transistor sizing with a little bit of increase of leakage power. But leakage power will be dominant according to the process minimization. Below the 90nm process, power dissipations do not change drastically. The RSVP dissipates less power since it occupies smaller area than the VLIW multiprocessor.

Figure 7 shows the performance per power (P^3) in MIPS/W of the RSVP and VLIW. The P^3 of the RSVP

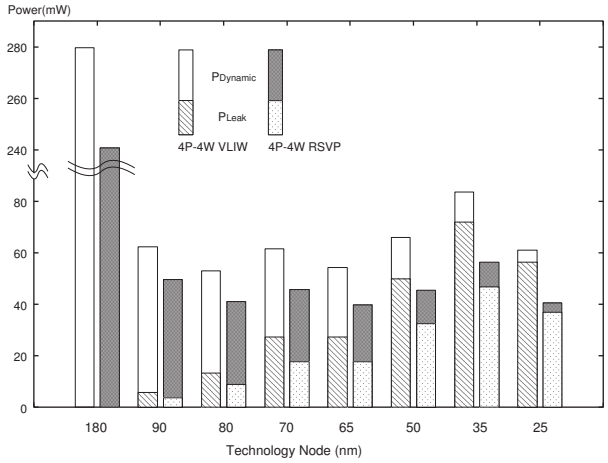


Fig. 6 Power dissipation of 4P-4W VLIW and RSVP as the process minimization.

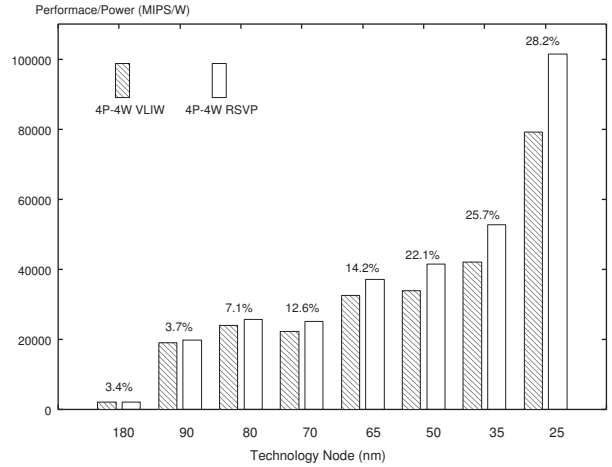


Fig. 7 Performance/Power(P^3) in MIPS/W of 4P-4W VLIW and RSVP as the process minimization. The values in percentage are calculated by $(P^3_{\text{RSVP}} - P^3_{\text{VLIW}})/P^3_{\text{VLIW}}$.

is almost equivalent to that of the VLIW in the 180nm process. But it becomes much better according to the process minimization. In the 90nm process, the P^3 of the RSVP is just 3.7% better than that of the VLIW. In the 25nm process the P^3 of the RSVP will become 28.2% better. On the other hand, the performance per area (P^{2}A) in MIPS/mm^2 increases at almost the same rate both on the RSVP and on the VLIW. The P^{2}As of the RSVP are 32.8% superior to those of the VLIW in all the processes in Table 4.

5. Test Chip

We have fabricated a test chip of the RSVP that contains two IPUs and one SPPE in a 5.9mm□ die using a 1P/5M 180nm CMOS process. Table 5 shows the gate count for the IPU, the SPPE and the Pipeline & Forwarding Controller (PFC). The SPPE of the implemented LSI contains no multiplier by the area lim-

Table 4 Features of the 4P-4W VLIW and RSVP as the process minimization estimated from the ITRS 2001 high performance model. Values of the 90nm process are obtained from an actual 90nm library.

	Process (nm)	90	80	70	65	50	35	25
	Active Power (ratio)	1.00	0.66	0.53	0.32	0.15	0.07	0.02
	Leakage Power (ratio)	1.00	2.36	4.82	4.82	8.82	12.73	10.00
	Frequency(MHz)	200	214	231	296	375	589	812
RSVP	Area (mm^2)	0.99	0.78	0.60	0.52	0.31	0.15	0.08
RSVP	Active Power(mW)	47.70	33.44	28.94	22.83	13.54	9.93	3.91
RSVP	Leakage Power(mW)	3.68	8.70	17.73	17.73	32.45	46.84	36.80
RSVP	Total Power(mW)	51.38	42.14	46.67	40.56	45.99	56.77	40.71
RSVP	Performace/Power(MIPS/W)	19800	25700	25100	37100	41400	52800	101500
RSVP	Performance/Area (MIPS/mm^2)	1028	1390	1964	2919	6244	20024	54114
VLIW	Area (mm^2)	1.54	1.22	0.93	0.80	0.48	0.23	0.12
VLIW	Active Power(mW)	56.60	39.68	34.34	27.09	16.07	11.79	4.64
VLIW	Leakage Power(mW)	5.64	13.33	27.17	27.17	49.73	71.78	56.40
VLIW	Total Power(mW)	62.24	53.01	61.51	54.26	65.80	83.57	61.04
VLIW	Performace/Power(MIPS/W)	19100	24000	22300	32500	33900	42000	79200
VLIW	Performance/Area (MIPS/mm^2)	774	1046	1478	2197	4700	15073	40733

Table 5 Gate count of each module of the implemented RSVP.

Module		#	# of gates	ratio(%)
IPU	CE	2	39324	49.7
	IPPE	2	31572	39.9
SPPE		1	7452	9.4
PFC		1	806	1.0

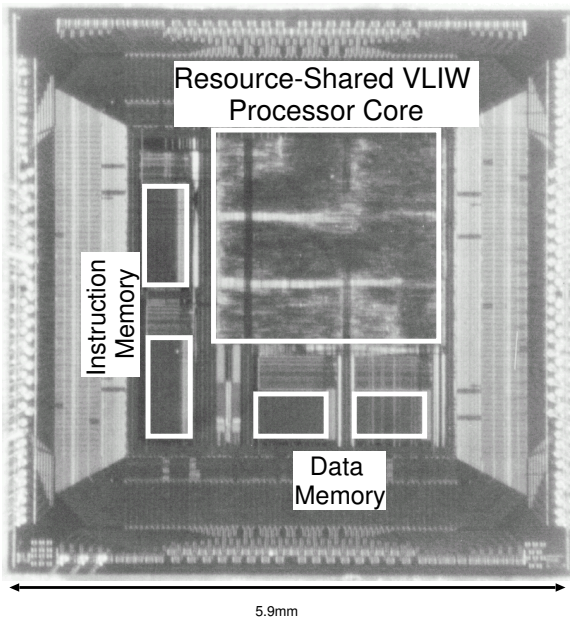


Fig. 8 Chip micrograph of an RSVP test chip including two IPUs and one SPPE.

itation. Fig. 8 shows a chip micrograph and Table 6 shows its specification. The RSVP core is fully synthesized from an RTL SystemC code and place-routed automatically with conventional DA tools.

The test chip is fully functional at 100MHz clock frequency and its power dissipation is 130mW including the RSVP core and data/instruction memory macros. Fig. 9 shows a Shmoo plot.

Table 6 Specification of the test chip.

Technology	1P/5M 180nm CMOS
Chip Area	34.8mm^2 (5.9mm□)
Supply Voltage	1.8V
Area of the RSVP (P&R)	5.35mm^2
(Synthesized)	2.60mm^2
Data Memory	64b×512W ×2 (instruction)
Inst. Memory	32b×1024W ×2 (data)
Operating Frequency	100MHz
Power Consumption	130mW

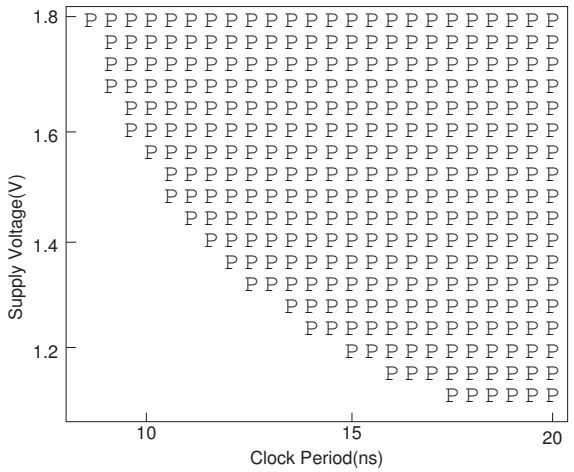


Fig. 9 Shmoo plot of the test chip.

6. Conclusions

The resource-shared VLIW processor (RSVP) increases the performance per area to share parallel hardware resources. The RSVP consists of independent processing units (IPUs) and shared pipelined processing elements (SPPEs). An IPU with the higher priority task always wins to get required number of SPPEs. Estimations from the ITRS 2001 high performance transistor models show that the 4P-4W RSVP with four

IPUs and four SPPEs achieves 3.7% better performance per power compared with the conventional the 4P-4W VLIW multiprocessor in the current 90nm process. In the nanometer era with more leaky transistors, leakage power will become dominant. The 4P-4W RSVP shows 28% better performance per power than the 4P-4W VLIW in the future 25nm process.

We have fabricated a test chip in a 1P-5M 180nm CMOS process that contains a 2P-2W RSVP . It is fully-functional and its power consumption at 100MHz is 130mW.

Parallel processing is frequently used to decrease frequencies and supply voltage while enhancing the performance. In general, prepared parallel processing resources are rarely used except for single-instruction multiple-data (SIMD) operations. These unused resources consume idle power in the future nanometer process. The proposed resource-shared VLIW processor architecture will give a solution for low-power in the nanometer era.

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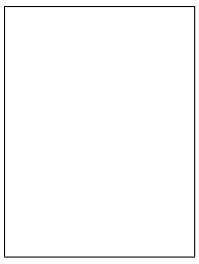
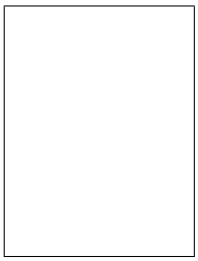
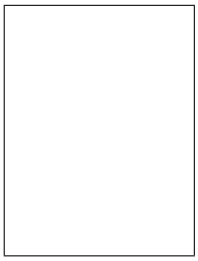


Kazutoshi Kobayashi was born in Kyoto, Japan in 1968. He received the B.E., M.E. and Dr. Eng. degrees in Electronic Engineering from Kyoto University, Kyoto, Japan, in 1991, 1993, 1999, respectively. His interests are in architectures and implementations of parallel computers. He was an Instructor (1993-2001), an Associate Professor(2001-2002) in Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. From 2002 to 2004, he was an Associate Professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2004, he is an Associate Professor in Kyoto University. He received a design award of the University LSI Design Contest at ASP-DAC'97. He is a member of IEEE, IEICE and IPSJ.



Masao Aramoto received the B.E. degree in Electrical and Electronic Engineering and the M.E. degree in Communication and Computer Engineering from Kyoto University, Japan in 2004. Since 2004 he has been with Renesas Technology Co., Ltd.



Hidetoshi Onodera received B.E., M.E. and Dr. Eng. degrees in Electronic Engineering from Kyoto University, Kyoto, Japan, in 1978, 1980, 1984, respectively. Since 1983 he has been an Instructor(1983-1991), an Associate Professor(1992-1998), a Professor(1999-) in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. His research interests include computer-aided design of digital and analog LSIs, analog and mixed analog-digital circuits design, and design methods for low power and high speed LSIs. He is a member of the Information Processing Society of Japan, and IEEE.