PAPER

An Analysis of Local BTI Variation with Ring-Oscillator in Advanced Processes and Its Impact on Logic Circuit and SRAM

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SUMMARY
In this paper, we present an analysis of local variability of bias temperature instability (BTI) by measuring Ring-Oscillators (RO) on various processes and its impact on logic circuit and SRAM. The evaluation results based on measuring ROs of a test elementary group (TEG) fabricated in 7 nm Fin Field Effect Transistor (FinFET) process, 16/14 nm generation FinFET processes and a 28 nm planer process show that the standard deviations of Negative BTI (NBTI) V_{th} degradation ($\sigma(\Delta V_{thp})$) are proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors and various recovery conditions. While the amount of local BTI variation depends on the gate length, width and number of fins, the amount of local BTI variation at the 7 nm FinFET process is slightly larger than other processes. Based on these measurement results, we present an analysis result of its impact on logic circuit considering measured V_{th} dependency on global NBTI in the 7 nm FinFET process. We also analyse its impact on SRAM minimum operation voltage (V_{min}) of static noise margin (SNM) based on sensitivity analysis and shows non-negligible V_{min} degradation caused by local NBTI.
key words: *local BTI variation, Ring-Oscillator, 7nm FinFET, SRAM Vmin*

1. Introduction

In recent years, it is inevitable to pursue higher performance for automotive LSIs such as advanced driver-assistance systems (ADAS) and autonomous driving [1][2]. Higher performance should be achieved under limited power budget at high temperature condition of the car because huge power consumption leads to requirement of huge and expensive cooling systems in the car's Electronic Control Unit (ECU). which is one of the key motivations for automotive chips to apply cutting-edge process technologies such as a 7 nm Fin Field Effect Transistor (FinFET) process [3][4]. Meanwhile, a high reliability is also required in automotive chips especially for autonomous driving era because car accidents directly threaten human life. Furthermore, the paradigm shift of car usage by autonomous driving would worsen reliability. The high temperature condition of the car causes a big impact on both power consumption and reliability. In general, chip designers take guard-band into account in product design and test [5] to prevent delay failures caused by device aging effects at the end of the products lifetime. However this guard-band restricts the performance and energy efficiency. To realize high performance with low power and high reliability, we need to optimize the guard-band for aging. The device aging effects such as bias temperature instability (BTI) manifest themselves especially in scaled-down process technologies because of small design margin at low supply voltage (VDD) [6]. In addition to time-0 variation due to process variation [7-10], there is BTI induced variability especially in scaled process technology node [11-14]. Therefore, considering both time-0 (before stress) process variation and local BTI variation (after stress) at cutting-edge process technologies is one of the key issues for robust design in automotive applications where high reliability is required for human safety.

This paper is an extended version of the original conference paper [15] with adding detail description, other results at different process nodes. This paper organized as followings. Section II introduces the structure of a test elementary group (TEG) and its measurement methodology. Section III describes the measurement results and discussions. In Section IV, we describe the analysis results of impact of local BTI variation on logic circuit and SRAM in 7 nm FinFET. A brief conclusion is given in Section V.

2. Test Element Group Structure and Measurement Methodology

In this section, we describe our test chip structure fabricated in a 7nm FinFET bulk CMOS technology and measurement methodology which enables to monitor V_{th} transition at various stressed phases.

Figure 1 shows a block diagram and a die photo of a TEG including lots of ring oscillators (ROs) to measure BTI degradations. The circuit diagram of Figure 1 shows a state of 0 or 1 of each node when ROs stop oscillation. The red and blue schematics illustrate that each cell has Negative BTI (NBTI) or Positive BTI (PBTI) stress during non-oscillation condition, respectively. The purpose of "Block A" and "Block B" is to measure on-chip variation and chip mean BTI degradation, respectively. In "Block A", there are 128 9-stage-ROs with 2-input NAND cell with 3 flavors of V_{th} and 2 types of cell heights to measure both time-0 variation and local BTI variation. As for cell-height type, one includes two fins per finger and the other four fins per finger. One of the input signals of each NAND cell is fixed to the VDD except for the control cell. We use it instead of

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the NAND in which the two inputs are connected to simulate the actual circuit of NAND. As illustrated in the red and blue schematic in Figure 1, this circuit configuration is affected by both NBTI and PBTI during non-oscillation condition. We select and activate one of ROs through the decoder and measure oscillation frequency with the counter one by one. All ROs share common counter, and each RO have dedicated frequency divider described as "divider" in Figure 1 because it is necessary to lower the oscillation frequency of each RO to transmit it to the common counter. In "Block B", there are two types of ROs; one is NOR-RO and the other is NAND-RO. NOR-RO and NAND-RO can fix all outputs to high or low respectively by EN or ENB that can apply NBTI or PBTI stress only on each RO [16][17]. These ROs have 61 stages to measure chip mean NBTI or PBTI degradation with local BTI variation suppressed. It is because if on chip BTI variation is random phenomenon like time-0 variation, it can be averaged over a large stage number of ROs. Note that we also have different three chips with similar configurations fabricated in two different 16/14 nm generation FinFET processes called process-A and process-B respectively and in a 28 nm process. In this paper, unless otherwise noted, the measurement results of the 7 nm TEG are shown.

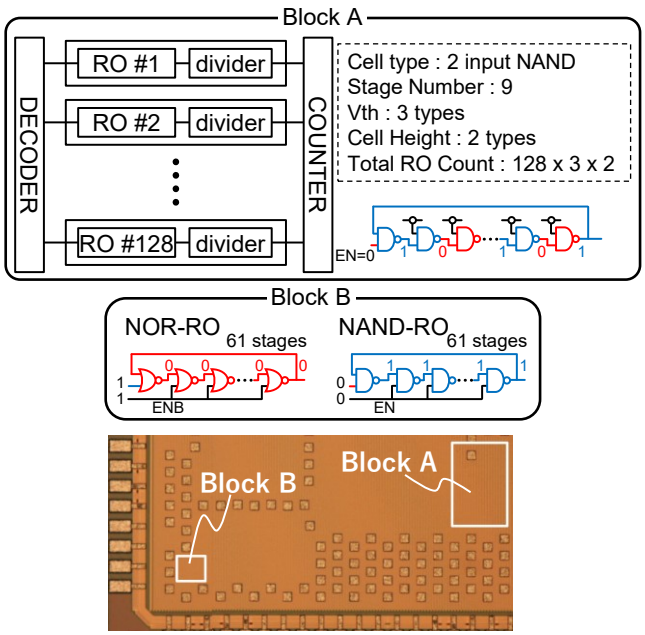

Fig. 1 Block diagram and die photo of TEG in 7 nm FinFET process

Figure 2 shows a schematic waveform of VDD which is applied to the TEG. *Tpd* means inverse of the oscillation frequency (*F*) of RO. We measure Tpd at 4 conditions as shown in red squares: (a) fresh measurement as a reference (*Tpd0* or *F0*), (b) stress phase measurement, (c) initial measurement after stress for suppressing BTI recovery effect, (d) measurement with recovery by power-down to accelerate recovery. A high voltage and high temperature stress with several hours stress are applied to all ROs during stress phase at non-oscillation condition (DC stress). This total amount of stress is intended to cover the expected field stress of the product. Stress voltage is more than 1.5 times higher than the monitor voltage. We measure Tpd only for "Block A" in the stress phase. ΔTpd and ΔF are the difference between fresh and aged *Tpd* and operation frequency *F*, respectively. The monitor voltage for measuring oscillation frequency is set to be lower than stress voltage because the impact of BTI on $\Delta Tpd/Tpd0$ and $\Delta F/F0$ is relatively increased with decreasing VDD due to decrease of gate overdrive voltage "$V_{gs} - V_{th}$". Note that all ROs are sequentially measured one by one to sufficiently suppress a power supply noise caused by the oscillation and ROs besides oscillated one are suspended. As a result, no harmonic noise was observed although the stage number of RO in "Block A" is not a prime number. The measurement time of each RO is around 200 μs and the interval between each RO is around 10 μs.

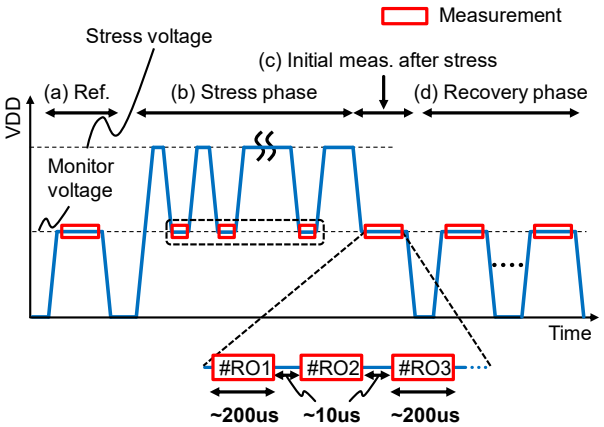

Fig. 2 Measurement waveform of supply voltage, measurement time and interval.

3. Measurement Results

In this section, we describe the measurement results and its analysis results of both chip mean BTI degradation and BTI induced local variation.

3.1 Chip Mean degradation of BTI

We estimated a chip mean V_{th} degradation (ΔV_{th}) of NBTI and PBTI based on measurement results of RO by using following equation:

$$\Delta Tpd/Tpd0 = \alpha \Delta Vthn + \beta \Delta Vthp \quad (1)$$

where ΔV_{thn} and ΔV_{thp} mean estimation result of PBTI and NBTI induced *Vth* degradation, ΔTpd and *Tpd0* means measured Tpd degradation and fresh one, and α and β mean simulated PBTI and NBTI sensitivity factor of each RO, respectively. For example, α is calculated from the simulated ΔTpd when the V_{th} of the stressed NMOS is increased by a certain amount of ΔV_{thn}. The parameter α and β are varied depended on circuit configuration of each RO [18] and V_{th} flavor. The linearity and additivity of Eq. (1) of each RO are

confirmed by SPICE simulation [18]. Since we can selectively apply NBTI or PBTI stress on NOR-RO and NAND-RO under DC stress as described in section 2, α of NOR-RO and β of NAND-RO equal 0. As a result, we can separately estimate ΔV_{thn} and ΔV_{thp} by measuring NOR-RO and NAND-RO. Figure 3 shows chip mean BTI degradation of 6 chips normalized by MVT NBTI. MVT, LVT and ULVT mean flavors of V_{th} and represent medium, low and ultra-low V_{th} transistor, respectively. #1 to #6 indicate measurement chip numbers. As a result, in 7 nm, lower V_{th} device causes larger NBTI and ULVT is exposed to the worst NBTI. This is similar result in ref. [19][20] in case of V_{th} modulation using metal gate work function (MWF). The physical mechanism is that as V_{th} decreases due to MWF tuning, the conduction band offset to the gate oxide decreases and the electric field across the gate dielectric increases. As a result, NBTI degradation increases [21]. In case of V_{th} modulation by doping, V_{th} dependency on NBTI is vice versa.

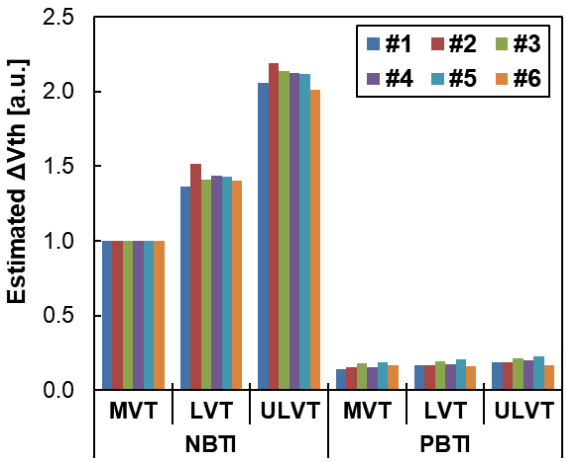

Fig. 3 Chip mean ΔV_{th} estimation by NOR-RO and NAND-RO measurement from 6 chips of 7 nm FinFET.

Figure 4 shows dependency of chip mean ΔV_{thp} on gate overdrive voltage "$V_{gs} - V_{thp}$" (Vov) normalized by MVT to analyze V_{th} dependency on NBTI. The dotted line is a line of exponential approximation. Note that we measured each V_{th} value of horizontal axis from Device Under Test (DUT) of PMOS transistors in the TEG. As a result, we can well explain the ΔV_{thp} of each V_{th} flavor with exponential approximation of Vov as described in ref. [21. ULVT has around 2.1x larger chip mean NBTI than MVT. In case of PBTI, it is significantly smaller than NBTI in all V_{th} flavors, indicating the similar result in ref. [22][23][24][25]. This is caused by decrease of the electrical field across gate dielectric in FinFET at the same Vov due to less depletion charge in strong inversion of fully depleted structure.

Figure 5 shows chip mean BTI degradation of each TEG normalized by each NBTI of MVT. When comparing NBTI and PBTI in each process, PBTI is significantly smaller than NBTI at process-A, process-B and 28 nm as same as 7 nm FinFET. Note that as for the 28 nm process we implemented only MVT and LVT transistors in the TEG. Therefore, NBTI and PBTI of ULVT of 28 nm process are N/A in Figure 5.

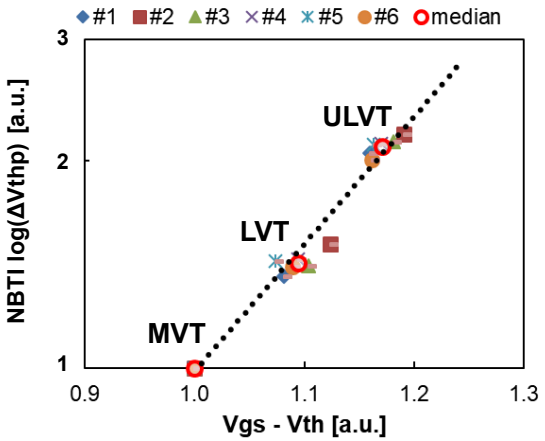

Fig. 4 V_{th} dependency on NBTI ΔV_{thp}

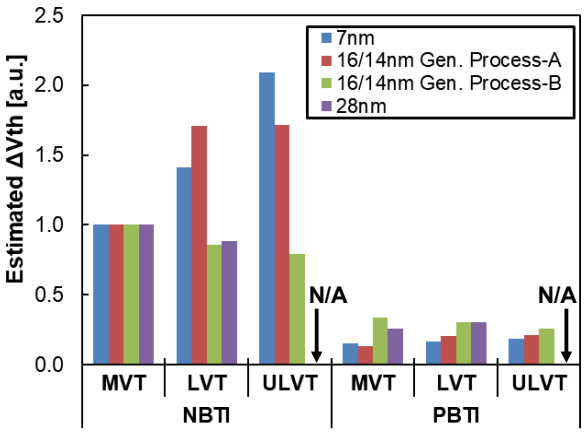

Fig. 5 Comparison of Chip mean ΔV_{th} of each process.

3.2 Local BTI Variation

Figure 6 shows dependency of ΔF of 128 ROs of "Block A" on its measurement order and its correlation coefficient. The numbers on the horizontal axis in Figure 6 (a) indicate the measurement order of the 128 ROs. Since we measured each RO one by one with around 200 μs measurement time and 10 μs interval, each RO have different wait time before measurement. Therefore, there is a concern that the BTI recovery effect may vary, depending on the measurement order. However, since the correlation coefficient between each ΔF and the measurement order is almost negligibly small as shown in Figure 6 (b), all measurement results of ΔF for each RO do not change by measurement order. From this result, we treat the recovery effect of each measurement result as almost the same.

Figure 7 demonstrates stress time and recovery time dependency on $\Delta F/F0$ of 128 ROs of "Block A" in the 7 nm TEG. We measured ΔF with different stress time from 30 seconds to 8 hours in case of 7 nm TEG. After 8 hours stress, stress is released for 100 seconds in total by power off. The

red bold line is drawn on the median values of 128 ROs and the other lines are measured results of each RO. The measured *ΔF/F0* follows a power-low model to stress time and its measured time dependency factor "*n*" is around 0.173 calculated by the median values. Figure 8 shows results of other processes whereas we extended the minimum stress time of process-B and 28 nm TEGs to 0.5 seconds to evaluate a characteristic of local BTI variation when BTI degradation is relatively small. The ratio of the maximum and minimum values to the median value of *ΔF/F0* decreases as the stress time increases in all measurement results.

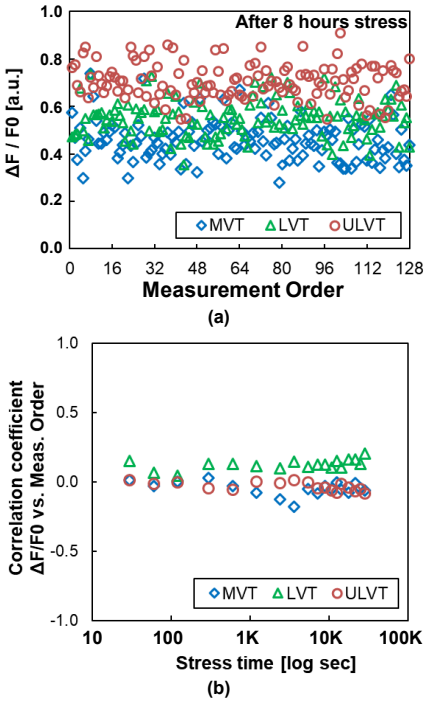

Fig. 6 Correlation between degradation of oscillation frequency of ROs and measurement order in "Block A"

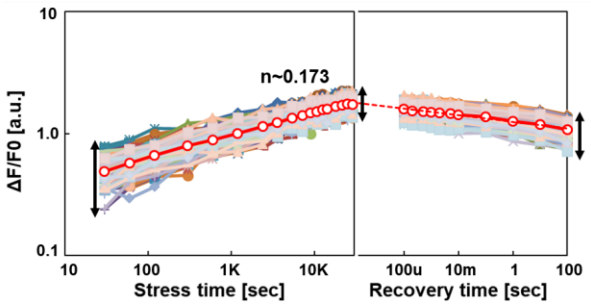

Fig. 7 Stress time and recovery time dependency on oscillation frequency degradation

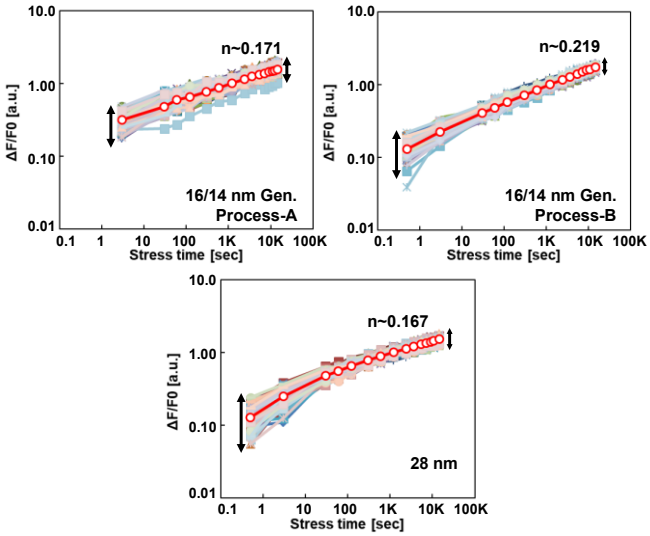

Fig 8. Stress time vs. oscillation frequency degradation of Process-A, B and 28 nm

Figure 9 shows distribution of *ΔF* at each stress time. It is not appropriate for evaluation of BTI variation to directly compare *ΔF* variation of different V_{th} flavors. It is because even if the degradation of BTI of each V_{th} flavor is the same, the *ΔF* of different V_{th} flavors is not the same due to the difference of *Vov* of each V_{th} flavor. For example, *ΔF* decreases with increasing *Vov* at constant ΔV_{th}. To address it, we convert *ΔF* to ΔV_{th}. Since NBTI is dominant factor compared to PBTI as shown in Figure 5, we assume that *ΔTpd* is proportional to NBTI degradation. We convert measured *ΔTpd* to ΔV_{thp} as in Equation (2).

$$\frac{\Delta Vthp}{\mu(\Delta Vthp)} = \frac{\Delta Tpd/Tpd0}{\mu(\Delta Tpd/Tpd0)} \quad (2)$$

where $\mu(\Delta Tpd/\Delta Tpd0)$ is measured mean *ΔTpd/Tpd0*, and $\mu(\Delta V_{thp})$ is estimated mean ΔV_{thp} from Eq. (1) and measured *ΔTpd* of NOR-RO.

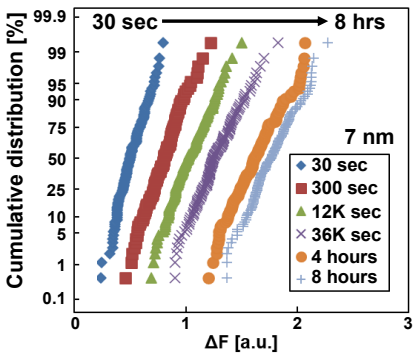

Fig. 9 Distribution of oscillation frequency degradation by local NBTI variation

Figure 10 shows relationship between the standard deviation of ΔV_{thp} ($\sigma(\Delta V_{thp})$) and $\mu(\Delta V_{thp})$ for each stress time and V_{th} flavor. The dots are measurement results and the solid line is an approximate line when $\sigma(\Delta V_{thp})$ is proportional to the square root of $\mu(\Delta V_{thp})$. As stress time increases, $\mu(\Delta V_{thp})$ increases whereas ratio of $\sigma(\Delta V_{thp})$ per

$\mu(\Delta V_{thp})$ decreases as expected in Figures 7 and 8, and the measurement results agree well with the approximate line. In this way, $\sigma(\Delta V_{thp})$ is proportional to the square root of $\mu(\Delta V_{thp})$ at any stress time and V_{th} flavors. This indicates that the total number of stress induced trapped carriers follows Poisson distribution as described in ref. [26][27] and this relationship is valid for all stress time and V_{th} flavors. In addition, Figure 11 shows measured results of $\sigma(\Delta V_{thp})/\mu(\Delta V_{thp})$ vs. $\mu(\Delta V_{thp})$ of 6 chip results. All of them follow the same universal curve. Furthermore, the measured results of 6 chips of both stress phase and recovery phase are shown in Figure 12 as black and red shapes, respectively. It shows that recovered ΔV_{thp} also follows the same universal curve. In this way, the amount of local NBTI variation of each V_{th} flavors at various stress and recovery condition can be estimated by the following simple equation:

$$\sigma(\Delta Vthp) = A \times \mu(\Delta Vthp)^{0.5} \quad (3)$$

where parameter "A" represents the magnitude of local NBTI variation. As shown in Figure 13, we can also see the same characteristics with respect to local BTI variation at the other three processes, where results of process-B and 28 nm process include relatively small stress condition (0.5 second).

Figure 14 shows fin number (Fin#) dependency on parameter "A" of the 7 nm FinFET. These were calculated by the measured data of 6 chips in each cell height with Eq. (3). Fin# means the number of fins per finger. The parameter "A" becomes 1.4x when Fin# becomes half (from 4 to 2). This rate almost the same as square root of 2. From these results, we assumed that the magnitude of the BTI induced variation is proportional to the inverse of the root of the fin number in the circuits as same as time-0 variation. In other words, parameter "A" of BTI corresponds to the "Avt" coefficient of process mismatch variation, called the Pelgrom's law [28].

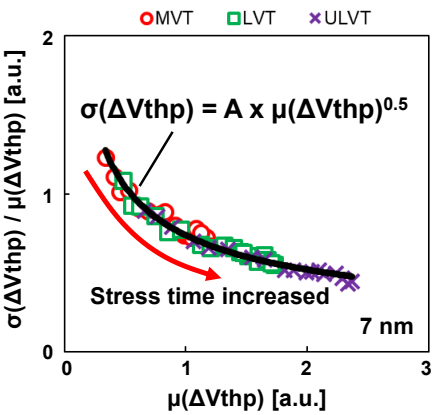

Fig. 10 Relationship between mean and standard deviation at 3 V_{th} flavors

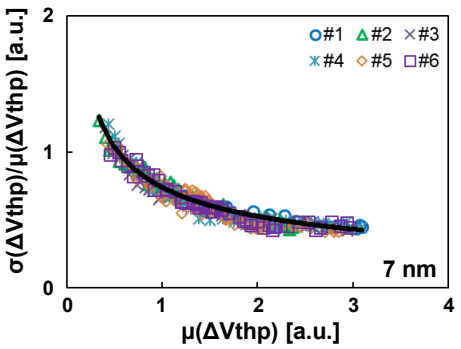

Fig. 11 σ/μ vs. μ of 6 chip measurement results

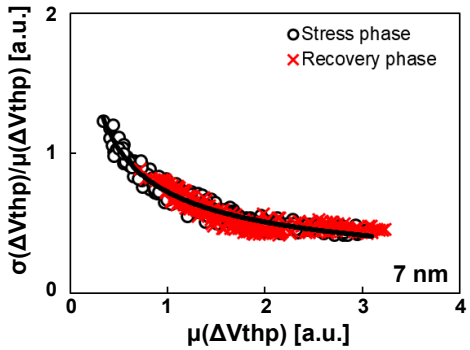

Fig. 12 σ/μ vs. μ at stress phase and recovery phase

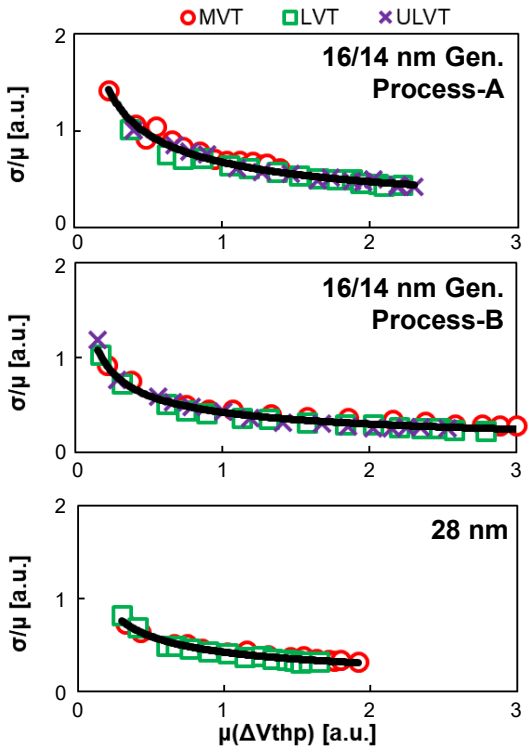

Fig. 13 σ/μ vs. μ at each process

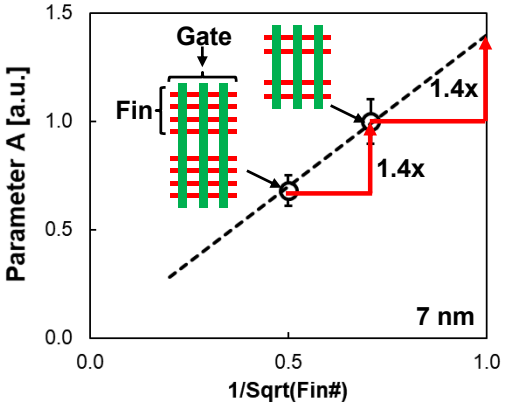

Fig. 14 Fin number dependency on local NBTI variation factor A

We also compare parameter *"A"* of each process. As for FinFET processes, we compared the parameter *"A"* with 2 fins based on measurement results or estimation results from other Fin# to make the condition uniform. In case of 28 nm, we used standard gate width of the highest density cell library. Figure 15 shows that the 7 nm FinFET has the largest local BTI variation compared with 16/14 nm generation FinFET processes and 28 nm process, and indicates the increase of importance of BTI variability as process technology proceed.

Figure 16 and 17 show the correlation between time-0 variation and local NBTI variation. ΔCount at fresh means the difference of the counted number from its mean value before stress. Figure 16 shows that correlation coefficient "R" between time-0 variation and local NBTI variation is 0.014, which can be considered uncorrelated. Figure 17 shows its correlation coefficient of each stress time and V_{th} flavor. Since there is almost no correlation between time-0 variation and local NBTI variation at each stress time, we regarded these variations are independent.

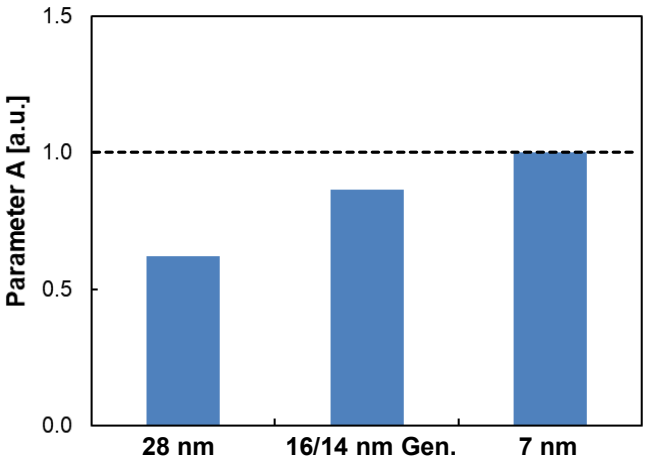

Figure 15. Comparison of parameter "A" of each process

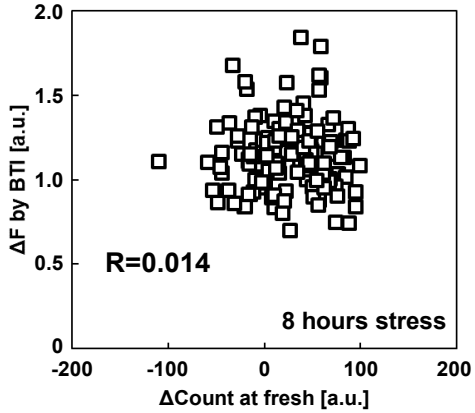

Figure 16. Time-0 variation vs. local NBTI variation induced oscillation frequency degradation

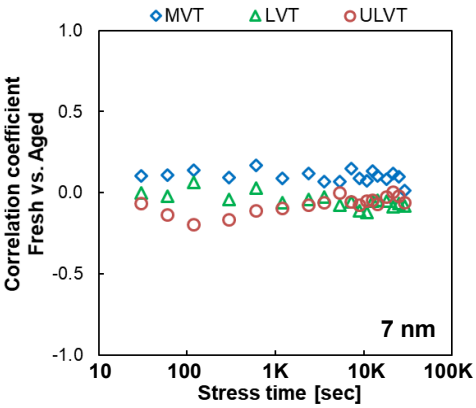

Figure 17. Correlation between time-0 variation and local NBTI variation

4. ANALYSIS OF IMPACT OF LOCAL BTI VARIATION ON LOGIC CIRCUIT AND SRAM

In this section, we discuss the impact of local NBTI variation on logic circuits and SRAM in the 7 nm FinFET process.

4.1 Analysis of Delay Variable of Logic Circuits

We estimated the impact of local NBTI variation on logic circuits. In this analysis, we focused on specific signal propagation delay only affected by NBTI in the normal case, expressed as Tpdlh in Figure 18 (a). Since time-0 variation and local NBTI variation are independent, we can estimate the total delay variation per stage by Eq. (4) that treats local NBTI variation follows a normal distribution:

$$\Delta Tpdlh(t) = \sqrt{\left(\Delta Tpdlh_{t0}{}^2 + \Delta Tpdlh_{NBTI}(t)^2\right)} \quad (4)$$

where $\Delta Tpdlh(t)$, $\Delta Tpdlh_{t0}$ and $\Delta Tpdlh_{nbti}(t)$ mean total, time-0 and local NBTI variation for fall input delay, respectively. Since $\Delta Tpdlh_{t0}$ is a time-independent variation factor, it is constant during product lifetime whereas $\Delta Tpdlh_{NBTI}(t)$ is a time-dependent factor following Eq. (3) and the sensitivity coefficient of *Tpdlh* to ΔV_{thp} as shown in Figure 18(b). As a result, when $\mu(\Delta V_{thp})$ of ULVT becomes 50mV, $\Delta Tpdlh(t)$ of ULVT is 1.11x increased in total by

local NBTI variation without considering local BTI. However, as shown in Figure 3 and the red line of Figure 18(c), there is V_{th} flavor dependency on NBTI and MVT has 2.1x smaller $\mu(\Delta V_{thp})$ than ULVT. This indicate that we can relax the impact of local NBTI variation on MVT cell which has the largest impact of V_{th} variation on its delay because of the smallest *Vov*. As a result, the uplift of $\Delta Tpdlh$ of MVT is relaxed from 1.11x to 1.06x with considering V_{th} dependency on NBTI.

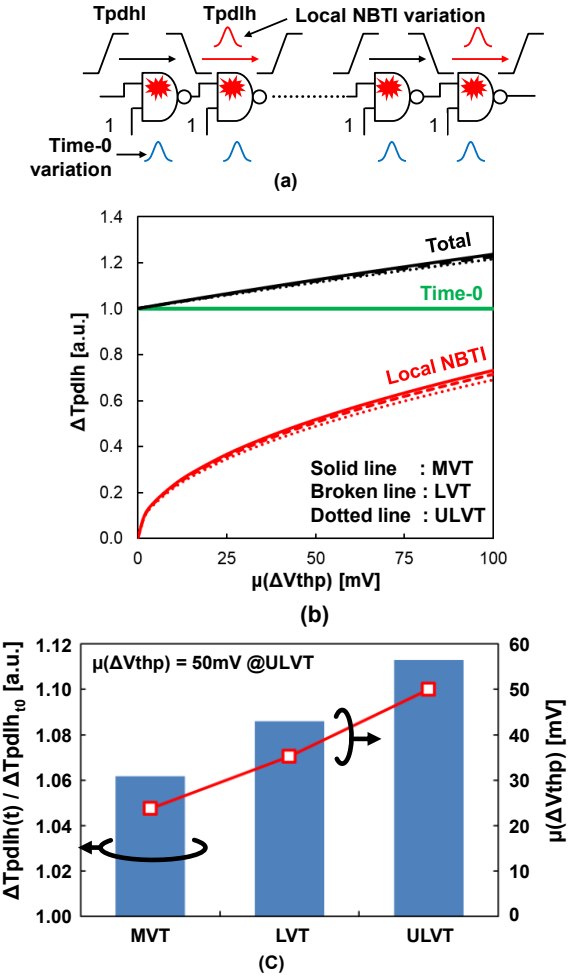

Fig. 18 (a) benchmark logic circuit, (b) impact of time-0, local NBTI and total variation on logic circuit based on measurement data and simulation (c) The impact of local BTI on circuit delay with considering V_{th} dependency of NBTI at the same stress condition

4.2 Analysis of Minimum Operation Voltage of SRAM

We examined how the local NBTI affects SRAM characteristics in 7 nm generation and beyond. In general, a single SRAM bit-cell has its own read/write margin depending on mean V_{th} and its local variation of the 6 transistors inside a bit-cell. Higher PMOS V_{th} degrades SRAM read margin (static noise margin, SNM) while it improves write margin, which indicates that NBTI with PMOS V_{th}-shift induces SNM deterioration [29][30]. The characteristic of a single bit-cell inside a collective SRAM macro manifests itself as a minimum operation voltage, V_{min}. Note that V_{min} is defined as the VDD where the first failure bit appears by lowering cell-array VDD. Figure 19 is a simulated sample of fail-bit rate of single 6T SRAM cell versus VDD without local NBTI before stress ($\mu(\Delta V_{thp})$ =0). The lower the VDD gets, the higher the fail-bit counts become (the smaller the absolute value of σ becomes), and we define V_{min} at 6σ [31]. We use the commercial SRAM bit cell's SPICE model and sensitivity analysis methodology shown in [31]. We demonstrate how V_{min} behaves by introducing NBTI mean shift, $\mu(\Delta V_{thp})$. The detail V_{min} difference between with and without local NBTI ($\sigma(\Delta V_{thp})$) is summarized in Figure 20, indicating non-negligible V_{min} degradation due to local NBTI. When $\mu(\Delta V_{thp})$ becomes 100 mV, $\Delta Vmin$ considering local NBTI variation is 1.4x bigger than without local NBTI variation.

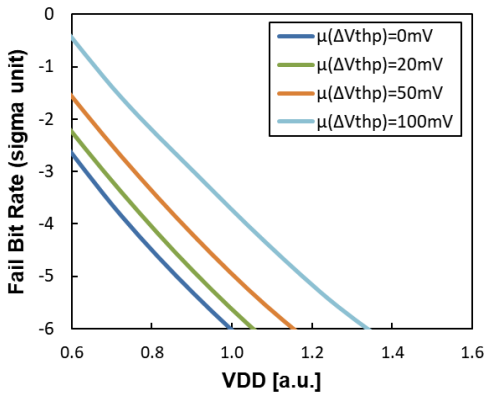

Fig. 19 Simulated SRAM fail-bit rate vs. VDD without local NBTI variation

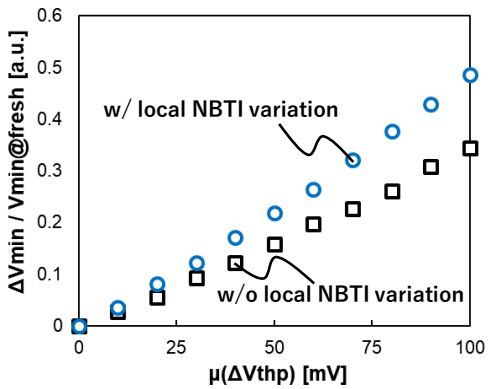

Fig. 20 Analysis of local NBTI variation induced SRAM Vmin degradation

5. Conclusion

We have presented the analysis of BTI degradation of both chip mean BTI and local BTI variation based on measurement results of Ring-Oscillators (RO) on TEGs fabricated in a 7 nm FinFET process, two 16/14 nm generation FinFET processes and a 28 nm process. The chip mean BTI degradation shows significant V_{th} dependency at

the 7 nm FinFET process. The negligibly small PBTI degradation compared with NBTI is also observed at all four processes. As for the analysis of local BTI variation, the standard deviation of NBTI V_{th} degradation is proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors any recovery time in all four processes. We also demonstrate the impact of Fin number and time-0 variation on local BTI. In addition, when comparing the magnitude of local NBTI variation of each process, it increased as process technology proceeds. From these evaluation results, we demonstrated the impact of local NBTI variation on the characteristics of both logic circuits and SRAM in the 7 nm FinFET. In logic circuits, when NBTI induced V_{th} degradation is 50 mV at ULVT and V_{th} dependency of NBTI is considered, the delay variation of MVT is increased by 1.06x from fresh one due to local NBTI variation. As for the impact on SRAM V_{min}, a simulation result indicates non-negligible V_{min} degradation due to local NBTI variation.

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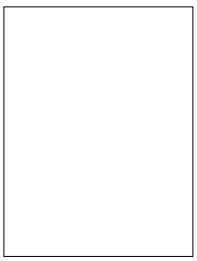

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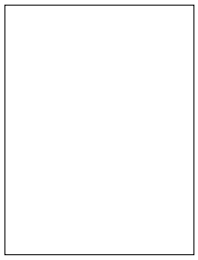

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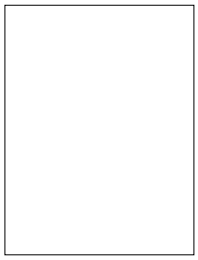

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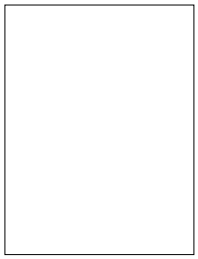
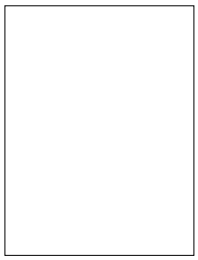
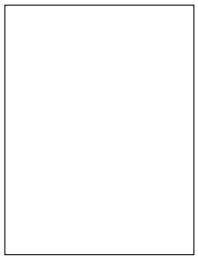


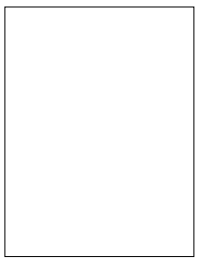
Makoto Yabuuchi received the B.S. and M.S. degrees in Electronic Engineering from Kanazawa University, Japan in 2002 and 2004, respectively, and the Ph. D. degree in the Graduate School of Natural Science and Technology from Kanazawa University, in 2018. He joined Renesas Technology Corp. after his graduation and transferred Renesas Electronics Corp. in 2010, where he has been working on designing embedded SRAMs for advanced CMOS logic process.



Yasumasa Tsukamoto received Ph. D. degree from Osaka University in 2001. His semiconductor research started at Mitsubishi Electric in 2001 through his transferring to Renesas Technology Corp. and Renesas Electronics Corporation. He had been engaged in the design of embedded SRAM based on 90nm to 28nm processes. From 2008 to 2010, he was a visiting industrial fellow at the UC Berkeley, where he conducted researches on tri-gate SRAM cell and reliability physics. Currently, he works for the design platform development in 16nm/10nm/7nm. He has authored or coauthored more than 40 papers including Young Researcher Award and the Best Paper Award.



Koji Shibutani received B.E. degrees in Materials Science and Chemical Engineering from Yokohama National University, Kanagawa, Japan in 1992. In 1992, he joined Mitsubishi Electronics Corporation Itami, Japan, where he has been working on designing Standard cells and embedded SRAMs. In 2003, he was transferred to Renesas Technology Corporation, Itami, Japan, which is a joint company of Mitsubishi Electric Corp. and Hitachi Ltd. in the semiconductor field. In January 2010, he transferred his work location to Kodaira, Tokyo from Itami, Hyogo. He currently works on developing design methodology and design platform on 28nm, 16nm FinFET and the beyond.



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While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors, Bias Temperature Instability and Plasma Induced Damage) of current and future VLSIs. He started a research related to gate drivers for power transistors since 2013.

He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.