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An Energy Efficient 2-Read/Write 8T Dual-Port SRAM with Disturbance Aware Self-Adjustable Replica Tracking Circuit

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SUMMARY An energy-efficient 2-read/write (2RW) dual-port (DP) SRAM with a new disturbance aware replica scheme has been demonstrated. This scheme aims to generate internal critical timing signals for sense-enable (SE) triggers and wordline (WL) negating paths during the readout operation. By placing individual replica circuits for each port, appropriate internal delays are generated self-adjustably, whether accessing same-row or different-row. Even when the two clock inputs have different phases and frequencies, the proposed replica circuit effectively generates internal timings by mimicking the discharge speeds of each bitline (BL) using replica 8T DP bitcells. A prototype of a 256-kbit DP SRAM macro has been implemented in 90 nm logic CMOS technology. Measurement results show that the dynamic power consumption in the cell array is reduced by 16.6% compared to the conventional replica scheme at a typical supply voltage of 1.2 V and room temperature.

key words: *dual-port SRAM, low power consumption, tracking, replica circuit, dummy memory cell, optimization of sense enable signal*

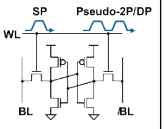
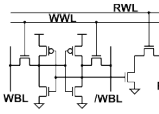
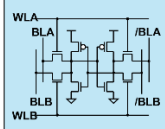
# Clock	1	1 (common)		1 (common) or **2 (individual)**	
# Port	1	2	2	2	**2**
Port config.	SP	pseudo 2P (1R1W)	pseudo DP (2RW)	2P (1R1W)	**DP (2RW)**
Bitcell	6T-SP			8T-2P	**8T-DP**
					
Disturbance free	Yes			No	No
Bit density	High			Middle	Low
Throughput	Low/Middle			High	High

Fig. 1 Several types of embedded SRAMs which are single-port (SP), 1-read/1-write (1R1W) 2-port (2P) and 2-read/write (2RW) dual-port (DP).

1. Introduction

Embedded SRAMs have become increasingly key components in advanced CMOS logic technologies for high-performance and energy efficient computing systems. There are several types of SRAMs as shown in Fig. 1. High-density or high-speed single-port (SP) SRAMs are frequently used in the system-on-chip (SoC) as cache memory operations. Usually the push-ruled dense 6T SRAM bitcells support requirements of total memory capacity increase [1]–[22].

Besides multi-port SRAMs, which can improve memory access throughputs, are also significantly demanded for achieving multi-processing operations in the imaging, graphics, AI and ML applications. In such parallel computing systems, 1-read/1-write (1R1W) 2-port (2P) SRAMs are one of the solutions to meet the requirements of both high-performance and energy efficient [23]–[30]. An 8T-2P bitcell is adopted, being consist of eight transistors including decoupled 2 NMOSs for read port.

In multi-CPUs and many-core architectures [31]–[34], 2-read/write (2RW) dual-port (DP) SRAMs with 8T-DP bitcell are also used as data caches or shared cache memories [35]–[51]. The 2RW DP-SRAM allows simultaneous access for both reading and writing operations from two different ports. This design enables two independent data paths, making it ideal for applications that require high-speed data processing and efficient multitasking. DP SRAMs also function as block RAMs in FPGAs [52] or buffer memories for reconfigurable processors [53], [54].

As listed in Fig. 1, there is capability to support 1R1W 2P-SRAM or 2RW DP SRAM by using 6T-SP bitcell with double pumping operation [56]–[61]. These pseudo macros are able to achieve high-density than 8T-2P or 8T-DP solutions, but there are some challenges to improve the maximum operating frequency (F_{max}) because the operations are sequentially executed twice within 1 clock cycle period. In addition, it is infeasible that more flexible access with independent clock domain for each port, which is required by reconfigurable systems, FPGAs and network processors for the data buffering.

Figure 2 shows the simple system diagrams and operating timing charts in the case of SP SRAM and true 2RW DP SRAM with 8T-DP bitcell [37]. For 2RW DP SRAM, each port can operate independently, meaning one can read/write data between Unit-A while the other read/write data through Unit-B at the same time even when the two clock inputs have different phases or frequencies.

However, the 2RW DP SRAM with 8T-DP bitcell has inherent disturbances when both ports access simultaneously. There are several reports to solve the disturbances by preventing the access conflict [35], [47]. However, those are limited to use a common clock input, meaning a synchronous clock with same or multiplied frequency for both ports. For supporting individual clock input for each port, meaning asynchronous clock inputs, test screening method or improving operating margins by considering disturbances have been reported [36], [37], [41].

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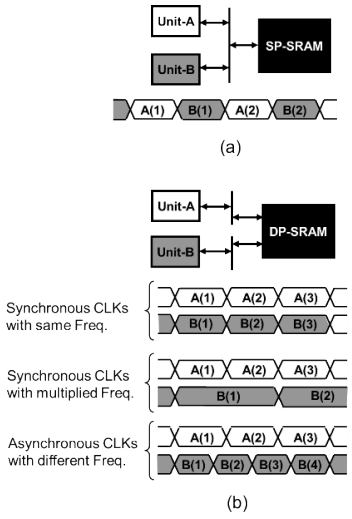


Fig. 2 Memory access diagrams and timing charts: (a) sequential memory access of SP SRAM, (b) parallel memory access of 2RW DP SRAM [37].

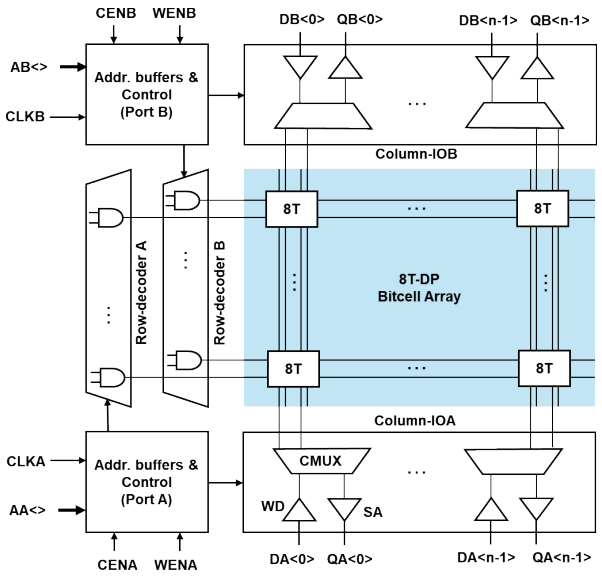


Fig. 3 Block diagram of 2RW DP SRAM macro with individual clock inputs and 8T-DP bitcell array.

Besides, several works have been undertaken for reducing the standby power of 2RW DP SRAM [37], [42], [45], but few studies have particularly addressed dynamic power reduction of 2RW DP SRAMs [47], [50]. To achieve an energy-efficient parallel computing system, dynamic power reduction of 2RW DP SRAM is important along with leakage power reduction. The disturbance aware power reduction scheme for 2RW DP-SRAM with 8T-DP bitcell has been also reported [47] but it is limited for common clock input. In this work, we propose a disturbance aware self-adjustable tracking circuit to improve the energy-efficiency for 2RW 8T DP SRAM macros allowing asynchronous individual clock inputs.

This paper is organized as follows. In Sect. 2, the function of 2RW DP SRAM and its inherent disturbances are described. Then, the motivation of dynamic power reduction is raised. To improve the energy-efficiency, proposed disturbance aware new tracking circuit is presented in Sect. 3. The test chip fabricated in 90 nm CMOS technology and silicon measured data are discussed in Sect. 4, followed by summarizing in Sect. 5.

2. Disturbance in 2RW DP SRAM

2.1 2-Read/Write (2RW) DP SRAM Macro

A 2-read/write dual-port SRAM is a type of memory that allows simultaneous access for both reading and writing operations from two different ports. This design enables two independent data paths, making it ideal for applications that require high-speed data processing and efficient multitasking. Figure 3 depicts a simple block diagram of 2RW DP SRAM macro. There are address buffer and control, row decoder, column-IO block for each port and an 8T-DP bitcell array. Each column-IO block has sense-amplifier (SA) and write-driver (WD) with column multiplexor (CMUX)

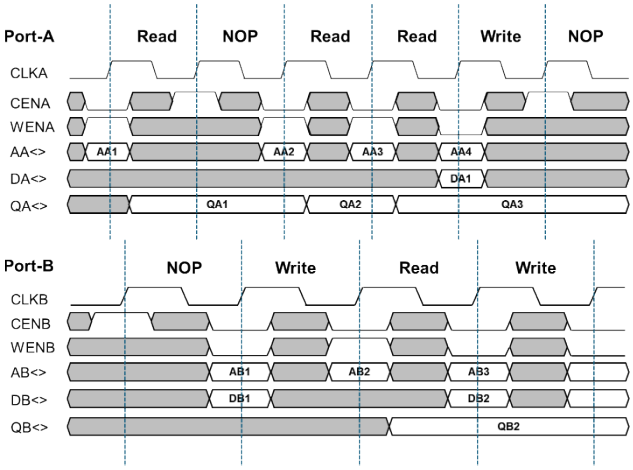


Fig. 4 Timing chart of 2RW DP SRAM macro with asynchronous individual clock input for each port.

for each data bit (0, 1, 2, ... n−1). The AA (AB) and DA/QA (DB/QB), respectively denote address inputs and data inputs/outputs for port A (port B). The CENA (CENB) and WENA (WENB) respectively stand for chip enable and write enable signals. The CLKA (CLKB) stands for the individual clock input for port A (B).

The timing chart is presented in Fig. 4. Both ports are allowed to operate individually with different clock phase and frequency. The reading and writing functions for port A are triggered by rising CLKA edge while those operations for port B are triggered by CLKB. The control signals of the chip enable and write enable are independent for each port. If the CENA (CENB) is "1", the port works as no operation (NOP). If the CENA (CENB) is "0" and the WENA (WENB) is "1", the port works as read operation, otherwise it works as write operation when the WENA (WENB) is "0". Each

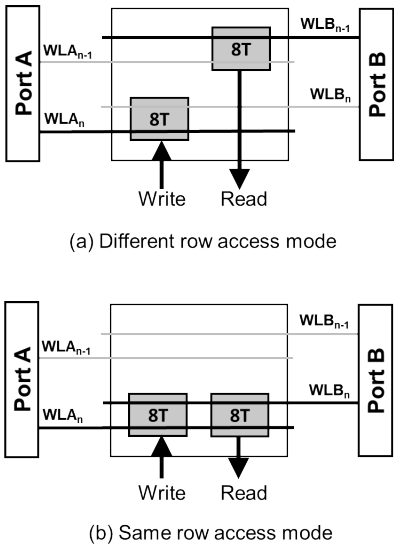


Fig. 5 Two kinds of access modes of DP SRAM: (a) diff.-row access, (b) same-row access [37].

port has its own address inputs, data inputs/outputs, enabling to operate NOP, read or write operation independently.

2.2 Disturbance in 2RW DP SRAM

The memory accesses for 2RW 8T DP-SRAM are mainly classified to modes: one is a different-row (diff.-row) access, the other is a same-row access as illustrated in Fig. 5 [37]. When the same-row access, both WLA and WLB to be accessed 8T-DP bitcell are activated simultaneously, then the disturbance happens. There are two kind of disturbance modes: read-disturbance and write-disturbance. The read-disturbance happens in the read operation at port-A (B) from another port-B (A) when the same-row is selected. The write-disturbance similarly happens in the write operation in port-A (B) from another port-B (A) when the same-row is selected. Note that the access from another port is either read or write operation for both disturbance modes [47].

In this work, we focus on the dynamic read power reduction by self-adjustable tracking circuit which is aware of the read disturbance in 2RW 8T DP SRAM. Figure 6 presents the read disturbance at the same-row address access when both WLA and WLB are activated. In the diff.-row access, the read operation is executed as a single-port 6T SRAM because either WLA or WLB is only activated. Then any disturbance from the other port never happens. In the same-row access, the cell current flows into the pull-down (PD) NMOS from both BLA and BLB in the accessed bitcell. In that case, the read current (I_{read}) of the target BLA through the pass-gate (PG) and PD NMOSs decreases by additional cell current from another BLB. As a result, the discharge speed of BLA decreases.

The read current (I_{read}) on BLA at diff.-row access mode ($I_{\mathrm{readA@diff}}$) is delivered analytically by Eq. (1) reported by [47]. The read current at same-row access mode ($I_{\mathrm{readA@same}}$) is delivered by Eq. (2) as well.

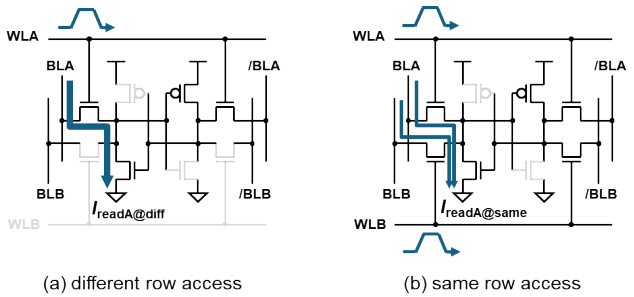


Fig. 6 Read access modes in 8T-DP bitcell: (a) diff.-row access, (b) same-row access.

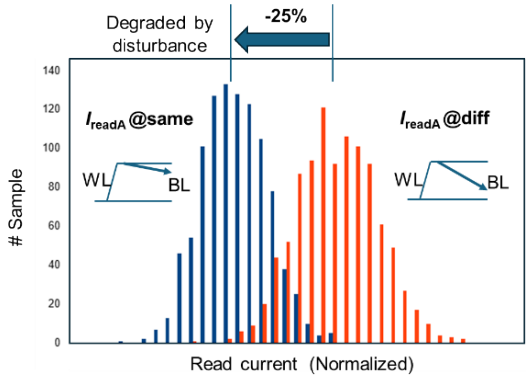


Fig. 7 Monte Carlo simulation results of read currents for 2RW 8T-DP bitcell at diff.-row access and same-row access.

$$I_{\mathrm{readA@diff}} = \frac{1}{2}\beta_{\mathrm{G}}\left(1 - \frac{1}{1+\frac{\beta_{\mathrm{D}}}{\beta_{\mathrm{G}}}}\right)(V_{\mathrm{DD}} - V_{\mathrm{tn}})^2 \tag{1}$$

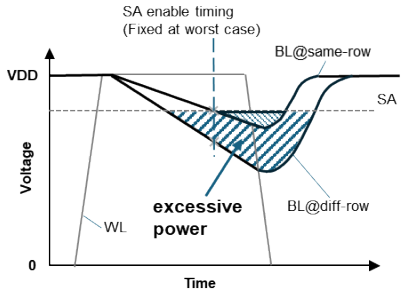
$$I_{\mathrm{readA@same}} = \frac{1}{2}\beta_{\mathrm{G}}\left(1 - \frac{1}{1+2\frac{\beta_{\mathrm{D}}}{\beta_{\mathrm{G}}}}\right)(V_{\mathrm{DD}} - V_{\mathrm{tn}})^2 \tag{2}$$

Here, each β_{G} and β_{D} is the gain factor of PG NMOS and PD NMOS respectively, and V_{tn} is assumed as the same threshold voltage of PG and PD NMOSs. By the Eqs. (1) and (2), the following Eq. (3) is concluded.

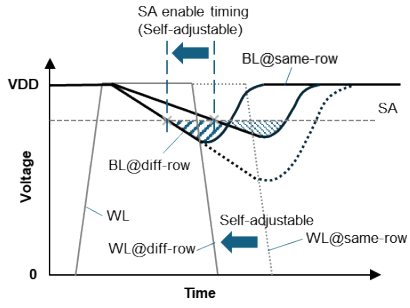
$$I_{\mathrm{readA@diff}} > I_{\mathrm{readA@same}} \tag{3}$$

Using 90 nm CMOS technology, the Monte Carlo simulation for the 2RW 8T-DP bitcell is carried out with 1000 iterations to deliver the distributions of $I_{\mathrm{readA@diff}}$ and $I_{\mathrm{readA@same}}$ with considering random variations. Figure 7 shows the histogram of $I_{\mathrm{readA@diff}}$ and $I_{\mathrm{readA@same}}$ distributions respectively at process-TT, 1.2 V typical supply voltage and 25°C conditions. It is obtained that the difference of mean values of read currents between both access modes is around 25%. The degradation of $I_{\mathrm{readA@same}}$ is due to the disturbance at same-row access.

Figure 8 shows the concept waveforms of read power reduction by self-adjustable tracking. As delivered in Eq. (3), $I_{\mathrm{readA@same}}$ is smaller than $I_{\mathrm{readA@diff}}$, BL swing speed at diff.-row access is faster than that of same-row access. If SE timing and WL disable timing are fixed to the worst condition, these timing have excessive margins at the diff.-row

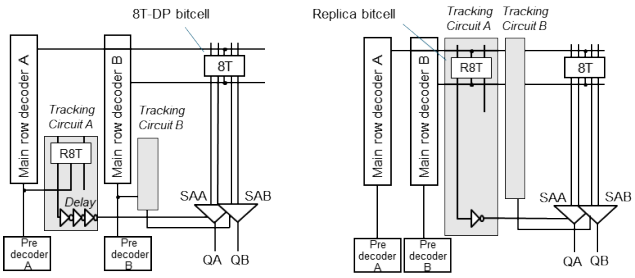


(a) Baseline timing



(a) Proposed timing

Fig. 8 Basic concept of read power reduction by self-adjustable tracking: (a) baseline timing, (b) proposed timing.



(a) Baseline tracking (b) Proposed tracking

Fig. 9 Tracking scheme for 2RW DP SRAM with 8T-DP bitcell (8T) array using a replica 8T-DP bitcell (R8T).

access. In that case, unexpected excessive BL discharging power is consumed as shown in Fig. 8 (a). If the SE timing and WL disable timing can be controlled by detecting whether diff-row or same-row is accessed, the excessive discharging power can be reduced at the diff-row access mode as shown in Fig. 8 (b). By introducing new replica tracking scheme, the disturbance can be detected automatically and the optimum internal critical timing for SE and WL disable are generated self-adjustably. In the next Section, proposed replica tracking circuit is explained in detail.

3. Disturbance Aware Self-Adjustable Tracking Circuit

3.1 Tracking Scheme Using Replica Bitcell

Figure 9 (a) shows a baseline tracking scheme for readout operation of 2RW DP SRAM with 8T-DP bitcell (8T) array using a replica 8T-DP bitcell (R8T). It is simply extended to 2RW 8T DP SRAM design from 6T-SP SRAM designs [62], [63]. The port A (B) has own tracking circuit A (B) without any relationship between both ports. As discussed in Sect. 2, the read current at same-row access is smaller than that of diff.-row access due to the disturbance. However, there is no way to detect whether the accesses from both ports are in the same-row or not. As a result, the sense enable (SE) timing that activates each sense amplifier (SAA/SAB) should be designed as the worst condition under the same-row access even though the diff.-row access can pull-in the SE timing. In addition, the input of baseline tracking circuit is triggered by the pre-decode signal as shown in Fig. 9 (a). In this case, there is undesirable timing mismatch between the main WL and tracking circuit activation timings. Then the buffer chain is required in the tracking output signal (equal to SE timing) to match the delay of the main row decoder.

The delay of buffer chain implemented by logic inverters induces the timing mismatch over the process-volage-temperature (PVT) variations because the MOS characteristics are different between logic CMOSs and pull-up (PU)/PD/PG transistors of the 8T-DP bitcell. It is important to match the 8T-DP bitcell characteristics for generating the critical internal timing. That is why the tracking replica circuits are utilized in resent SRAM designs.

Figure 9 (b) shows the concept of proposed tracking circuit for 2RW DP SRAM. The input of tracking circuit is the same timing of the WL activation. It uses the same replica R8T bitcells but enables to track whether the accesses from both ports are in the same-row or not. In addition, there is no undesirable timing mismatch between the main WL and tracking circuit activation timings. The additional buffer chain is not required.

Figure 10 shows the schematic of the proposed self-adjustable disturbance aware tracking circuit [64]. There are two replica columns which are same layout structures of 8T-DP bitcells. One is tracking for port A and another is tracking for port B. Eight replica R8T bitcells in each column are connected to own tracking wordline (TWLA, TWLB). In each column, two BL pairs run vertical, but only one of the BL (TBLA, TBLB) is used to generate the SE signal. The bitcell structure of replica R8T bitcell is same as that of the 8T bitcell, so that the interconnect capacitance and resistance are identical. To discharge the TBLA (TBLB) every time, however, the data in the replica R8T bitcell is fixed to "L" by modifying slight metal/via layout changes. TBLA (TBLB) reflects the discharge speed of the BLA (BLB) voltage. It makes use of both WLA and WLB pulses in the selected row to generate the SE signal. This indicates that all replica R8T bitcells in replica column are utilized to generate the SE signal. On the other hand, the baseline scheme as shown in Fig. 9 (a) made use of only some localized replica R8T bitcells with dummy 8T (D8T) bitcells (not shown in the figure) in the replica column.

Two tracking-WLs ($TWLA_A$, $TWLA_B$) are controlled by selected WLA and WLB through 1-stacked and 2-stacked PMOS transiters. $TWLA_A$, $TWLA_B$ are expected to mimic

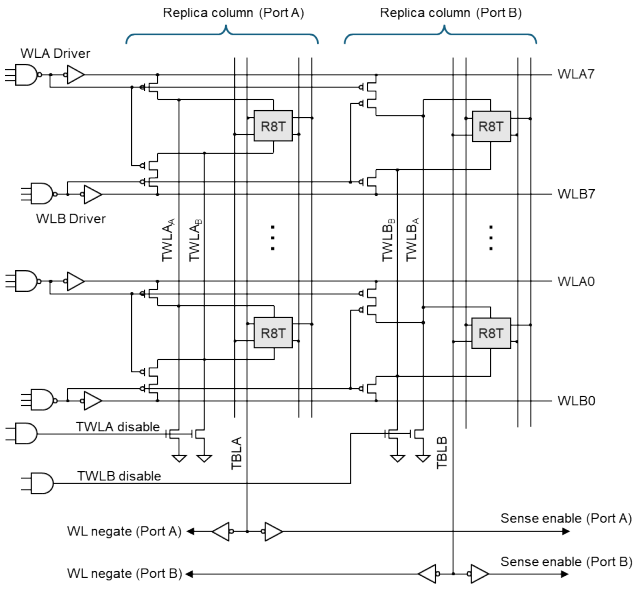


Fig. 10 Proposed self-adjustable disturbance aware tracking circuit.

the same-row access or diff.-row access in the replica column. To generate the optimum timing, the timing delay of TBL should be faster than that of BL in the 8T bitcell array. To enable it, the multiple replica R8T bitcells are activated in parallel. The multiple R8T bitcells also help to reduce the impact of local-Vt variation. Estimated optimum number of multiplications is in the range of 8–16 for 512 × 512 array in 90nm CMOS technology. Then the TWL is commonly connected to eight replica R8T bitcells arranged in the same column direction in our design discussed here after. Of course, the different number can be applied for the proposed tracking circuit if needed.

Figure 11 shows the block diagram of proposed tracking scheme [64]. The replica column for port A and port B are composed every 8 rows between 8T bitcell array and main row decoders with WL drivers. The main row decoder A (B) activates the WLA (WLB) corresponding to the input row address, then the data stored in the accessed 8T bitcell is transferred through the BLA pair (BLB pair). On the same time, a signal from the activated 8 replica bitcells (R8Ts) in the replica column is transferred through the tracking BL labeled as TBLA (TBLB) in Fig. 10. The signal is fed to the Controller A (B) to generate the SEA (SEB) signal for sense amplifier SAA (SAB) and DSA (DSB) signal for WLA (WLB) inactivation. The differential voltage of BLA pair (BLB pair) is latched by SAA (SAB) adequately through column multiplexer (CMUX) and then data is readout to QA (QB). Note that the TBLA and TBLB run vertically and connected to all R8Ts in the replica column. The TWLA (TWLB) disenable signal is to inactivate the tacking WL when the replica column block is not selected or after readout operation done.

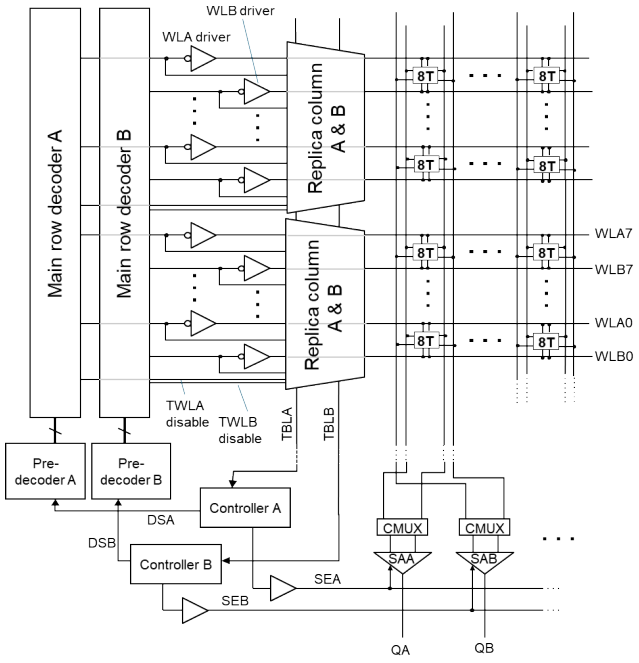


Fig. 11 Block diagram of proposed disturbance aware self-adjustable tracking scheme for 2RW DP SRAM macro [64].

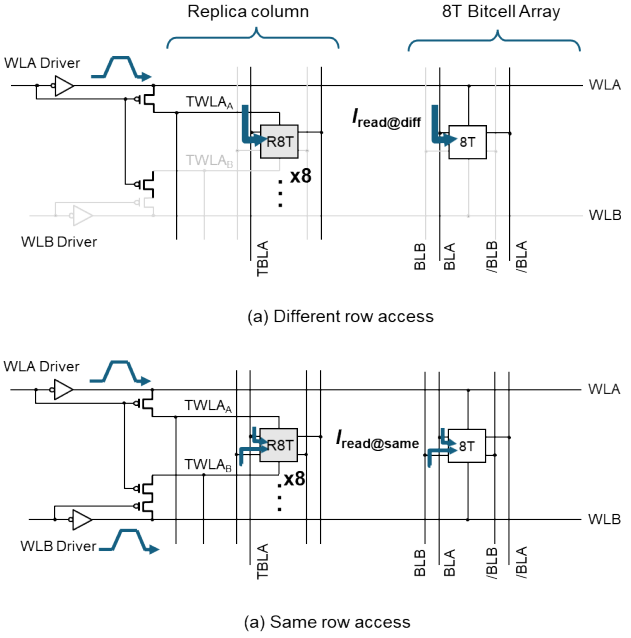


Fig. 12 Self-adjustable tracking operation for port A: (a) diff.-row access mode, (b) same-row access mode.

3.2 Functionality of Proposed Tracking Circuit

Figure 12 represents the self-adjustable tracking operation for port A at the diff./same-row access modes. In the diff.-row access, WLA and $TWLA_A$ are activated at the same timing by turning on the 1-stacked PMOS. The WLB in the same-row is inactivated (selected the other diff.-row),

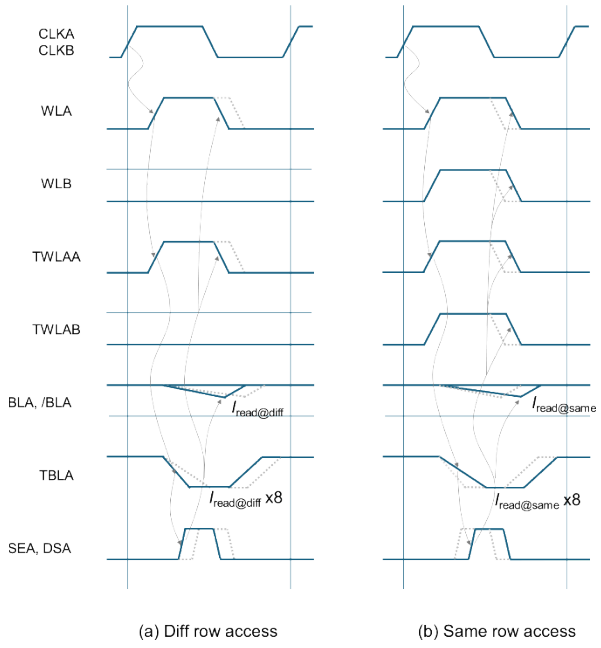


Fig. 13 Timing waveforms of proposed self-adjustable tracking circuit.

$TWLA_B$ is also inactivated because one of the 2-stacked PMOS is still turning off. Then 8x $I_{readA@diff}$ flows in the TBLA because the eight R-8Ts are connected to $TWLA_A$ commonly in the replica column A. Consequently, the discharging speed of TBLA is 8x faster than that of each BLA, making an appropriate SEA timing and DSA timing for WLA inactivation under the diff.-row access mode. In the same-row access, WLA and $TWLA_A$ are activated almost same timing and WLB and $TWLA_B$ are similarly activated same timing. As a result, 8x $I_{readA@same}$ flows through the TBLA as the same-row access mode. The timing waveforms are shown in Fig. 13. The port A tracking operation is described here, the equivalent tracking operation for port B is executed by the other replica column B.

3.3 SPICE Simulation Result

Figure 14 shows the SPICE simulation waveforms of the BLs and WLs at diff./same-row access modes. Different timings of SE signals are generated in accordance with the discharge speed of the BLs. Here the target differential voltage of SA is set to 200 mV at 1.2 V and 25°C. The simulation result show that the WL pulse width at diff.-row access is shorter than that of same-row access. This indicates that SE timing is self-adjustably generated by the tracking circuit. If the timing is not aware the row access mode, the excessive BL swing appears due to the same timing at worst condition which is equal to same-row-access mode. By proposed disturbance aware self-adjustable tracking circuit, it can be cut off by pulling-in the WL inactivating timing. Therefore, dynamic power in read operation at diff.-row access mode is effectively reduced.

The proposed tracking circuit is effective for individual clock inputs with different phase or frequency. Figure 15 shows the SPICE simulation result of the average read current variation by sweeping the CLKA and CLKB input phases. Both read currents flowing BLA in the cell array and TBLA in the replica column are varied with the same percentages along with the overlap period of both WLA and WLB activations. The simulation result shows the average read currents in both 8TDP bitcell and replica R8T bitcells degrade by 27% at the peak when the WLA and WLB are exactly activated simultaneously. By pulling-in the WL inactivation timing with the proposed self-adjustable circuit, the excessive read dynamic power can be reduced as discussed in Sect. 2.

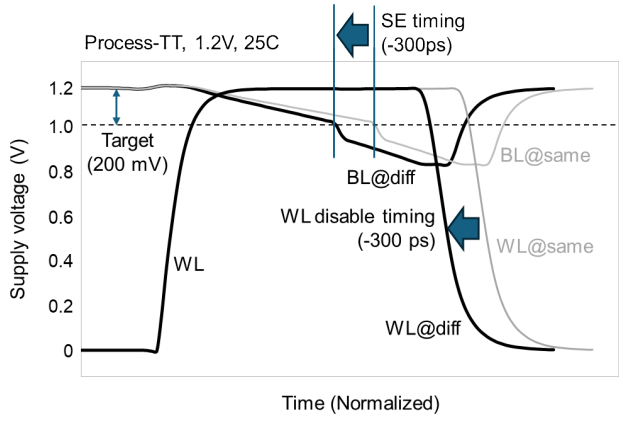


Fig. 14 SPICE simulation waveform for read operation.

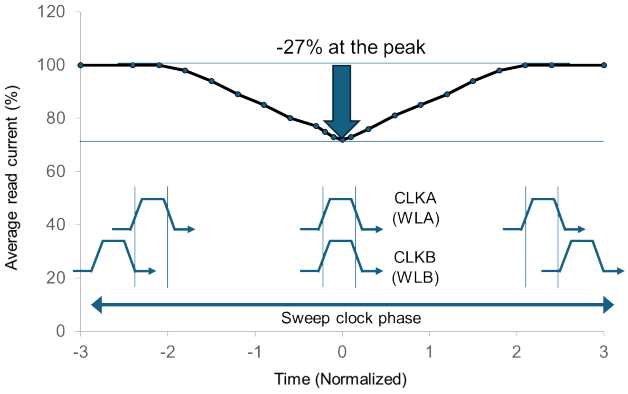


Fig. 15 SPICE simulation result of the read current variation depending on CLKA and CLKB input phases.

4. Test-chip Design and Fabrication

4.1 Implementation of 2RW DP SRAM Macro

We designed and fabricated a test chip using 90 nm CMOS technology with 5-Cu metals. Figure 16 illustrate the layout of the logic-ruled 8T-DP bitcell up to the first metal layer. The cell size is 2.94 um^2 with balanced symmetrical layout. It is 1.44x larger than the dense push-ruled 8T-DP bitcell and 2.35x larger than the dense push-ruled 6T-SP bitcell [50]. The BLs run vertically in the 2^{nd} metal layer while WLs run horizontally with 3^{rd} metal layer. The BL

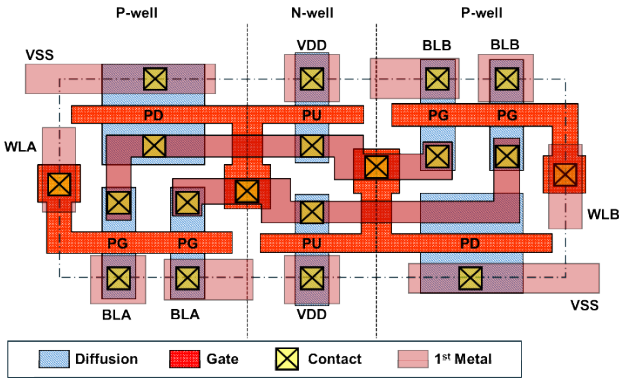


Fig. 16 Layout plot of logic-rule based 8T-DP bitcell.

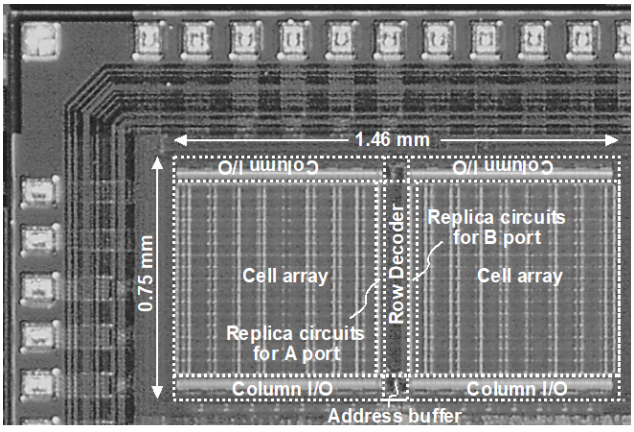


Fig. 17 Photograph of the implemented 256-kbit DP SRAM macro.

Table 1 Test chip features.

Technology	90-nm logic CMOS
SRAM type	2-Read/Write 8T Dual-port SRAM
Bitcell size	2.58 um x 1.14 um (2.94 um^2)
Bit-word config.	16-bit x 16-kword
Array size	512-row x 512-column
Column MUX	32
Macro capacity	256-kbit
Macro size	1.46 x 0.75 mm^2
Density	234-kbit/mm^2

coupling noise between each port is isolated by VDD shield in the center location. Figure 17 portrays a photograph of the implemented 256-kbit DP SRAM macro. 512-row by 512-column size is divided into two cell arrays by center placed row decoders. Note that the proposed tracking circuits are physically placed on both sides next to the center row decoders. The area overhead of the tracking circuits is less than 2% of the macro. Table 1 summarizes the features of implemented 256-kbit 2RW DP SRAM macros in 90-nm CMOS logic technology.

4.2 Silicon Measurements

Figure 18 shows the measured typical shmoo plot of read access time over supply voltage at 25°C. The area marked

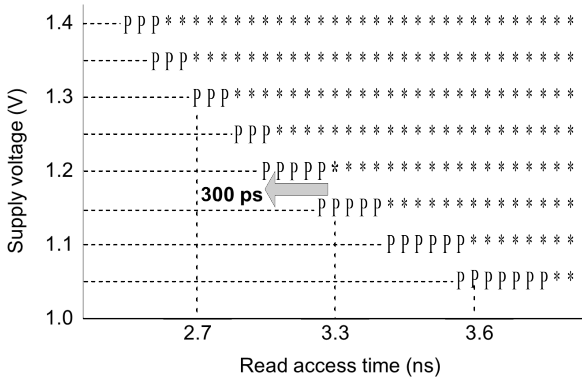


Fig. 18 Measured shmoo plot for read access time vs supply voltage at room temperature.

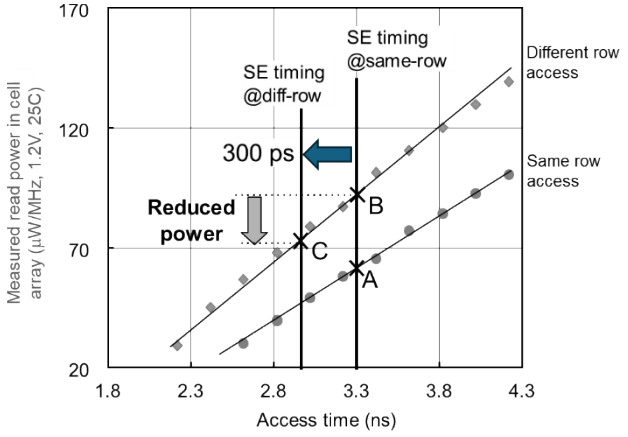


Fig. 19 Relationship between access time and dynamic read power in the 512 × 512 cell array.

with (*) shows passes at both same-row access and diff.-row access. The area marked with (p) shows the additional passes at diff.-row access mode. The read access time of diff.-row access is 300 ps faster than that of same-row access. This result shows that the proposed tracking circuit can self-adjustably generate the appropriate SE and WL negating timings being aware of the diff./same-row access modes.

In the prototype macro design, the SE signal can be arbitrarily controlled by an external test signal under the testing mode. We measured dynamic read power consumption by sweeping the SE timing. Figure 19 shows the relationship between the read access time and the power consumption of the BL discharge. The horizontal axis represents the read access time, which is equivalent to that in Fig. 18. The vertical axis represents the dynamic power consumption of the BL discharge. Considering that the BL discharge decreases linearly, the power dissipation increases linearly as the SE timing increases. Point A represents the power consumed in the same-row access. Point B indicates the power dissipation in diff.-row access if the baseline tracking scheme is applied. The faster SE signal is obtained for the diff.-row access, so that the power consumed in our scheme is represented by C. By comparing C with B, we achieved a 16.6% power

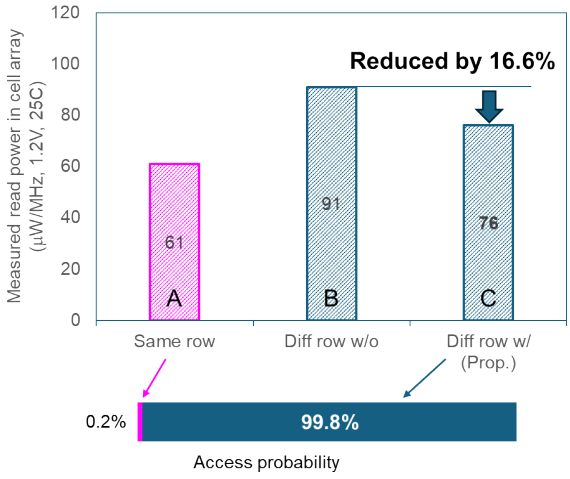


Fig. 20 Measured dynamic read power in the 512 × 512 cell array.

reduction in the BL discharge.

The read dynamic power comparison is summarized in Fig. 20. If the row address is accessed randomly, the probability of occurrence of the same-row access is 1/row. It is only 0.2% in the 512-row array. Although a small probability of the same-row access exists, the same-row access should be regarded as a worst condition for maintaining the design margin. By introducing proposed tracking circuit, 99.8% read operation can be reduced excessive read power consumption by 16.6% with keeping the worst same-row access timing margin.

5. Conclusions

A disturbance aware self-adjustable replica tracing circuit is proposed for the embedded 2RW dual-port SRAM. It is to generate internal critical timings by each replica circuit which generates appropriate internal delays self-adjustably in accordance with the same-row or different-row accesses. The proposed replica circuit effectively generates the internal timings by being mimic each BL discharge speed with replica 8T DP bitcells. As a result, it is applicable even if the two clock inputs for port-A and port-B are different phases and frequencies individually. A prototype 256-kbit DP SRAM macro is implemented in 90 nm logic CMOS technology. The measurement silicon data shows that the dynamic read power consumption in the cell-array is reduced by 16.6% compared to the conventional baseline tracking scheme at 1.2 V typical supply voltage and 25°C.

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