PAPER

Measuring SET Pulse Widths in pMOSFETs and nMOSFETs Separately by Heavy-ion and Neutron Irradiation

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SUMMARY Radiation-induced temporal errors become a significant issue for circuit reliability. We measured the pulse widths of radiation-induced single event transients (SETs) from pMOSFETs and nMOSFETs separately. Test results show that heavy-ion induced SET rates of nMOSFETs were twice as high as those of pMOSFETs and that neutron-induced SETs occurred only in nMOSFETs. It was confirmed that the SET distribution from inverter chains can be estimated using the SET distribution from pMOSFETs and nMOSFETs by considering the difference in load capacitance of the measurement circuits.

key words: *Single Event Transient, Pulse Width, Heavy Ion, High Energy Neutron*

1. Introduction

Single event effects are one of a significant issue for circuit reliability since they transiently flip the output of transistor, resulting in circuit malfunction. This malfunction is called soft error [1]–[4]. Single event effects are caused by a charged particle. A charged particle generates electron-hole pairs in semiconductor along its track and the generated electrons are collected to the diffusion region of off-state nMOSFET by the electric field in the depletion layer. Thereby, the output of the off-state nMOSFET is flipped transiently. When a charged particle passes through a logic circuit, its output is inverted for a time depending on the amount of collected charge, which is called single event transient (SET). When a charged particle passes through a storage element, its stored data can be flipped by collected charge, which is called single event upset (SEU). The SEU is more critical to the circuit reliability because incorrect outputs due to SET can only lead to malfunctions when they are captured by flip-flops (FFs). However, SET is more frequently captured by FFs as the clock frequency increases [5], [6]. Therefore, in advanced technology, measuring SET rates and their pulse widths has become important for calculating the soft error rate and estimating the reduction of error rate by low-pass filters [7], [8]. Furthermore, measuring the SET pulse width distribution can be used to evaluate the distribution of the amount of collected charge generated by radiation strike, since the SET pulse width depends on the amount of collected charge.

Previous researches on SETs have reported numerous characteristics, such as temperature characteristics, dependence on well contact density, driving strength and logic circuit structure [9]–[14]. However, most of these studies measured SET pulse widths using CMOS inverter chains. Hence, it is impossible to determine whether the measured SET was generated from an nMOSFET or a pMOSFET. Since the electrons and holes generated by a radiation strike are collected by nMOSFETs and pMOSFETs, respectively, the SETs produced in nMOSFETs can have different characteristics from those in pMOSFETs. Therefore, separated measurement of SETs from nMOSFETs and from pMOSFETs is important to obtain detailed characteristics of single event transients. To address the above problem, S. Jagannathan et al. measured SET pulse widths from nMOSFET and pMOSFET using partially-duplicated logic chains [12]. Their results showed that pMOSFET had 3.9 times more SETs than nMOSFET. However, only a few reports have measured SET pulse widths using this method.

In addition to a lack of distinction between SETs from nMOSFET and pMOSFET, there were issues with the measurement accuracy of SET pulse width [15]–[17]. SET pulse width can be modulated during propagation through logic gates since SET pulse widths are generally measured using a long logic chain [18]. This propagation-induced pulse modulation (shrinking / broadening) is caused by the difference between the rise and fall propagation times. Thus, the target logic structures need to be considered to achieve high measurement accuracy of SET pulse widths. Additionally, it is crucial to measure the same SET characteristics using different measurement circuits in order to verify the SET characteristics that depend on specific circuit structures.

In this paper, SET pulses widths from nMOSFET (nSET pulse widths) and pMOSFET (pSET pulse widths) were measured to separate single event effects on nMOSFET and pMOSFET. We show that the impact of single-event effects is different for nMOSFETs and pMOSFETs by performing the above measurements, indicating that separate measurements are essential for accurate SET modeling and estimating the soft error rate of a circuit. In addition, we clarify the effects of the differences in the measurement circuits by comparing the measurement results of nSETs and pSETs with SET pulse widths measured by the conventional method using inverter chains. The rest of this paper is organized as follows. Section 2 introduces structures of Target logic circuits and time-to-digital converter. The measurement results by Kr ions and neutron irradiation are shown in Section 3. We conclude this paper in Section 4.

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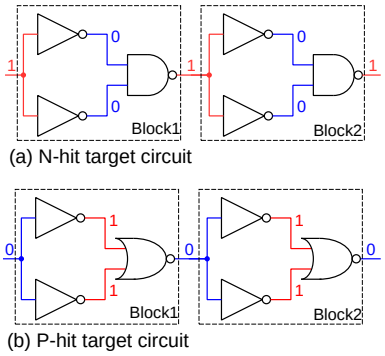

Fig. 1 Schematics of two of the blocks of (a) N-hit target circuit and (b) P-hit target circuit proposed by S. Jagannathan et al [12].

2. SET Pulse Width Measurement Structures

2.1 Conventional Measurement Structures

Typically, SET pulse widths are measured by a logic gate chain and a time-to-digital converter (TDC) such as vernier delay line [19], [20]. When a SET pulse is generated by radiation passing through one logic gate, the SET propagates through the logic gate chain and is input to the TDC. Thus, SET pulse width can be measured by storing the SET pulse width as a digital signal. The more the number of stages in the logic gate chain under measurement, the more area-efficient the measurement can achieve.

Fig. 1 shows target logic chains to measure nSET and pSET separately, which was proposed by S. Jagannathan et al. Since the inverters are duplicated, a SET generated on the inverters does not change output of NOR gate or NAND gate. Thereby, SETs generated on off-state nMOSFETs in NAND gates are only measured by the N-hit target circuit, and we can measure nSETs and pSETs separately.

SET pulse width measurement using a logic gate chain has a problem due to propagation-induced pulse modulation (PIPM) effect [15]. Because of the difference in propagation delay time of the logic circuit between rising and falling signals, the pulse width increases or decreases linearly as the SET pulse passes through the logic circuit. Thus, the SET pulse width depends on the position in the logic gate chain through which the radiation passes. PIPM effects can occur even in inverter chains due to negative bias temperature instability (NBTI) [17], and it is particularly significant in logic circuits with different even and odd numbered stages, as in the block in Fig. 1. To reduce the PIPM effect, short logic gate chains connected to the inputs of a multi-input OR gate are used for the measurement target.

2.2 Target Structures

SET pulse width measurement circuits were implemented in a 65 nm bulk process. Their simplified schematic is shown in Fig. 2. It consists of 27 unit circuits as the SET source,

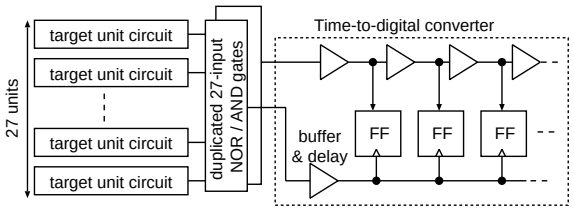

Fig. 2 Simplified schematic diagram of SET pulse width measurement circuit.

duplicated 27-input NOR (or AND) gates and a time-to-digital converter (TDC). In this circuit, the output inversion of an unit circuit caused by a SET is transmitted to inputs of the TDC by the 27-input NOR gates, and the pulse width is saved as a digital signal by the TDC.

Fig. 3 shows the target unit structures used to measure nSET widths, pSET widths and SET widths from the inverters. Fig. 3 (a) and (b) are based on victim circuit structures reported in Ref. [21]. The structure for nSET was composed of one on-state pMOSFET and 30 off-state nMOSFETs connected in parallel. In this structure, only SET pulses from nMOSFETs were measured because single event effect is caused on off-state MOSFETs. Additionally, the SET pulse width does not change unintentionally by PIPM effect, therefore, SET pulse widths from nMOSFET and pMOSFET can be measured accurately and individually using the unit structures as shown in Fig. 3 (a) and (b). Furthermore, all target unit structures contain an equal number of off-state MOSFETs, so the area efficiency of the measurement circuit does not decrease when nSETs and pSETs are measured separately.

The SETs from the inverter chain (SET_{inv}) cannot separate nSETs and pSETs because the inverter chain contains 15 off-state pMOSFETs and 15 off-state nMOSFETs. SET_{inv} were measured for comparison with SETs calculated using nSETs and pSETs obtained from the circuits in Fig. 3 (a) and (b), respectively.

Fig. 4 shows the structure of the 27-input NOR gate. It consists of 3-input NOR gates and 3-input NAND gates to reduce fanout less than four.

2.3 Time-to-digital Converter

The TDC was implemented based on a snapshot circuit introduced in Ref. [11]. Fig. 5 shows a detailed schematic diagram of the implemented TDC. Fig. 6 shows timing chart of the TDC when a SET is simultaneously input to the two input ports, PULSE_IN and TRIG_IN. Input pulse width can be calculated by multiplying the delay time of the buffer and the number of positive-edge triggered FFs that capture flipped output values of the buffers. Measured SET pulse width is stored in the FFs as a sequence of '0'.

The TDC has two input ports to measure pulse width, PULSE_IN is for the input of the pulse to be measured, and TRIG_IN is used as a trigger to save the output values of the buffers. The pulse width is not stored unless the SET pulse is simultaneously propagated to the two input ports.

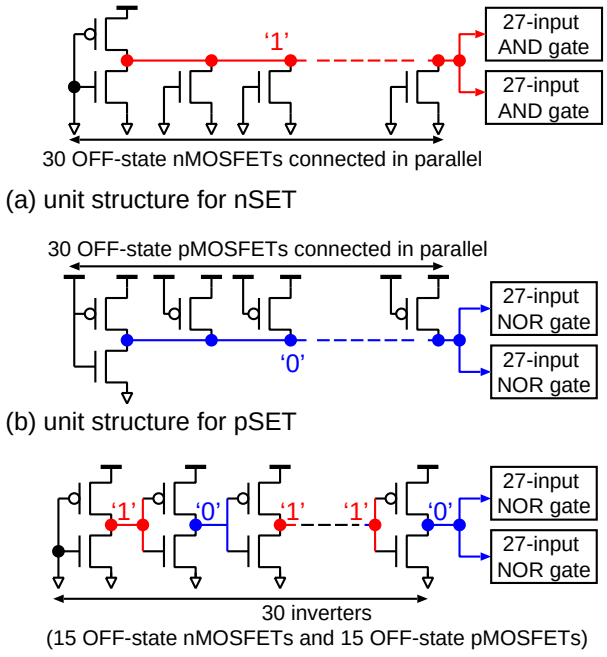

Fig. 3 Schematic diagrams of target unit circuits.

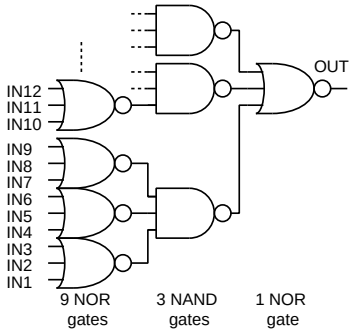

Fig. 4 The structure of the implemented 27-input NOR gate.

Therefore, SETs caused in the TDC and the 27-input NOR / AND gates were not captured by FFs, and SETs caused in the target unit circuits are only measured and stored by the TDC. Therefore, the TDC does not need to be duplicated and achieves better area efficiency than conventional TDCs for SET pulse width measurement.

2.4 Fabricated Test Chip

150 SET pulse width measurement circuits were implemented in a 65 nm twin-well bulk process. We implemented single-finger (1x) and two-finger (2x) transistors versions of the three circuits shown in Fig. 3 as the evaluation targets. Two-finger transistors duplicate on-current, while the drain area is quite similar to that of a single-finger transistor. The gate widths of the nMOSFETs and pMOSFETs in Fig. 3 (a) - (c) are 390 nm and 520 nm per finger, respectively. The gate width ratio between pMOSFETs and nMOSFETs is 1.33,

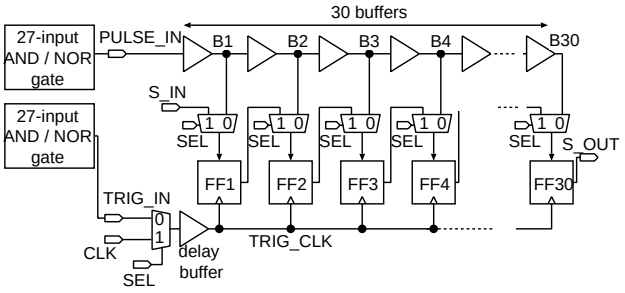

Fig. 5 Detailed schematic diagram of the implemented TDC. 31 multiplexers are inserted to perform 30 stage shift register which is used to initialize the TDC and to read the measurement.

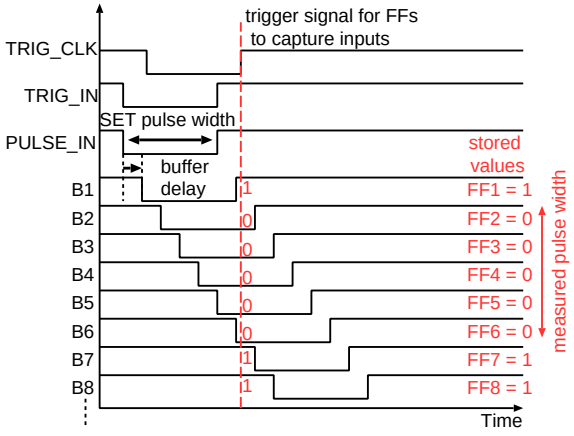

Fig. 6 Timing chart of the TDC when a SET is simultaneously input to the two input ports, PULSE_IN and TRIG_IN. The delay time of the multiplexers and the setup time of the FFs are ignored in this timing chart.

which is determined by optimizing the delay time and area in the standard cell library [22].

The simplified layouts of the implemented target circuits are partially shown in Fig. 7. Since there are 30 off-state MOSFETs in Fig. 3 (a) and (b), it is possible that a charged particle may affect multiple off-state MOSFETs at the same time. This phenomenon is called charge sharing or multiple-node charge collection [23]. Charge collection in multiple MOSFET connected in parallel can increase the SET pulse width significantly, making it impossible to measure SET pulse widths from a MOSFET. To mitigate this problem, only two off-state MOSFETs in the unit circuit were placed in the same well and an array of well-contacts were inserted between them to suppress multiple-node charge collection and parasitic bipolar effect. Additionally, the unit circuits are placed 1 μm from each other to avoid charge sharing between the two unit circuits and to prevent two SET pulses from occurring simultaneously [24].

Fig. 8 shows calibration results of the fabricated TDCs in different chips by inputting square wave from a variable-stage ring oscillator and frequency divider circuit. The generated square wave was input to first stage of a 30-stage inverter chain. In this calibration, it was not possible to check the TDC operation using pulses of under 600 ps. However,

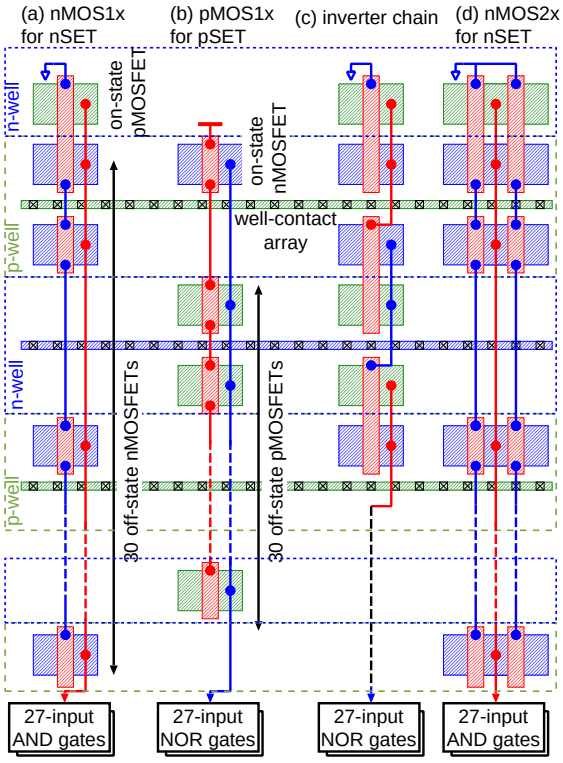

Fig. 7 Simplified layouts of target unit structures: (a) unit structure for nSET with one finger, (b) unit structure for pSET with one finger, (c) inverter chain with one finger and (d) unit structure for nSET with two fingers.

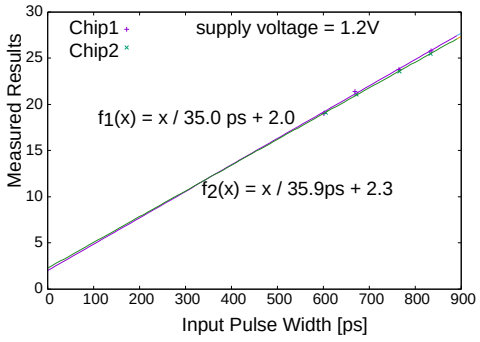

Fig. 8 Calibration results of the implemented TDCs.

resolution of the TDC determined by the delay time of the 30 buffers which does not differ significantly from buffer to buffer. Moreover, the calibration results agreed well with circuit-level simulation results. The resolution of the TDCs was about 35 ps when supply voltage was 1.2 V, which is less than 10% error from the value obtained by the circuit-level simulation. Therefore, we estimate that the TDC maintains a resolution of 35 ps even with input pulses below 600 ps.

3. Experiment Results

3.1 Experiment Setup

Heavy ion tests were performed at Cyclotron and Radioisotope Center (CYRIC), Tohoku University, Japan. The chip was irradiated perpendicularly with $^{84}Kr^{17+}$. The energy and linear energy transfer (LET) values of the Kr ions are 322 MeV and 40 MeVcm^2/mg. Total fluence of the Kr ions was about 8,000,000 ions/cm^2.

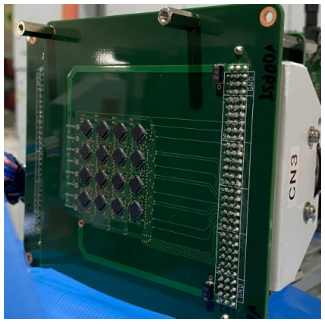

Fig. 9 Simultaneous measurement of 32 test chips using two PCB boards in the neutron irradiation test.

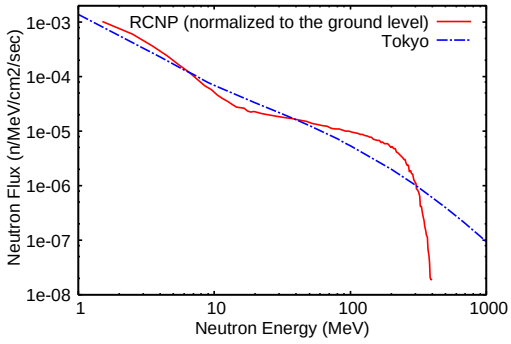

Fig. 10 Neutron spectrum at Tokyo and that from spallation neutron source at RCNP.

The flux of heavy ions varies greatly with position in space. Therefore, the probability of heavy-ion-induced SETs is generally expressed using the cross-section (CS) calculated from the following equation [25].

$$CS[\mathrm{cm}^2/\mathrm{target}] = \frac{\mathrm{N_{SET}}}{\mathrm{F_{ION}} \times \mathrm{N_{target}}}, \quad (1)$$

where, N_{SET} is the number of measured SETs, F_{ION} is ion fluence per cm^2, N_{target} is the number of measurement target (off-state nMOSFETs, pMOSFETs or inverters).

High energy neutron tests using spallation neutron source were performed at Research Center for Nuclear Physics (RCNP), Osaka University, Japan. Fig. 10 shows neutron spectrum at Tokyo and that from spallation neutron source at RCNP. In order to observe as many SET pulses as possible, two test boards with 16 chips each (32 in total) were measured simultaneously (Fig. 9). Chips were tested to a total fluence of 5×10^9 n/cm^2, which is equivalent to the total fluence of neutrons in 400,000 years at ground level (terrestrial neutron flux = 12.9 n/cm^2/hr [26]). The probability of neutron-induced SETs is expressed using failure in time (FIT) rate. FIT rate is the number of SETs that can be expected in 10^9 hours.

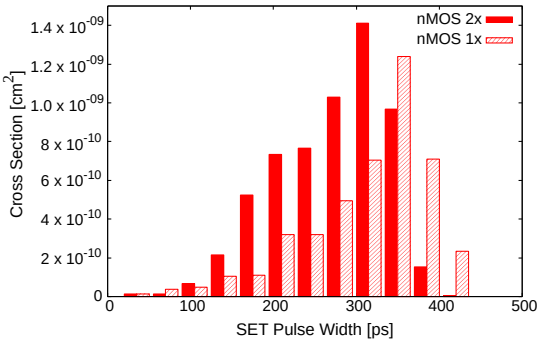

Fig. 11 Distribution of nSET pulse widths by Kr-ion irradiation.

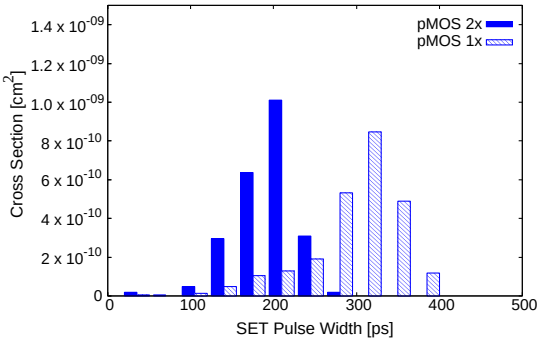

Fig. 12 Distribution of pSET pulse widths by Kr-ion irradiation.

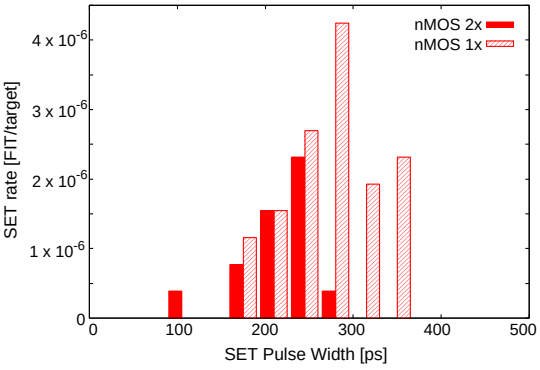

Fig. 13 Distribution of nSET pulse widths by neutron irradiation.

3.2 SET Pulse Widths from pMOSFET and nMOSFET

Figs. 11, 12 and 13 show the pulse width distributions of Kr-ion-induced nSET, Kr-ion-induced pSET and neutron-induced nSET, respectively. Since pSET was not induced by neutron tests, only the distribution of nSET pulse widths is shown in Fig. 13. Total number of SETs, total probability of SETs and average SET pulse width are summarized in Tables 1 and 2.

SETs from off-state nMOSFET have larger CS and longer average pulse width than those from off-state pMOSFET. Additionally, there were no pSET events during the neutron tests. These results are due to differences in electron and hole mobility. The electrons that are collected in the off-state nMOSFET had higher mobility than holes, and more charge is collected in the nMOSFET diffusion region. Furthermore, pMOSFET on-current is smaller than nMOSFET on-current in the measured structures. Thus, longer SETs were more frequently generated from nMOSFETs than from pMOSFETs. The nSETs have a greater impact on circuit reliability than the pSETs, at least when the transistor sizes evaluated in this paper are used in standard cells.

The nSETs and pSETs also have different degrees of dependence on the number of fingers (drive strength). In the Kr-ion tests, increasing the number of fingers reduced the pulse widths of the nSETs and pSETs by 10% and 40%, respectively. It is assumed that the pulse widths of pSETs are reduced by the on-current from nMOSFETs, which doubles with the increase in the number of fingers. In the case of nSETs, the increase in the number of fingers also doubles the on-current from pMOSFETs, but we assume that twice the number of off-state nMOSFETs increases the amount of radiation-induced parasitic bipolar current, so that the effect of twice the on-current from pMOSFETs become smaller [10]. These results are consistent with the fact that the current amplification factor of a lateral npn bipolar transistor is greater than that of a lateral pnp bipolar transistor in the 65 nm process design kit. Based on the above measurements, separate measurements of nSET and pSET are essential in SET modeling because the characteristics of nSET and pSET are different.

In a previous study, pSETs were reported to be approximately 3.9 times higher than nSETs [12], however, this is not consistent with our results. We assume that this is due to the difference in the gate width of the pMOSFETs. In Ref. [12], the gate widths of sensitive pMOSFET and nMOSFET were 1.3 μm and 400 nm, respectively, while, in our target circuits they were 520 nm and 390 nm. There is more than twice the difference in the gate width of the pMOSFETs.

In this experiment, we also measured the single event upset (SEU) rates on standard FFs using Kr ions and neutrons. The CS of Kr-ion-induced SEU rate was 1.50 $\times 10^{-8}$cm^2/FF and the neutron-induced SEU rate was 5 $\times$ 10^{-4} FIT/FF. Neutron-induced SET rate was about two order of magnitude lower than the SEU rate. In contrast, CS of Kr-ion-induced SET was 1/6 – 1/4 of the SEU rate, which is a significant ratio since combinational circuits are basically composed of a large number of logic circuits. SET protection is also necessary in space where heavy ions exist. As can be inferred from the SEU rates on standard FFs, 851 and 533 SEUs on FFs in the TDC were also observed in the accelerated tests with neutrons and Kr ions, respectively. However, as shown in the calibration results (Fig. 8), SET measurement data is always stored in the FFs as three or more consecutive zeros, making it easily distinguishable from the SEUs.

3.3 nSET and pSETs versus SETs from Inverter Chains

SETs from a 30-stage inverter chain (Fig.3(c)) occur in 15 off-state nMOSFETs and 15 off-state pMOSFETs. Therefore,

Table 1 Measurement results of SET pulses by Kr-ions irradiation.

target	finger	total number of SETs	total CS of SETs [cm^2/target]	avg. SET width [ps]
nMOSFET	2x	956	5.9×10^{-9}	270
	1x	703	4.3×10^{-9}	310
pMOSFET	2x	382	2.4×10^{-9}	190
	1x	404	2.5×10^{-9}	300

Table 2 Measurement results of SET pulses by neutron irradiation.

target	finger	total number of SETs	total SET rate [FIT/target]	avg. SET width [ps]
nMOSFET	2x	14	5.4×10^{-6}	150
	1x	36	1.4×10^{-5}	200
pMOSFET	2x	0	–	–
	1x	0	–	–

Table 3 Measurement and calculated results of Kr-ion-induced SETs from inverters.

	finger	total number of SETs	total CS of SETs [cm^2/target]	avg. SET width [ps]
measured SET_{inv}	2x	725	4.5×10^{-9}	180
	1x	711	4.4×10^{-9}	160
calculated SET_{inv}	2x	–	4.2×10^{-9}	250
	1x	–	3.4×10^{-9}	310

Table 4 Measurement and calculated results of neutron-induced SETs from inverters.

	finger	total number of SETs	total SET rate [FIT/target]	avg. SET width [ps]
measured SET_{inv}	2x	4	1.5×10^{-6}	40
	1x	13	5.0×10^{-6}	80
calculated SET_{inv}	2x	–	2.7×10^{-6}	150
	1x	–	7.0×10^{-6}	200

the SET cross section and error probability of the inverter chain, CS_{inv} and P_{inv} can be calculated from the following equations.

$$CS_{\mathrm{inv}} = \frac{CS_{\mathrm{pSET}} + CS_{\mathrm{nSET}}}{2}, \tag{2}$$

$$P_{\mathrm{inv}} = \frac{P_{\mathrm{pSET}} + P_{\mathrm{nSET}}}{2}. \tag{3}$$

In this section, we compare measured SETs from the inverter chain and SETs calculated from the measurement results of nSET and pSETs.

The measured and calculated SET rates in inverter chain are summarized in Tables 3 and 4. For both neutron and heavy ion tests, the average SET_{inv} pulse widths were about 100 ps shorter than the average SET_{inv} pulse width calculated by nSET and pSET. There are two possible reasons for this: one is the difference in load capacitance, and the other is multiple node charge collection in the inverter chain. In the nSETs and pSETs measurement circuits, 30 off-state MOSFETs provided a large junction capacitance and load capacitance are several times larger than those in the inverter chain. Thereby, the recovery speed from radiation-induced inversion became slower. The voltage variation due to an ion strike is also slower due to the large load capacitance.

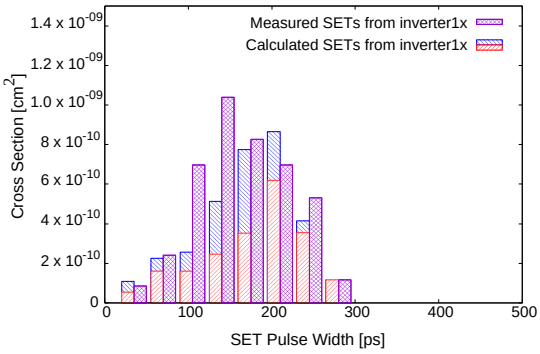

Fig. 14 Measured and calculated distribution of SET pulse widths from inverter 1x. Red and blue bars represent nSET and pSET, respectively.

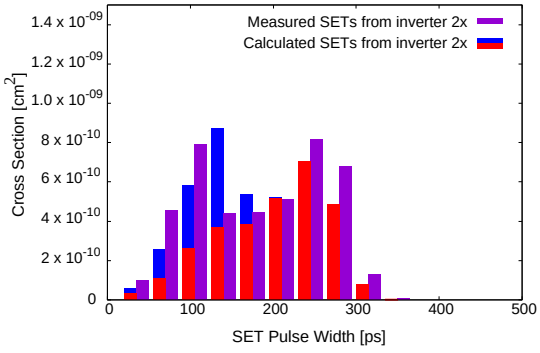

Fig. 15 Measured and calculated distribution of SET pulse widths from inverter 2x. Red and blue bars represent nSET and pSET, respectively.

However, compared to the increase in recovery time, the time increase in radiation-induced voltage change is relatively small since the drift current due to a radiation strike has a large peak value [27], [28]. In addition, the drift is effective for a longer time due to the large load capacitance, and more significant charges are collected. As a result, longer SET pulses were more likely to occur in the nSETs and pSETs experiment circuits. Another reason could be pulse quenching, which is a reduction of SET pulse widths in the inverter chains due to multiple node charge collection [29]–[31]. Pulse quenching is caused by charge collecting in the on-state MOSFETs and the collected charge suppresses the inversion time (SET pulse width). Additionally, since the charge generated by radiation strikes change the well potential, it increases the on-current of the MOSFET as a forward body bias. Thus, the recovery speed increases from the SET inversion and the SET pulse width shortens. These effects are less likely to occur in nSETs and pSETs measurement circuits because there are only one on-state MOSFET and it is separated from most of the off-state MOSFETs (Fig. 7).

Measured and calculated distributions of the Kr-ion-induced SET_{inv} pulse widths are shown in Figs. 14 and 15. The distributions calculated by nSETs and pSETs were adjusted by subtracting the difference in average pulse widths to consider the effects described above. The calculated pulse width distributions were consistent with the measurement results using the inverter chain. In particular, the calculated

distribution reproduced the measurement result of two-finger transistors that had two peaks: the peak around 100 ps is composed of nSETs and pSETs , while the other peak is composed of only nSETs (Fig. 15). The above results indicate that the proposed nSET and pSET measurement circuits can be used to analyze SET in inverters. For more accurate measurement, use a circuit that matches the load capacitance of the inverter chain and to consider multiple node charge collection in the inverter chain.

4. Conclusion

SET pulse widths for pMOSFETs were measured separately from those for nMOSFETs in a 65 nm bulk process using off-state pMOSFETs or nMOSFETs connected in parallel. Measurement results show that nMOSFETs had twice the the heavy-ion-induced SET rate as pMOSFETs and neutron-induced SETs were only observed from nMOSFETs. In addition, the nSETs and pSETs also have different degrees of dependence on the number of fingers. In the Kr-ion tests, increasing the number of fingers reduced the pulse widths of the nSETs and pSETs by 10% and 40%, respectively. Based on the above results, separate measurements of nSET and pSET are essential in SET modeling because the characteristics of nSET and pSET are different. On the ground level, it is less effective for circuit reliability to protect pMOSFETs from single event effects when the transistor sizes of the nMOSFET and pMOSFET are roughly equivalent.

This measurement also compared SET from inverter chains with nSETs and pSETs, and observed that nSETs and pSETs had larger average SET pulse width than SET from inverters, due to differences in load capacitance and multi-node charge collection. However, it was confirmed that the peaks in the pulse width distribution of SETs from inverter chains could be reproduced by the pulse width distribution calculated from measurement results of nSETs and pSETs. More accurate nSETs and pSETs measurements can be achieved by reducing the number of MOSFETs connected in parallel, thereby reducing load capacitance. By reducing the load capacitance of the target circuits, the SET distribution of an inverter can be calculated from pSET and nSET without measuring the average SET of an inverter.

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