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Soft-error Tolerance by Guard-Gate Structures on Flip-Flops in 22 and 65 nm FD-SOI Technologies

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SUMMARY We evaluated soft-error tolerance by heavy-ion irradiation test on three-types of flip-flops (FFs) named the standard FF (STDFF), the dual feedback recovery FF (DFRFF), and the DFRFF with long delay (DFRFFLD) in 22 and 65 nm fully-depleted silicon on insulator (FD-SOI) technologies. The guard-gate (GG) structure in DFRFF mitigates soft errors. A single event transient (SET) pulse is removed by the C-element with the signal delayed by the GG structure. DFRFFLD increases the GG delay by adding two more inverters as delay elements. We investigated the effectiveness of the GG structure in 22 and 65 nm. In 22 nm, Kr (40.3 MeV-cm^2/mg) and Xe (67.2 MeV-cm^2/mg) irradiation tests revealed that DFRFFLD has sufficient soft-error tolerance in outer space. In 65 nm, the relationship between GG delay and CS reveals the GG delay time which no error was observed under Kr irradiation.

key words: *soft error, heavy ion, FD-SOI, 22 nm, flip-flop, guard-gate, radiation-hard.*

1. Introduction

Process scaling results in high integration density and low power consumption. However, reliability issues of integrated circuits are becoming more serious with process scaling. Soft errors are one of the important reliability issues. When a radiation particle hits on a transistor, an error pulse is generated, which is called a single event transient (SET) pulse. A single event upset (SEU) is a phenomenon in which a stored value is flipped when a SET pulse is generated in a storage element such as SRAM or flip-flop (FF).

In the device level, the fully-depleted silicon on insulator (FD-SOI) process has around 10-100x higher soft-error tolerance than the bulk process [1][2]. It is because the buried oxide (BOX) layer prevents charge collected from substrate [3]. However, soft errors still occur on FFs or SRAMs on FD-SOI structure. Soft errors in FD-SOI are mainly caused by parasitic bipolar effects (PBEs) [4]. Therefore, circuit-level countermeasures are mandatory for mission-critical applications.

In the circuit level, several redundant FFs such as triple modular redundancy (TMR) [5] and dual interlocked storage cell (DICE) [6][7] have been proposed as radiation-hardened structures. However, they have larger area, delay, and power overheads than conventional standard FFs. Therefore, radiation-hard FFs with minimum overheads are required.

Single-event effects have been becoming dominant with process scaling [8][9][10]. There are two main reasons for that. One is that the amount of charge required to flip the output values of transistors is decreased. The other is that simultaneous errors are caused in multiple cells by a single particle. According to [11] [12], the benefits of redundant FFs decrease with process scaling. This is because the output values of the redundant nodes are flipped simultaneously due to the reduction of the distance between the redundant nodes caused by process scaling. Thus, countermeasures in advanced technologies such as interleaving are mandatory and should also be investigated.

Besides multiplexed circuits such as TMR and DICE, radiation hardened FFs with guard-gate structures [13] have also been proposed [14]–[18]. The guard-gate structure works as a low-pass filter that eliminates SET pulses. Dual feedback recovery flip-flop (DFRFF), a radiation hardened FF with low delay overhead, has been proposed in [18]. The soft-error tolerance of DFRFF has been evaluated by heavy-ion irradiation [19]. However, the soft-error tolerance is not sufficient because the delay time of the guard-gate structure is smaller than SET pulse width. In addition, errors also occur in the C-element of the guard-gate structure. Errors in C-elements occur more easily with process scaling. Thus, it is required to increase the delay time in the guard gate structure and to revise the structure of the C-element.

In this paper, we evaluate soft-error tolerance of FFs in 22 and 65 nm FD-SOI technologies by heavy-ion irradiation test and investigate the effect of the guard-gate structure in 22 and 65 nm [20]. The lack of GG delay, which is a problem in previous work, was improved without increasing the area compared to conventional circuits. In addition, the C-element was modified as a countermeasure for miniaturization. We clarified that our proposed circuit is suitable for the 22 nm FD-SOI process with the flip-well structure because the improvement is higher than that of the 65 nm process. We explain the soft-error mitigation techniques in FD-SOI process in Section II. Section III explains device architectures and several types of FFs evaluated for soft-error tolerance. Section IV explains the heavy-ion irradiation test. Section V explains the experimental results and the discussion. We conclude this paper in Section VI.

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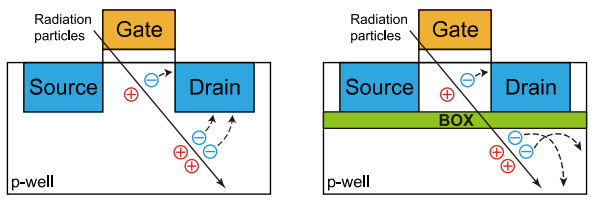
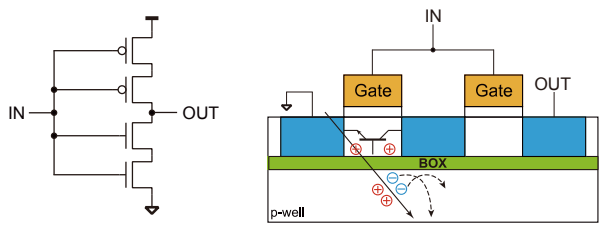


(a) Bulk structure. (b) FD-SOI structure.

Fig. 1: Soft error suppression mechanism of FD-SOI. Carriers generated in the substrate below the BOX layer are blocked by the BOX layer.



(a) Schematic (b) Cross section (nMOS)

Fig. 2: Stacked inverter. By adopting a stacked structure, the output value does not flip because one of the stacked transistors is in the off state.

2. Soft-error mitigation techniques in FD-SOI

In this section, soft errors occurred in FD-SOI and mitigation technique for soft errors are described.

2.1 Soft Errors in FD-SOI

The FD-SOI process has 10-100 times higher soft error tolerance than the bulk process. The soft error suppression mechanism of FD-SOI is shown in Fig. 1. Carriers generated in the substrate layer are blocked by the BOX layer [3]. Hence, the amount of charge collected in the diffusion layer in the FD-SOI process is less than that in the bulk process.

However, soft errors due to parasitic bipolar effects (PBEs) are vulnerable in the FD-SOI process. PBE is a phenomenon in which the channel potential changes due to carriers remaining in the substrate [4]. The output value of a logic gate is flipped when the parasitic bipolar transistor conducts as the channel potential changes.

2.2 Stacked structure [21]

The stacked structure is a design in which transistors are stacked in series. Fig. 2 shows a stacked inverter. By adopting the stacked structure, the output value does not switch without both transistors in the ON state. However, the delay time increases because the amount of drain current is reduced by stacking the transistors in series.

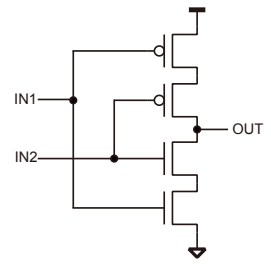
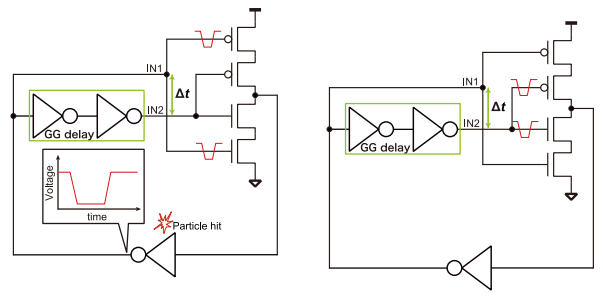


Fig. 3: Schematic of the C-element.

Table 1: Truth table of the C-element

IN1	IN2	OUT
0	0	1
0	1	Z (previous state)
1	0	Z (previous state)
1	1	0



(a) At the time of SET pulse generation (b) After Δt

Fig. 4: Guard-gate structure. Immediately after the SET pulse generation, IN1 is flipped and IN2 is kept at the correct value. After Δt, IN1 is recovered and IN2 is flipped. During this time, IN1 and IN2 are not flipped simultaneously, thus the output of the C-element is not changed.

2.3 C-element

C-element has a stacked-inverter structure with two inputs. A schematic and a truth table of the C-element are shown in Fig. 3 and Table 1, respectively. The output changes when IN1 and IN2 are the same value. If IN1 and IN2 become different, the output is in a high impedance state and keeps the previous value. The C-element itself is also robust to soft errors because of its stacked structure.

2.4 Guard-gate structure [13]

Guard-gate (GG) structure is a structure with delay elements added to one of the inputs of the C-element. Fig. 4 shows a guard gate structure with two inverters added as delay elements. When a SET pulse is generated at INV, the delay elements prevent the pulse from reaching the two inputs of the C-element at the same time. If the SET pulse is shorter than the delay time at the delay element (GG delay), the pulse is eliminated and the output value of the C-element is not flipped. The SET pulse width increases as the LET of the inrushing ions increases[22]. Soft-error tolerance is higher

Table 2: Device parameters of FD-SOI.

Technology node	Gate length [nm]	Body thickness [nm]	BOX thickness [nm]
22 nm	28	12	20
65 nm	65	12	15

with longer GG delays because longer SET pulses can be eliminated.

3. Test device

The thin-BOX FD-SOI process with low power and high performance is used for aerospace and automotive applications. The performance can be optimized by changing body bias through the thin BOX layer. Fig. 5 shows the cross sections of thin BOX FD-SOI devices in 22 and 65 nm. In 22 nm, the flip-well architecture is adopted instead of the conventional well architecture in 65 nm [23]. In the flip-well architecture, the speed performance of pMOS transistors is higher than that in the conventional one because the body bias of both pMOS and nMOS transistors is usually set to 0 V, forward body bias. Table 2 shows the parameters of 22 and 65 nm processes [24][25].

We designed three types of FFs, a standard FF (STDFF), and two radiation-hardened FFs (DFRFF, DFRFFLD), in 22 and 65 nm thin BOX FD-SOI processes. In 22 nm, all FFs have reset and scan input pins, while those in 65 nm have no reset and scan pins.

Fig. 6 shows STDFF without radiation hardness. STACKEDFF shown in Fig. 7 is a radiation-hard FF by the stacked transistors [21]. STACKEDFF is composed of latches including stacked inverters and stacked tristate inverters. The stacked structure in SOI prevents the parasitic bipolar effect (PBE). The PBE is the main cause of soft errors in SOI. However, STACKEDFF has lower performance than STDFF. In particular, the delay time of STACKEDFF is reported to be around 2x of STDFF [26][27].

Fig. 8 shows the dual feedback recovery flip-flop (DFRFF) [19]. DFRFF is a radiation-hardened flip-flop with a small delay, area and power overheads. The GG structure in DFRFF mitigates soft errors. However, the delay of the GG structures (GG delay) within the DFRFF is small and must be increased to protect long SET pulses generated in outer space by a heavy-ion strike. In this work, the GG delay of the primary latch (PL) is increased from [19] by swapping inputs of the C-element of the secondary latch (SL) as shown in Fig. 9. Moreover, DFRFF in Fig. 8 adopts the modified stacking structure compared with STACKEDFF and DFRFF in [19] as shown in Fig. 10. The on-state nMOS transistor with CLK input are placed between two off-state nMOS transistors. It prevents radiation particles from hitting at the two off-state transistors simultaneously.

Fig. 11 shows the dual feedback recovery flip-flop with long delay (DFRFFLD). DFRFFLD increases the GG delay by adding two inverters as delay elements. In the 22 nm process, the output inverter is placed outside of the GG delay element.

Table 3 shows the simulation results of area, setup time, hold time, CLK-Q delay, and power consumption at 10% data activity of STDFF, DFRFF, and DFRFFLD in 22 and 65 nm. The supply voltage (V_{DD}) is set to 0.8 V and 1.2 V in 22 nm and 65 nm, respectively. Power consumption is estimated at 10% data activity.

In 65 nm DFRFF, the performance overheads of proposed type is not significantly different from that of conventional type. CLK-Q delay overhead is kept to about 10%. In 65 nm, dynamic power overheads of both DFRFF and DFRFFLD are kept below 10%. Comparing DFRFF and DFRFFLD results, there is no significant overhead in delay and dynamic power, but the area and static power overhead of DFRFFLD becomes bigger than DFRFF due to the additional delay elements.

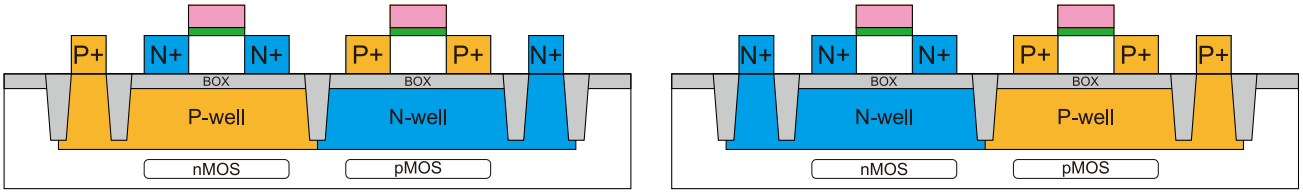
In 22 nm, all performance overheads are large unlike 65 nm. This is because that performances are limited by strict design rules. In particular, the significant large area overhead is due to dummy transistors in the C-elements of DFRFF and DFRFFLD. The source and drain of all dummy transistors are shorted. In 22 nm, even the low-overhead radiation-hard FFs have large performance overhead, which means large-overhead radiation-hard FFs such as DICE have much more performance overhead.

4. Heavy-ion Irradiation Test

The test chips were fabricated in 22 and 65 nm FD-SOI. All FFs are implemented in shift registers. Heavy ion irradiation test was conducted by Ar, Kr and Xe at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) and Cyclotron and Radioisotope Center (CYRIC). Fig. 12 shows the experimental setup of the heavy-ion irradiation tests. Table 4 shows linear energy transfer (LET) and energy of irradiated heavy ions. Fig. 13 shows the existence probability of heavy ions in outer space [28]. The number of particles above 40 MeV-cm^2/mg is very small in outer space compared to that of particles below 40 MeV-cm^2/mg. Secondary ions generated by a neutron hit with Si is mainly less than 18 MeV-cm^2/mg which is close to LET of Ar [29]. The measurement procedure is as below.

1. Initialize all FFs by 0 or 1.
2. Irradiate ions with clock signal fixed to 0 or 1.
3. Read out all FFs.

Irradiation tests were performed in the four static conditions of $(Q, CLK) = (0, 0), (0, 1), (1, 0), (1, 1)$. The cross section (CS) represents the soft-error rate. CS refers to the upset area when a particle passes through the circuit block. CS is calculated by Eq. (1) using the number of errors (N_{error}), the number of FFs (N_{FF}), the effective heavy-ion fluence per cm^2 (N_{ion}), and the angle of heavy-ion to the chips (θ) [30]. In this measurement, Heavy ions were irradiated to the test chip perpendicularly ($\theta = 0°$).



(a) Conventional well structure. Regular threshold voltage type.

(b) Flip well structure. Low threshold voltage type.

Fig. 5: Cross sections of thin BOX FD-SOI devices.

Table 3: Comparison of Area, Setup time, Hold time CLK-Q delay, Static power and Dynamic power in 22 and 65 nm.

		Area	Setup time	Hold time	CLK-Q delay	Static power	Dynamic power
22 nm	STDFF	1.00	1.00	-1.00	1.00	1.00	1.00
	DFRFF (Proposed type)	1.94	1.57	6.36	2.16	1.66	1.47
	DFRFFLD	2.05	1.37	0.91	2.22	1.61	1.60
65 nm	STDFF	1.00	1.00	-1.00	1.00	1.00	1.00
	DFRFF (Conventional type)	1.18	1.21	-1.27	1.04	1.11	1.02
	DFRFF (Proposed type)	1.18	1.17	-1.27	1.16	1.10	1.09
	DFRFFLD	1.35	1.13	-1.21	1.15	1.24	1.08

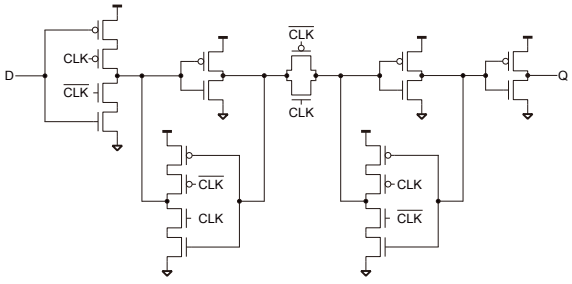


Fig. 6: Standard D-FF (STDFF).

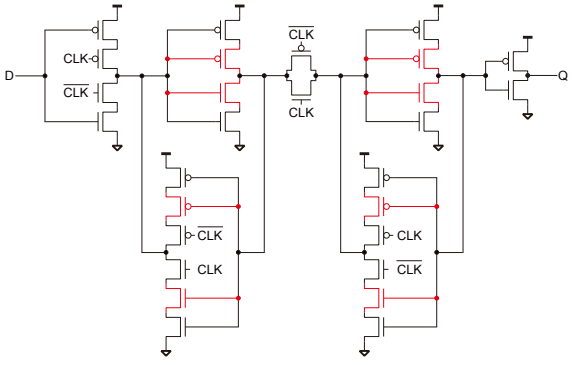
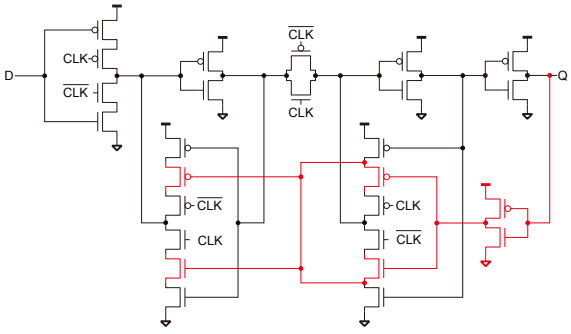
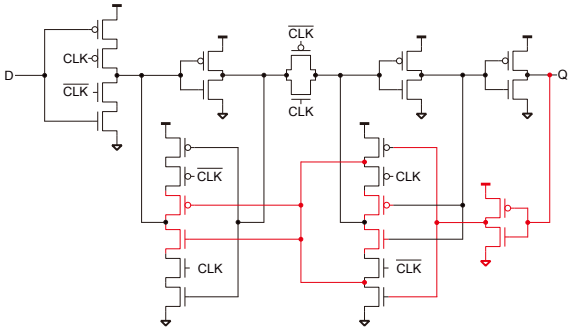


Fig. 7: STACKEDFF. The red transistors and wires are added to STDFF. The transistors that construct the inverters in the latches are stacked.



(a) Conventional type [19].



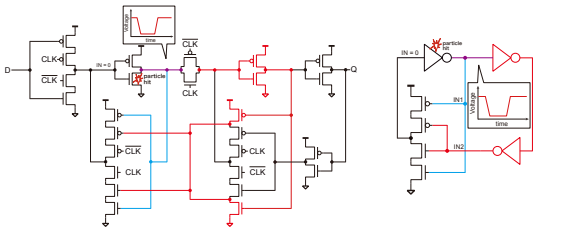
(b) Proposed type.

Fig. 8: Dual feedback recovery flip-flop (DFRFF). The red transistors and wires are added to STDFF. The delay overheads are small because the inverters between inputs D and outputs Q are not stacked.

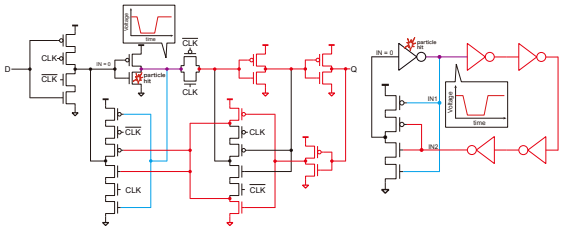
$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}} \cos\theta}. \quad (1)$$

5. Experimental Results and Discussion

Figs. 14 and 15 show the experimental results of the CS of

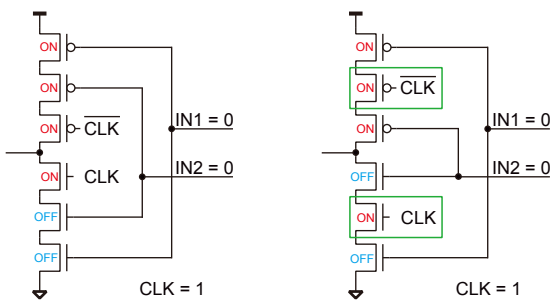


(a) Conventional type [19].



(b) Proposed type.

Fig. 9: GG delay of the PL. The red and blue lines are the signal paths. SET pulses with a wider width can be attenuated by the proposed method in (b) because the red signal path is longer than that of the conventional method in (a).



(a) Conventional type. (b) Proposed type.

Fig. 10: Two types of C-elements. The transistors in the green box are always in on-state. They prevent radiation particles from hitting at the two off-state transistors simultaneously.

Table 4: LET and energy of irradiated heavy ions.

	Ar	Kr	Xe
LET [MeV-cm^2/mg]	15.8	40.3	67.2
Energy [MeV]	137	289	454

22 and 65 nm with error bars of 95% confidence. V_{DD} is set to 0.8 V in 22 nm and 1.2 V in 65 nm. In this work, we assume that SET pulses are generated only in nMOS transistors because more than 90% of soft errors are generated by heavy ion hits on nMOS transistors [31].

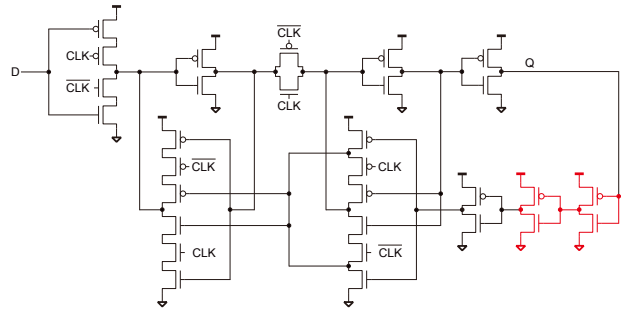
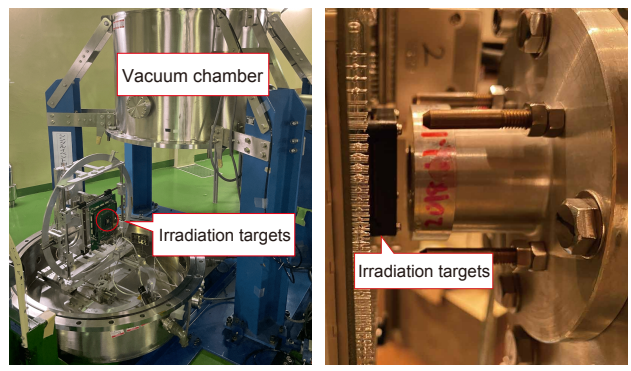


Fig. 11: DFRFFLD. The red inverters are added as GG delay elements.



(a) Ar, Kr (TIARA) (b) Xe (CYRIC)

Fig. 12: Measurement setup. In TIARA, a vacuum chamber was used to prevent attenuation of the heavy ion beam by air. In CYRIC, the measurement target was placed 5 mm from the beam opening because of the atmospheric irradiation.

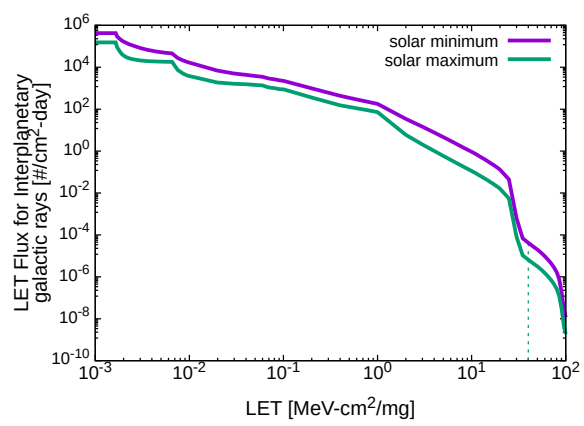
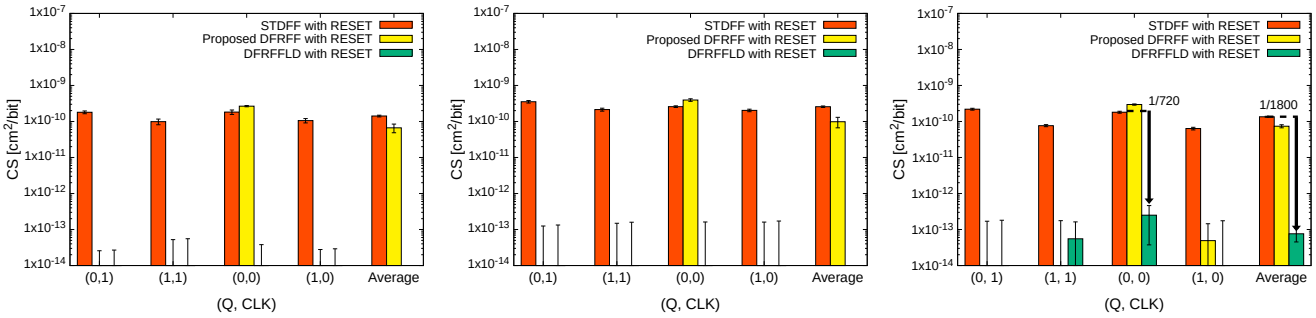


Fig. 13: LET distribution of heavy ions in outer space [28]. The dot line marks 40 MeV-cm^2/mg.

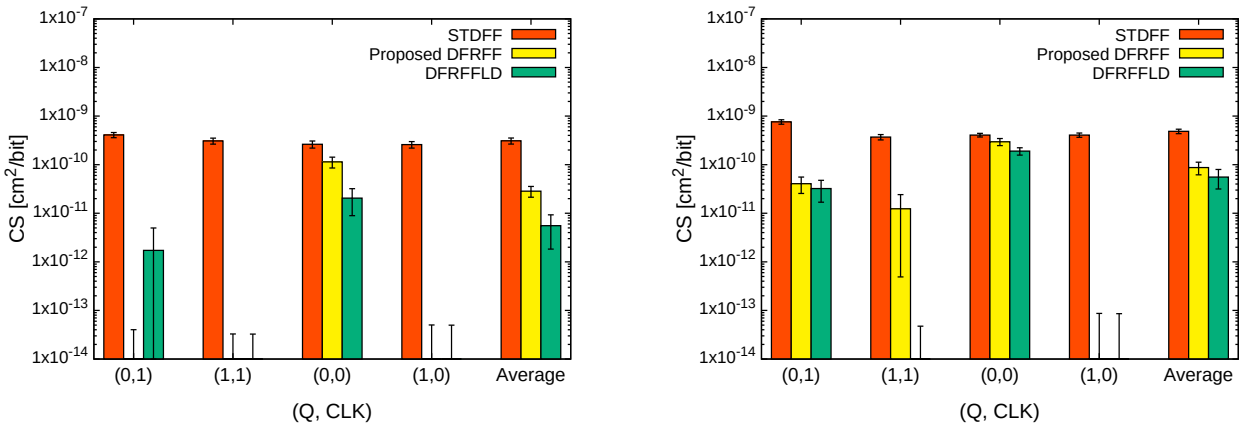
5.1 22 nm

At (Q, CLK) = (0, 0), the soft-error tolerance of DFRFF is



(a) Ar (b) Kr (c) Xe

Fig. 14: Experimental results of the CS in 22 nm by Ar, Kr, and Xe irradiation with error bars of 95% confidence. The supply voltage is set to 0.8 V.



(a) Ar (b) Kr

Fig. 15: Experimental results of the CS in 65 nm by Ar and Kr irradiation with error bars of 95% confidence. The supply voltage is set to 1.2 V.

equivalent to that of STDFF because of shorter GG delay in SL. Therefore, the soft-error tolerance of DFRFFLD with more delay elements than DFRFF is improved. In particular, DFRFFLD has no error under Kr irradiation.

DFRFFLD has no error at $(\mathrm{Q}, \mathrm{CLK}) = (0, 1)$ and $(1, 0)$ under Xe irradiation. The soft-error tolerance of DFRFFLD at $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$ is the most vulnerable among all $(\mathrm{Q}, \mathrm{CLK})$ conditions. However, the soft-error tolerance of DFRFFLD is more than 720x of STDFF. Fig. 14 (c) shows that the soft-error tolerance of DFRFFLD is 1800x higher than that of STDFF in the average of all $(\mathrm{Q}, \mathrm{CLK})$ conditions. Therefore, the GG structure of DFRFFLD is effective to ensure high soft-error tolerance in 22 nm for outer space use.

5.2 Conventional DFRFF vs proposed DFRFF in 65 nm

We compare the conventional DFRFF with the proposed DFRFF in Fig. 8. Comparison of Kr irradiation results between DFRFF in [19] and the proposed DFRFF is shown in Fig. 16. At $(\mathrm{Q}, \mathrm{CLK}) = (1, 1)$, CS of the proposed DFRFF decreases due to the increase in GG delay of PL. At $(\mathrm{Q}, \mathrm{CLK}) = (1, 0)$, CS of the proposed DFRFF decreases due to the C-element revision as shown in Fig. 10. At $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$, CS of the proposed DFRFF decreases due to the increase of GG delay of SL. The GG delay of the conventional type is 25.7 ps, in contrast to 26.5 ps of the proposed type. The number of GG delay elements is not changed. However, the change in parasitic components due to the change in the C-element paths caused an increase of the GG delay. At $(\mathrm{Q}, \mathrm{CLK}) = (0, 1)$, CS of the proposed DFRFF is not changed from the conventional type despite the change in the C-element. The reason for this is given in Section 5.3.

5.3 DFRFFLD vs proposed DFRFF in 65 nm

We compare the DFRFFLD with the proposed DFRFF in Fig. 15. At $(\mathrm{Q}, \mathrm{CLK}) = (0, 1)$, the soft-error tolerances of both DFRFF and DFRFFLD have more than 200x of STDFF

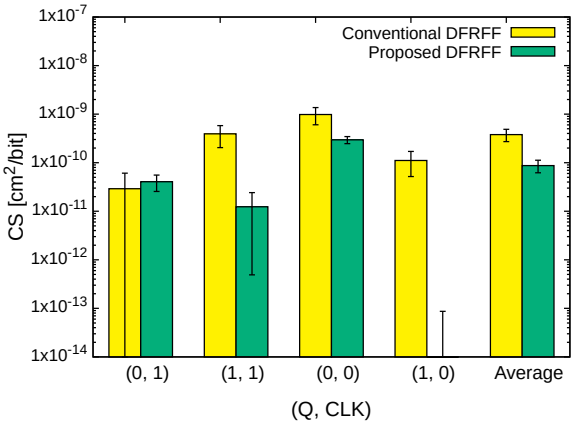


Fig. 16: Comparison of Kr irradiation results between the conventional DFRFF and the proposed DFRFF with error bars of 95% confidence. Average CS was reduced by approximately 77% by increasing GG delay and revising the C-elements.

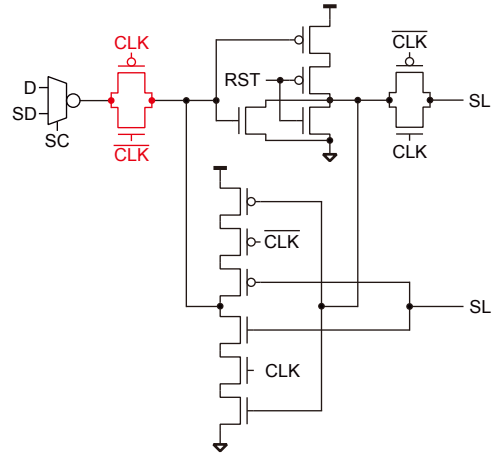


Fig. 17: PL of DFRFF and DFRFFLD in 22 nm.

under Ar irradiation as shown in Fig. 15 (a). However, the soft-error tolerances of both DFRFF and DFRFFLD were only around 20x of STDFF under Kr irradiation as shown in Fig. 15 (b). The SET pulses are generated at the outputs of the feedback gates in the PLs or the clocked inverters at D. However, the feedback gates are formed by stacked transistors and no SET pulse is generated at the stacked feedback gates and the transmission gates in SLs at $(\mathrm{Q}, \mathrm{CLK}) = (1, 0)$. In 22 nm, the transmission gates are attached at the input of PL as shown in Fig. 17 and no error was observed. Therefore, the SET pulses in 65 nm are generated at the inverters at D. Under Ar irradiation, the tolerances of both DFRFF and DFRFFLD have more than 200x of STDFF because the amount of charge generated is reduced due to the lower LET of Ar than that of Kr. When the amount of charge generated is reduced, the amount of holes stored in the body layer of the nMOS transistor is also reduced. Hence, the region where the channel potential changes is reduced, and PBEs are less likely to occur in neighbor transistors. Moreover, both nMOS transistors in the input tri-state inverter are in OFF state, which is equivalent to the stacked structure at $(\mathrm{Q}, \mathrm{CLK}) = (0, 1)$. Thus, the clocked inverter at D must be split into an inverter and a transmission gate as in SL to increase radiation hardness.

At $(\mathrm{Q}, \mathrm{CLK}) = (1, 1)$, DFRFFLD has no error in 65 nm because the number of GG delay elements is larger than DFRFF by two inverters. However, DFRFF and DFRFFLD are as vulnerable as STDFF in 65 nm at $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$ because of the insufficient GG delay in SL. In particular, the soft-error tolerance of DFRFFLD in 65 nm is only around 2x of STDFF under Kr irradiation. Hence, additional inverters must be added as GG delay elements for DFRFFLD in 65 nm.

We investigate the relationship between the GG delay and CS under Kr irradiation in 65 nm as shown in Fig. 18. The CS values are the same as those shown in Fig. 15 (b). GG delay is calculated under nominal conditions because the heavy-ion irradiation tests were conducted under nominal conditions. At the point where the GG delay of PL on DFRFFLD was 151 ps, no error was observed. The blue line refers to the fitting function as shown in Eq. (2).

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = -3.37 \times t\ [\mathrm{sec}] + 3.94 \times 10^{-10}. \quad (2)$$

According to Eq. (2), CS become $0\,\mathrm{cm}^2/\mathrm{bit}$ at 117 ps GG delay. Thus, the width of the longest SET pulses generated by Kr in 65 nm is less than 117 ps. The GG delay must be longer than 117 ps to prevent errors by Kr in 65 nm.

6. Conclusion

We evaluated the soft-error tolerance of three types of FFs, STDFF, DFRFF, and DFRFFLD, in 22 and 65 nm FD-SOI by heavy-ion irradiation. In this study, we modified the DFRFF guard gate and C-element structures. The GG delay of PL is increased by swapping inputs of the C-element of the SL. An on-state transistor with CLK input is placed between two off-state transistors to prevent radiation from simultaneously hitting the two off-state transistors. In 22 nm, DFRFFLD has no error under Ar and Kr irradiation test. Under Xe irradiation, it has 1800x higher soft-error tolerance than STDFF. Therefore DFRFFLD in 22 nm has enough soft-error tolerance for outer space use. In 65 nm, the proposed DFRFF has 77% less CS than the conventional DFRFF. Therefore, the revisions of the guard gate structure and C-element are effective. However, DFRFFLD has only about 2x of STDFF at $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$ under Kr irradiation. The relationship between GG delay and CS reveals the condition of GG delay which no error was observed under Kr irradiation. The GG delay must be longer than the condition to prevent errors by a heavy ion hit.

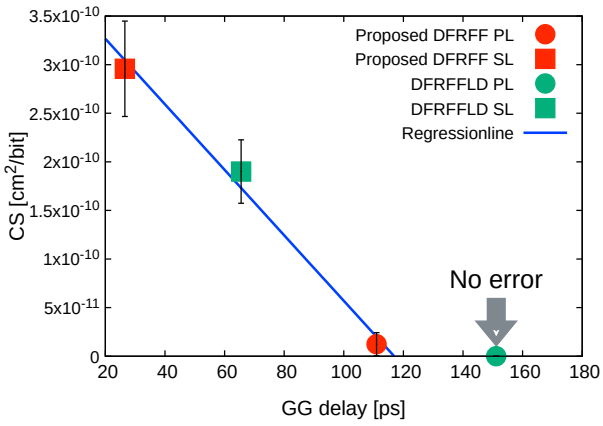


Fig. 18: Comparison between the GG delay and CS under Kr irradiation in 65 nm. At the point where the GG delay of PL on DFRFFLD was 151 ps, no error was observed. In 22 nm, the slope of the fitting function for the relationship between GG delay and CS is steeper than that in 65 nm. The difference in slope is due to the difference in pMOS performance (speed and current) caused by the difference in well structures. Under typical condition, the 22 nm device is in a forward body bias state, which increases the amount of current of the pMOS. The increase in current also suppresses the SET pulses generated in nMOS.

7. Acknowledgment

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References

[1] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera, "A low-power and area-efficient radiation-hard redundant flip-flop, dice acff, in a 65 nm thin-box fd-soi," IEEE Transactions on Nuclear Science, vol.61, no.4, pp.1881–1888, 2014.

[2] M. Hifumi, H. Maruoka, S. Umehara, K. Yamada, J. Furuta, and K. Kobayashi, "Influence of layout structures to soft errors caused by higher-energy particles on 28/65 nm fdsoi flip-flops," 2017 IEEE International Reliability Physics Symposium (IRPS), pp.SE–5.1–SE–5.4, 2017.

[3] D. Kobayashi, K. Hirose, H. Ikeda, and H. Saito, "Radiation-induced pulse noise in soi cmos logic," Int'l Symposium on Advanced Semiconductor-on-insulator Technology and Related Physics (in 219th ECS Meeting), May 2011.

[4] M. Raine, M. Gaillardin, T. Lagutere, O. Duhamel, and P. Paillet, "Estimation of the single-event upset sensitivity of advanced SOI SRAMs," IEEE Trans. Nucl. Sci., vol.65, no.1, pp.339–345, Jan. 2018.

[5] D. Mavis and P. Eaton, "Soft error rate mitigation techniques for modern microcircuits," 2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320), pp.216–225, 2002.

[6] F. Mori, M. Ebara, Y. Tsukita, J. Furuta, and K. Kobayashi, "Intrinsic vulnerability to soft errors and a mitigation technique by layout optimization on dice flip flops in a 65-nm bulk process," IEEE Transactions on Nuclear Science, vol.68, no.8, pp.1727–1735, 2021.

[7] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," IEEE Transactions on Nuclear Science, vol.43, no.6, pp.2874–2878, 1996.

[8] S.M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "An analytical model for soft error critical charge of nanometric srams," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.17, no.9, pp.1187–1195, 2009.

[9] H. Liu, M. Cotter, S. Datta, and V. Narayanan, "Technology assessment of si and iii-v finfets and iii-v tunnel fets from soft error rate perspective," 2012 International Electron Devices Meeting, pp.25.5.1–25.5.4, 2012.

[10] P. Roche, J. Autran, G. Gasiot, and D. Munteanu, "Technology downscaling worsening radiation effects in bulk: Soi to the rescue," 2013 IEEE International Electron Devices Meeting, pp.31.1.1–31.1.4, 2013.

[11] T.D. Loveless, S. Jagannathan, T. Reece, J. Chetia, B.L. Bhuva, M.W. McCurdy, L.W. Massengill, S.J. Wen, R. Wong, and D. Rennie, "Neutron- and proton-induced single event upsets for d- and dice-flip/flop designs at a 40 nm technology node," IEEE Transactions on Nuclear Science, vol.58, no.3, pp.1008–1014, 2011.

[12] N.J. Gaspard, S. Jagannathan, Z.J. Diggins, M.P. King, S.J. Wen, R. Wong, T.D. Loveless, K. Lilja, M. Bounasser, T. Reece, A.F. Witulski, W.T. Holman, B.L. Bhuva, and L.W. Massengill, "Technology scaling comparison of flip-flop heavy-ion single-event upset cross sections," IEEE Transactions on Nuclear Science, vol.60, no.6, pp.4368–4373, 2013.

[13] A. Balasubramanian, B. Bhuva, J. Black, and L. Massengill, "Rhbd techniques for mitigating effects of single-event hits using guard-gates," IEEE Transactions on Nuclear Science, vol.52, no.6, pp.2531–2535, 2005.

[14] Y.Q. Li, H.B. Wang, R. Liu, L. Chen, I. Nofal, Q.Y. Chen, A.L. He, G. Guo, S.H. Baeg, S.J. Wen, R. Wong, Q. Wu, and M. Chen, "A 65 nm temporally hardened flip-flop circuit," IEEE Transactions on Nuclear Science, vol.63, no.6, pp.2934–2940, 2016.

[15] T. Uemura, S. Lee, D. Min, I. Moon, S. Lee, and S. Pae, "Seiff: Soft error immune flip-flop for mitigating single event upset and single event transient in 10 nm finfet," 2019 IEEE International Reliability Physics Symposium (IRPS), pp.1–6, 2019.

[16] A. Jain, A.M. Veggetti, D. Crippa, A. Benfante, S. Gerardin, and M. Bagatin, "Radiation tolerant multi-bit flip-flop system with embedded timing pre-error sensing," IEEE Journal of Solid-State Circuits, vol.57, no.9, pp.2878–2890, 2022.

[17] H. Zhang, H. Jiang, T.R. Assis, D.R. Ball, K. Ni, J.S. Kauppila, R.D. Schrimpf, L. Massengill, B.L. Bhuva, B. Narasimham, S. Hatami, A. Anvar, A. Lin, and J.K. Wang, "Temperature dependence of soft-error rates for ff designs in 20-nm bulk planar and 16-nm bulk finfet technologies," 2016 IEEE International Reliability Physics Symposium (IRPS), pp.5C–3–1–5C–3–5, 2016.

[18] K. Yamada, J. Furuta, and K. Kobayashi, "Radiation-hardened flip-flops with small area and delay overheads using guard-gates in fd-soi processes," 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp.1–3, 2018.

[19] M. Ebara, K. Yamada, K. Kojima, Y. Tsukita, J. Furuta, and K. Kobayashi, "Evaluation of soft-error tolerance by neutrons and heavy ions on flip flops with guard gates in a 65-nm thin box fd-soi process," IEEE Transactions on Nuclear Science, vol.67, no.7, pp.1470–1477, 2020.

[20] R. Nakajima, T. Ito, T. Kii, M. Ebara, J. Furuta, K. Kobayashi, M. Louvat, F. Jacquet, O. Montfort, J. Lionel, and V. Huard, "Soft-error tolerance by guard-gate structures on flip-flops in 22/65 nm fd-soi technologies," 2022 European Conference on Radiation and its Effects on Components and Systems, 2022.

[21] A. Makihara, T. Yamaguchi, H. Asai, Y. Tsuchiya, Y. Amano, M. Mi-

dorikawa, H. Shindou, S. Onoda, T. Hirao, Y. Nakajima, T. Takahashi, K. Ohnishi, and S. Kuboyama, "Optimization for seu/set immunity on 0.15 @article4395066, author=Narasimham, Balaji and Bhuva, Bharat L. and Schrimpf, Ronald D. and Massengill, Lloyd W. and Gadlage, Matthew J. and Amusan, Oluwole A. and Holman, William Timothy and Witulski, Arthur F. and Robinson, William H. and Black, Jeffrey D. and Benedetto, Joseph M. and Eaton, Paul H., journal=IEEE Transactions on Nuclear Science, title=Characterization of Digital Single Event Transient Pulse-Widths in 130-nm and 90-nm CMOS Technologies, year=2007, volume=54, number=6, pages=2506-2511, doi=10.1109/TNS.2007.910125 μm fully depleted cmos/soi digital logic devices," IEEE Transactions on Nuclear Science, vol.53, no.6, pp.3422–3427, 2006.

[22] B. Narasimham, B.L. Bhuva, R.D. Schrimpf, L.W. Massengill, M.J. Gadlage, O.A. Amusan, W.T. Holman, A.F. Witulski, W.H. Robinson, J.D. Black, J.M. Benedetto, and P.H. Eaton, "Characterization of digital single event transient pulse-widths in 130-nm and 90-nm cmos technologies," IEEE Transactions on Nuclear Science, vol.54, no.6, pp.2506–2511, 2007.

[23] R. Ranica, N. Planes, O. Weber, O. Thomas, S. Haendler, D. Noblet, D. Croain, C. Gardin, and F. Arnaud, "Fdsoi process/design full solutions for ultra low leakage, high speed and low voltage srams," 2013 Symposium on VLSI Circuits, pp.T210–T211, 2013.

[24] J. Auerhammer, C. Hartig, K. Wendt, R. van Oostrum, G. Pfeiffer, S. Bayer, and B. Srocka, "Silicon thickness variation of fd-soi wafers investigated by differential reflective microscopy," 2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp.1–3, 2016.

[25] Y. Yamamoto, H. Makiyama, H. Shinohara, T. Iwamatsu, H. Oda, S. Kamohara, N. Sugii, Y. Yamaguchi, T. Mizutani, and T. Hiramoto, "Ultralow-voltage operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM down to 0.37 V utilizing adaptive back bias," VLSI Cir. Symp., pp.T212–T213, 2013.

[26] K. Yamada, M. Ebara, K. Kojima, Y. Tsukita, J. Furuta, and K. Kobayashi, "Radiation-hardened structure to reduce sensitive range of a stacked structure for fdsoi," IEEE Transactions on Nuclear Science, vol.66, no.7, pp.1418–1426, 2019.

[27] J. Furuta, J. Yamaguchi, and K. Kobayashi, "A radiation-hardened non-redundant flip-flop, stacked leveling critical charge flip-flop in a 65 nm thin box fd-soi process," IEEE Transactions on Nuclear Science, vol.63, no.4, pp.2080–2086, 2016.

[28] C.P. Jenet L. B., John C. I., "The radiation environment for the next generation space telescope," NGST Document, pp.A8–A12, Sep. 2000 [Online] Available: https://bhi.gsfc.nasa.gov.

[29] H. Asai, K. Sugimoto, I. Nashiyama, Y. Iide, K. Shiba, M. Matsuda, and Y. Miyazaki, "Terrestrial neutron-induced single-event burnout in SiC power diodes," 2011 12th European Conference on Radiation and its Effects on Components and Systems, pp.238–243, Sep. 2011.

[30] J.S. Kauppila, T.D. Loveless, R.C. Quinn, J.A. Maharrey, M.L. Alles, M.W. McCurdy, R.A. Reed, B.L. Bhuva, L.W. Massengill, and K. Lilja, "Utilizing device stacking for area efficient hardened soi flip-flop designs," 2014 IEEE International Reliability Physics Symposium, pp.SE.4.1–SE.4.7, 2014.

[31] K. Yamada, H. Maruoka, J. Furuta, and K. Kobayashi, "Sensitivity to soft errors of nmos and pmos transistors evaluated by latches with stacking structures in a 65 nm fdsoi process," 2018 IEEE International Reliability Physics Symposium (IRPS), pp.P–SE.3–1–P–SE.3–5, 2018.

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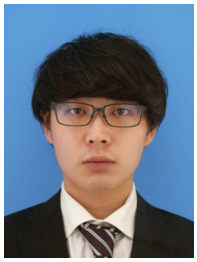

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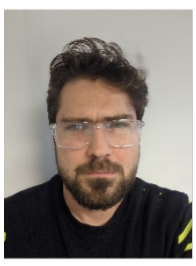

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