Impact of Random Telegraph Noise on CMOS Logic Delay Uncertainty under Low Voltage Operation

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Abstract

Statistical nature of RTN-induced delay fluctuation is described by measuring 2,520 ROs fabricated in a commercial 40 nm CMOS technology. Small number of samples have a large RTN-induced delay fluctuation. RTN-induced delay fluctuation becomes as much as 10.4% of nominal oscillation frequency under low supply voltage (0.65V). By slightly increasing the transistor size, more than 50% reduction of frequency uncertainty can be achieved under 0.75V operation. The impact of the parameters that can be changed by circuit designers is clarified in view of RTN-induced CMOS logic delay uncertainty.

Introduction

Designing reliable systems has become more difficult in recent years[1]-[3]. In addition to conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems. Random Telegraph Noise (RTN) has attracted much attention as a temporal transistor performance fluctuation. RTN already has a serious impact on CMOS image sensors[4], flash memories[5], and SRAMs[6]. Recently we have shown that RTN also induces performance fluctuation to logic circuits[7]. In this paper, we investigated the impact of RTN on CMOS logic delay uncertainty based on the measurement data. Circuit designers can change various parameters such as operating voltage, transistor size, logic stage number, logic gate type, and substrate bias. However, the impact of such parameters on RTN is not well understood at the circuit level. The main contribution of this paper is clarifying this impact based on the measurement data.

Test Structure for RTN Evaluation

Figure 1 shows a typical synchronous circuit structure where a logic path exists between two registers. Figure 2 shows the simplest test structure that can emulate the synchronous circuit operation of Fig. 1. Combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. Sequential circuit operation is emulated by D flip-flop (DFF) toggled by the RO output. The power supply for RO (VDD_{RO}) and DFF (VDD_{DFF}) can be independently controlled. We can also control the substrate bias for pMOS and nMOS. Figure 3 shows the whole test structure for the RTN measurement. RTN-induced delay fluctuation is measured by
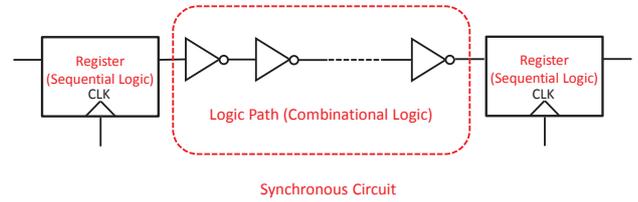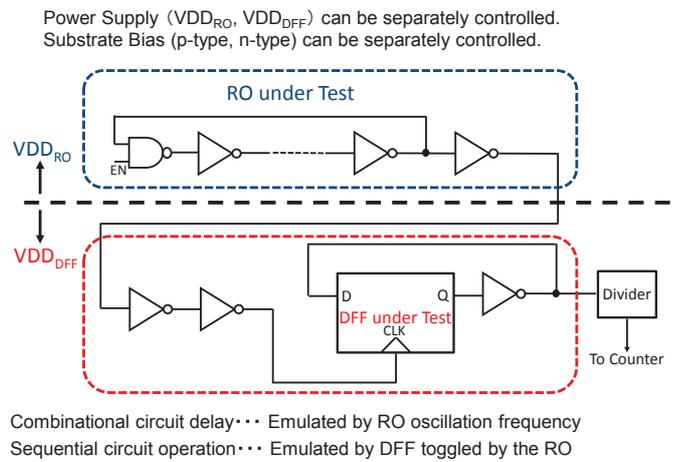

Figure 1: Typical synchronous circuit structure.

Power Supply (VDD_RO, VDD_DFF) can be separately controlled.
Substrate Bias (p-type, n-type) can be separately controlled.

Combinational circuit delay··· Emulated by RO oscillation frequency
Sequential circuit operation··· Emulated by DFF toggled by the RO

Figure 2: Simplest test structure that can emulate the synchronous circuit operation.

RO array (840 ROs / 2mm²)
·40nm CMOS Technology
·Various ROs / section
·Statistical nature of RTN can be evaluated.
·RO power supply can be separately controlled.
·Substrate bias can be separately controlled.

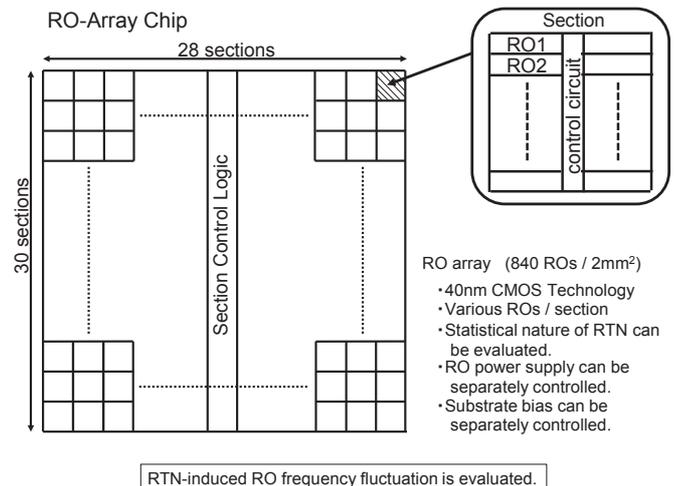RTN-induced RO frequency fluctuation is evaluated.

Figure 3: Whole test structure for RTN measurement. One test structure contains 840 ROs.

the RO frequency fluctuation. Various type of ROs are contained in one circuit unit, which is called a section (Fig. 3). There are 840 same sections on 2 mm² area. Thus the statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at the room temperature.

Measurement Results of Logic Delay Fluctuation

Figure 4 (a) shows the measurement result of the oscillation frequency of a 7-stage RO for about 80 s at VDD_{RO}=0.65V. The size of the inverter is smallest in this technology. The
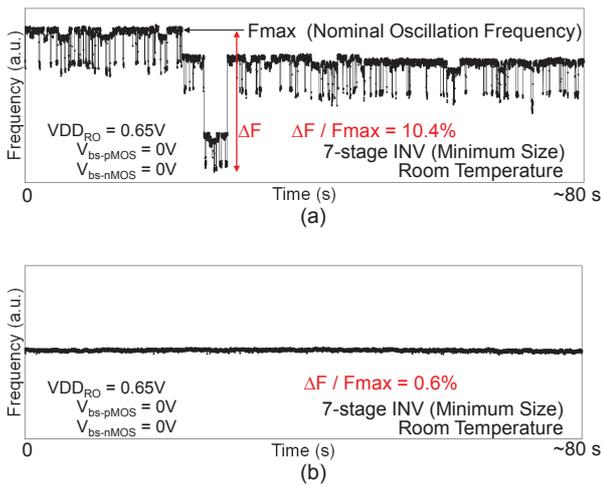

Figure 4: Measurement result of RTN-induced RO frequency fluctuation. (a) $\Delta F/F_{\max} = 10.4\%$ (b) $\Delta F/F_{\max} = 0.6\%$.
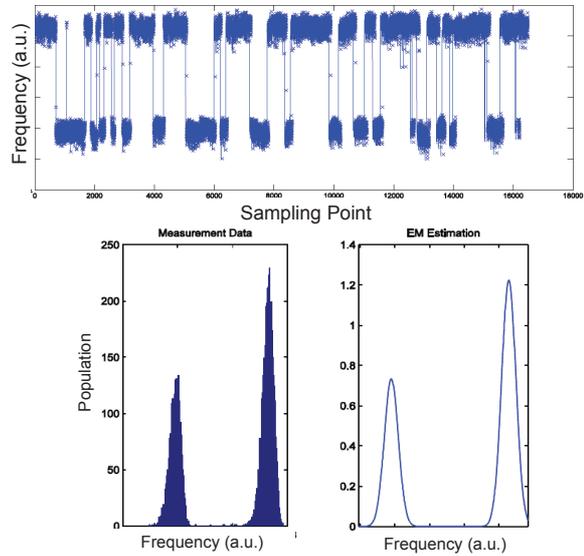

Figure 5: Measurement results that shows 2-state fluctuation.

Figure 6: PSD of Fig. 5

Figure 7: Time constant distribution of Fig. 5

Figure 8: Estimation of discrete states by EM algorithm for a 2-state case.

Figure 9: Estimation of discrete states by EM algorithm for a complex case.
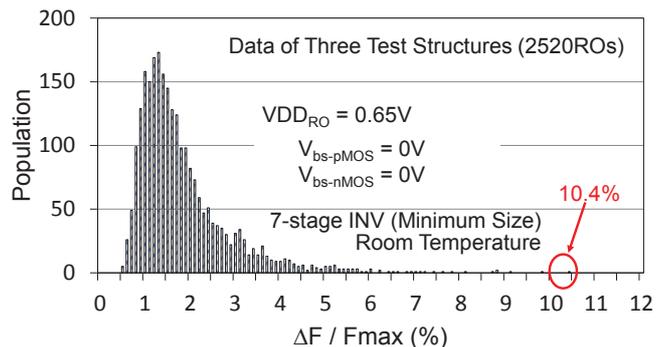
Figure 10: Histogram of measured $\Delta F/F_{\max}$.

body bias for pMOS ($V_{\text{bs}-\text{pMOS}}$) and nMOS ($V_{\text{bs}-\text{nMOS}}$) are set to 0V. Measurement results show the large step-like frequency fluctuation. Here, $F_{\max}$ is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation as shown in Fig. 4 (a). $\Delta F/F_{\max}$ is a good measure for the impact of RTN-induced frequency fluctuation. It is 10.4 % for Fig. 4 (a). However, significant fluctuation is not observed for the case of Fig. 4 (b). Large fluctuation such as Fig. 4 (a) is a rare case that reflects the RTN nature. Figure 5 shows a typical measurement data at VDD$_{\text{RO}}$=0.65V where a large 2-state fluctuation is observed. Time constants τ_{c} and τ_{e} are defined as the time that the RO stays at high-frequency state and low-frequency state respectively. The power spectrum density (PSD) of Fig. 5 is obtained by quantizing the measurement data of Fig. 5 into the 2-state waveform. Lorentzian power spectrum is observed (Fig. 6). Figure 7 shows time constant (τ_{c}, τ_{e}) distributions of Fig. 5. It is found that both distributions for τ_{c} and τ_{e} follow exponential distribution ($e^{-t/\tau}$). Lorentzian PSD and $e^{-t/\tau}$ distribution are observed for the case of a transistor where a single defect causes RTN fluctuation. This indicates that RTN fluctuation of Fig. 5 is caused by a single defect in a specific transistor in the 7-stage RO. Figure 8 and 9 show the automatic discrete state estimation by the EM (Expectation Maximization) algorithm[8]. Figure 8 shows 2-state fluctuation. There are two peaks in the histogram. It is assumed to be composed of two normal distributions. Average values of two normal distributions are identified with discrete two states of RO oscillation by the EM algorithm. Figure 9 shows the complex fluctuation. The EM algorithm works well in such a complex case. It is possible to estimate discrete states of measurement data automatically by the EM method. Figure 10 shows the histogram of measured $\Delta F/F_{\max}$ for the whole test structure of Fig. 3 over three chips (2,520 ROs). It is found that the small number of samples have a large RTN-induced fluctuation and a long tail exists for larger $\Delta F/F_{\max}$.

Impact of RTN on Delay Uncertainty

Figure 11 shows the cumulative distribution function (CDF) of $\Delta F/F_{\max}$ for various VDD$_{\text{RO}}$. The impact of RTN-induced delay fluctuation increases rapidly under low voltage operation. Figure 12 shows CDF of $\Delta F/F_{\max}$ for two transistor sizes. The ratio of nMOS gate area ($W \times L$) of the minimum size inverter (INV) to the standard size INV is 0.30. The ratio of pMOS gate area of minimum INV to the standard INV is 0.21. Increasing the gate area slightly is very effective to suppress the delay uncertainty. More than 50% reduction of $\Delta F/F_{\max}$ can be achieved under 0.75V operation. Figure 13 shows the CDF of $\Delta F/F_{\max}$ for various logic stage numbers. As the stage number decreases, the impact of RTN becomes larger. Figure 14 shows the CDF of $\Delta F/F_{\max}$ for various logic types of 19-stage ROs. The impact of RTN is most pronounced for the inverter case. Figure 15 shows
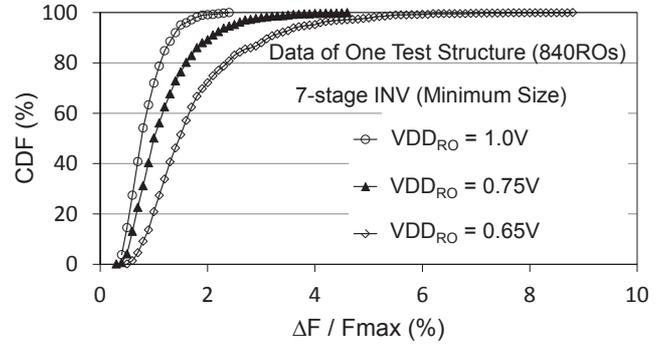

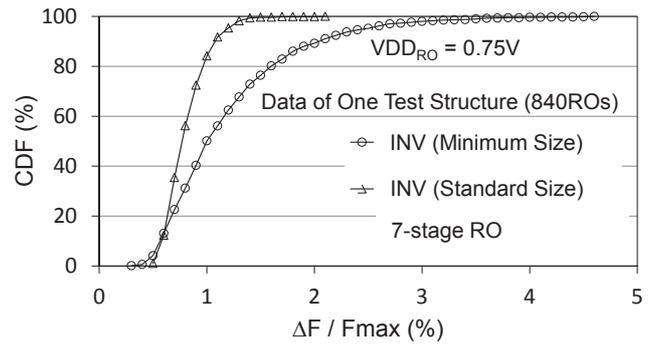Figure 11: CDF of $\Delta F/F_{max}$ for various VDD$_{\text{RO}}$.

Figure 12: CDF of $\Delta F/F_{max}$ for two transistor sizes.
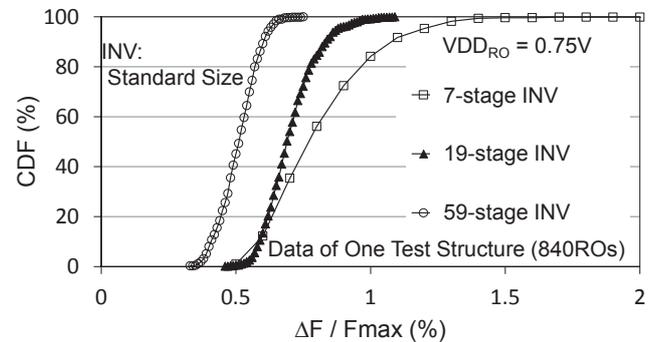

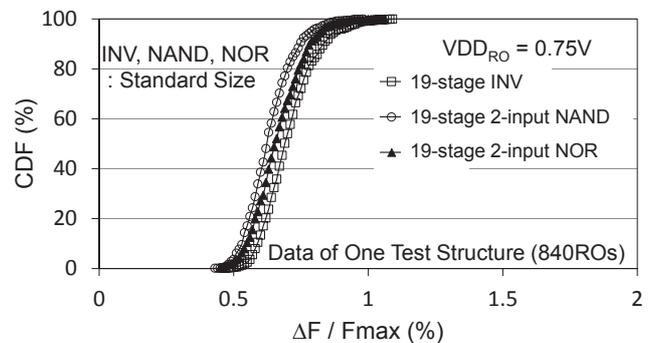Figure 13: CDF of $\Delta F/F_{max}$ for various logic stage numbers.

Figure 14: CDF of $\Delta F/F_{max}$ for various logic types.

the the measurement results of frequency fluctuation of one RO for various substrate bias conditions. For this sample, the time constant is modulated considerably only when the pMOS substrate bias is changed from 0V to 0.2V. Figure 16 is the power spectrum density (PSD) for the same sample of Fig. 15. RTN-induced RO frequency fluctuation for 60 s is evaluated under various substrate bias conditions. We observe the effect of one trap at the PMOS inside the RO that induces large delay fluctuation at the circuit level.
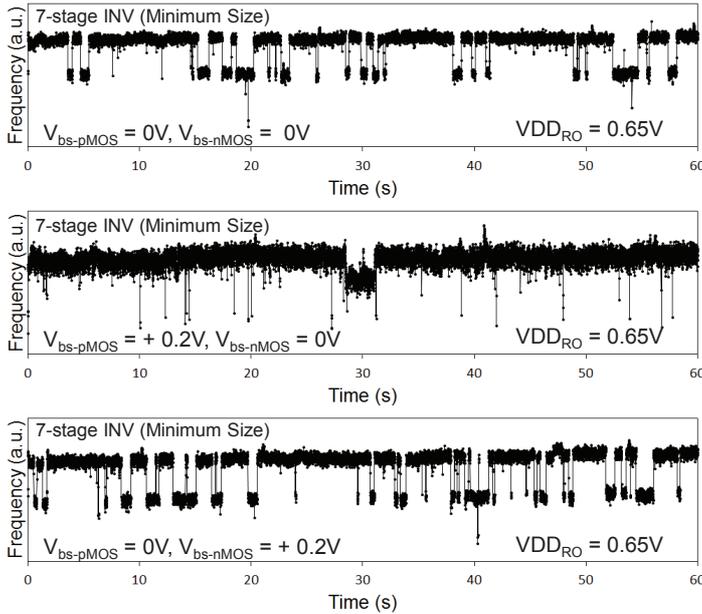

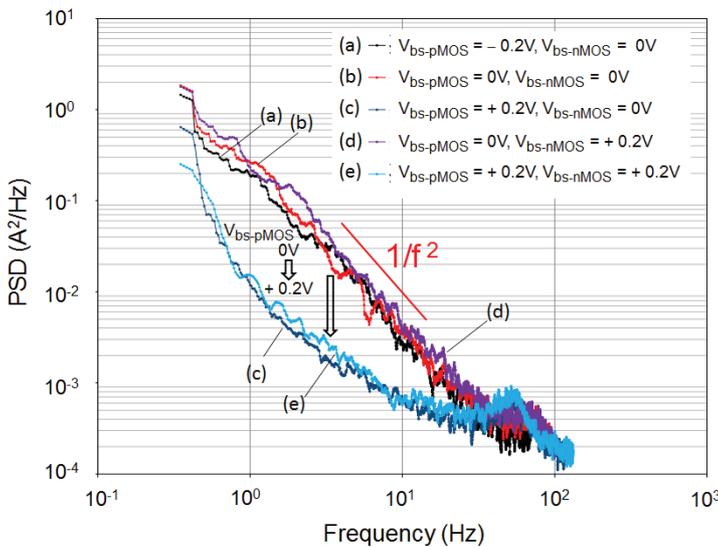Figure 15: RTN-induced RO frequency fluctuation for various substrate bias conditions.

Figure 16: Power spectrum of RTN-induced RO frequency fluctuation for various substrate bias conditions.

Conclusions

Statistical nature of RTN-induced delay fluctuation is described by measuring 2,520 ROs fabricated in a commercial 40 nm CMOS technology. The small number of samples have a large RTN-induced delay fluctuation. RTN-induced delay fluctuation becomes as much as 10.4% of nominal oscillation frequency under low supply voltage (0.65V) operation. It is also indicated that a single defect in a specific transistor in an RO causes clear 2-state oscillation fluctuation. The EM algorithm works well to identify discrete states for a complex fluctuation as well as a simple 2-state one. More than 50% reduction of frequency uncertainty ($\Delta F/F_{\max}$) can be achieved under 0.75V operation by slightly increasing the transistor size. The impact of the parameters that can be changed by circuit designers such as operating voltage, transistor size, logic stage number, logic gate type, and substrate bias is clarified in view of RTN-induced CMOS logic delay uncertainty.

Acknowledgement

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