Measurement Results of Substrate Bias Dependency on Negative Bias Temperature Instability Degradation in a 65 nm Process

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Abstract— The transistor size keeps shrinking by Moore's law and timing degradation of the scaled transistors is becoming critical. Recently, the scaling of CMOS technology increases the effect of NBTI (Negative Bias Temperature Instability) in PMOS. NBTI is an important reliability issue for analog as well as digital CMOS circuits. As transistors are scaled refined,the impact of NBTI becomes more critical. This paper deals with relationship between NBTI and the substrate bias. If the substrate bias go a forward, degradation of NBTI is accelerated. We show measurement results of degradation due to NBTI according to the forward and reverse body biases.

I. Introduction

Integrated circuit technologies have advanced rapidly. The number of transistors on a chip has been exponentially increased in these decades. As a result, the element becomes small, the number of transistors per chip increases and operation speed progresses. But the problem due to the variation in the elements has become apparent as the number of elements increases. As the element is becoming smaller in this way, the NBTI (Negative Bias Temeperature Instability)problems happen. The main contribution in this paper is showing measurement results of substrate bias dependency on NBTI degradation. NBTI is the phenomenon in which threshold voltage of the device increases gradually over time by negative bias voltage being applied between the gate and source nodes of PMOS[1]. When threshold voltage of the device increases, logic gates become slower. The speed of degradation by NBTI is different according to the history of dynamic and static stress[2].

The substrate bias control technology controls threshold voltages. It can suppress global variations[3]. We measure substrate bias dependency on NBTI degradation. In the measurement, we shift the substrate bias forward and backward as shown in Fig. 1. In forward body bias, $V_{\rm bs}$ decrease on PMOS and increase on NMOS. In reverse body bias, $V_{\rm bs}$ increase on PMOS and decrease on NMOS. NBTI degradation accelerates in forward body bias[4].

In this paper, we show the measurement circuit and how to measure substrate bias dependency on NBTI in Section II. Section III shows measurement results. Finally, we conclude this paper in Section IV.

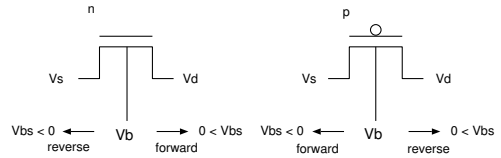

Fig. 1. Forward and reverse body bias on NMOS and PMOS.

II. Measurement circuit and setups

In this section, we explain the structure of measurement circuit and RO in a measurement circuit. We measure a chip which integrates lots of ROs in a 65 nm process.

A. Measurement Circuit

The measurement circuit [5] includes two parts, the NBTI-measurement and variation-measurement parts. They are connected in series. We measured the NBTI-measurement part in this paper. Fig. 3 shows the block diagram of the test structure composed of sections (S0-S2) and units (U0-UF). The NBTI-measurement part is composed of 44 sections. A unit contains an RO, a 1/2 divider and a one-bit counter. Fig. 4 is a block diagram of the unit. The RO starts to oscillate when ROEN is enabled. Then the oscillated signals are divided by the 1/2 divider. The scan FF works as the LSB (Least Significant Bit) of the 16-bit counter. When the RO in U0 is oscillating, the other 15 units (U1-UF) work as the upper 15-bit counter. The NBTI degradations can be measured as the number of oscillation in a specific time duration. When oscillated, the RO is exposed to the AC stress. When stopped, it is exposed to the DC stress.

When the ECSR (ENABLE-CONTROLL shift register) stores 1, ROEN can be activated. In order to oscillate all ROs in the units, all ECSRs store 1. In the measured chip, 44 sections are embedded. There are 16 types of ROs in the unit, but we measured the 5-stage RO composed of four inverters and a NAND gate with the minimum size transistors in a 65 nm process as shown in Fig. 2. When the input value of inverter is "1", PMOS transistors are degraded due to NBTI. When it is "0", these degraded transistors are rapidl recovering.When ROs stop, recovered and stressed inverters are located alternately as shown in Fig. 2.

B. Measurement Setups

We observe NBTI degradation to measure oscillation frequency (f) of ROs. It is because frequency is degraded in

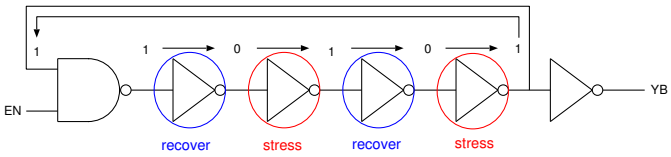

Fig. 2. 5-stage RO for NBTI measurement.

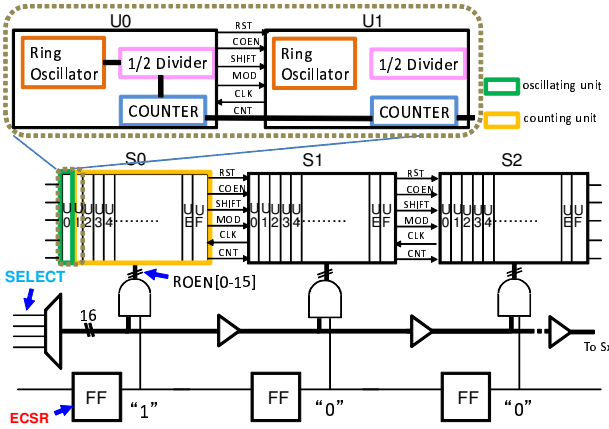

Fig. 3. Block diagram of sections (S0-2) and units (U0-F).

proportion to the threshold shift due to NBTI. When the circuit shifts values of count, ROs stop to oscillation. When it finishes to shift values of count, it starts to sleep phase. It is not oscillation phase with keeping voltage applied. During measurements, ROs repeat the oscillation and stop phases as shown in Fig. 5. In oscillation phase, ROs get AC stress and those get DC stress in stop phase. In order to measure the degradation, the stop phase is activated at 1s, 10 s, 100 s, 200 s, ... and 1,000 s. The NBTI degradation is measured until the DC stress time reaches to 1,000 s.

DUTs are turned off over 2 hours between each measurement cycle to be recovered from the NBTI degradation. These measurements were repeated 19 times by changing the substrate biases. A measurement takes about 16 minutes. So, the time of all measuring is about 41 hours.In measurements of the forward body biases, PMOS substrate bias changes from 0 V to 0.3 V. As for the reverse body bias, it changes from 0 V to -0.7 V. Fig. 6 shows the flow chart of the

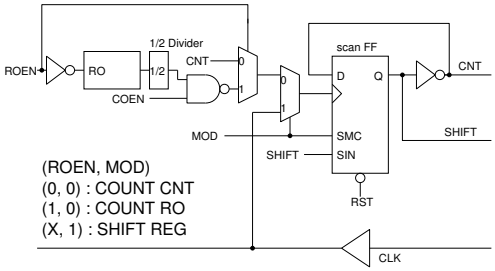

Fig. 4. Block diagram of a unit.

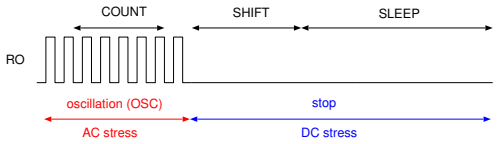

Fig. 5. State of ROs to measure NBTI degradation.

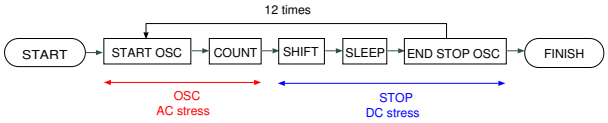

Fig. 6. Flowchart of NBTI measurement.

measurement. The measured chip is fabricated in a 65-nm bulk CMOS process. The power supply voltage is increased to 2.0 V in order to accelerate the NBTI degradation.

III. Results and Discussion

In this section, we discuss results of substrate bias dependency on the NBTI degradation.

A. Reaction-Diffusion (RD) Model

The Reaction-diffusion model is one of the NBTI degradation model. Negative voltage between the gate and the source of a PMOS transistor separates the bond of silicon and hydrogen or nitrogen in the interface between substrate and gate oxide. The electron pairs generated by these reactions are called interface traps. The channel current decreases because of these trapped carriers. NBTI is the degradation of performance based on this phenomenon. Eq. (1)-(3) show the degradation model formula of threshold voltage based on the RD model.

$$\Delta V_{\rm th} = \{K_{\rm v}(t-t_0)^{0.5} + \sqrt[2n]{\Delta V_{\rm th0}}\}^{2n} \quad (1)$$

$$K_{\rm v} = (\frac{qt_{\rm ox}}{\epsilon_{\rm ox}})^3 K_1^2 C_{\rm ox}(V_{\rm gs}-V_{\rm th})\sqrt{C}\exp(\frac{2E_{\rm ox}}{E_{\rm o}}) \quad (2)$$

$$C = \frac{\exp(-\frac{E_{\rm a}}{kT})}{T_0} \quad (3)$$

Table I shows details of these parameters. The time constant n is between 0.16 (1/6) and 0.25 (1/4)[6]. We evaluate the measurement results by the RD model.

TABLE I
Parameters in Eq. (1)-(3)

K_1	3×10^4[$C^{-0.5}nm^{-2.5}$]	T_0	10^{-8}[$sn^{-1}m^{-2}$]
E_0	0.335[$Vn^{-1}m^{-1}$]	t	stress time[s]
t_0	DC stress start time[s]	$\Delta V_{\rm th0}$	"n" at t_0 ΔV_{th}
n	parameter depends on stress	q	charge[c]
$t_{\rm ox}$	oxide thickness[m]	$\epsilon_{\rm ox}$	dielectric constant
$C_{\rm ox}$	gate capacitance per unit area[F]	$V_{\rm gs}$	voltage between gate and source[V]
$V_{\rm th}$	threshold voltage[V]	$E_{\rm ox}$	vertical electrical field
$E_{\rm a}$	0.49[eV]	k	1.38×10^{-23}[JK^{-1}]

B. Measurement Results of NBTI Degradation by Substrate Biases

From the measurement results of oscillating frequencies over the DC stress time by changing the substrate biases, the degradation of the frequencies is modeled by Eq. (4)

$$f = at^b + f_0 \quad (4)$$

The parameter f in Eq. (4) is the oscillation frequency of ROs and t is the DC stress time. It contains 3 fitting parameters. The parameter b denotes the index of the stress time and f_0 shows the initial oscillation frequency. We calculate the degradation rate (R_{D}) from measurement results by Eq. (5).

$$R_{\mathrm{D}} = \frac{f_0 - f}{f_0}[\%] \quad (5)$$

We evaluate the measurement results based on b, f_0 and R_{D}.

Table II shows the degradation rates for 1,000 s. Fig. 7 shows the fitting parameters "b" according to the substrate biases. We can see whether those measurement result conform with RD theory. The parameter "b" is an index of stress time. According to RD theory, the parameter "b" is between 0.16 and 0.25. The measurement results are consistent with the RD theory except V_{bs} = -0.35 V.

Fig. 8 shows the fitting parameters "f_0" according to the substrate biases. The oscillation frequency is increasing linearly according to the body bias in the forward and reverse regions. It is because V_{th} decreases when the substrate bias goes to forward. As the result, ROs oscillate faster according to the body bias.

Fig. 9 shows the rates of the measured NBTI degradation by the substrate bias of PMOS. The NBTI degradation is accelerated by the forward body bias. But it is almost constant in the reverse body bias. As a result, the NBTI degradation depends on substrate bias in forward body bias. But it does not depend on substrate bias in reverse body bias. So, by Fig. 8 and Fig. 9, there are not interrelation between the operating speed and the degradation rate.

As shown in Fig. 9, the degradation rate in the forward bias region follows the exponential of the bias voltage. Eq. (6) is used to fit the NBTI acceleration rate by the body bias.

$$R_{\mathrm{D}} = k \times \exp(l \times V_{\mathrm{bs}}) + m \quad (6)$$

It has 3 fitting parameters k, l and m. Fig. 10 shows the graph of fitting result. Table III shows parameters of fitting results. According to Fig. 10, the degradation rate is increased exponentially by the forward body bias. But Eq. (6) does not fit degradation rate in reverse body bias.

TABLE II

DEGRADATION RATE R_{D} FOR 1,000 S.

V_{bs} [V]	-0.70	-0.60	-0.50	-0.45	-0.40
R_{D}[%]	0.826	0.770	0.775	0.783	0.674
V_{bs} [V]	-0.35	-0.30	-0.25	-0.20	-0.15
R_{D}[%]	0.712	0.734	0.770	0.731	0.827
V_{bs} [V]	-0.10	-0.05	0.00	0.05	0.10
R_{D}[%]	0.831	0.683	0.711	0.827	0.867
V_{bs} [V]	0.15	0.20	0.25	0.30	
R_{D}[%]	0.812	0.998	1.128	1.602	

TABLE III

FITTING RESULTS k, l, m

k	l	m
0.00976	14.8	0.778

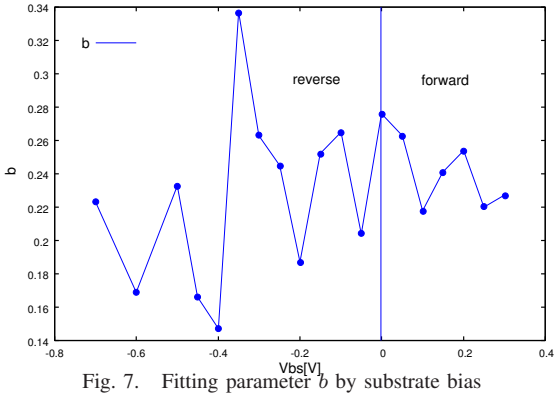

Fig. 7. Fitting parameter b by substrate bias

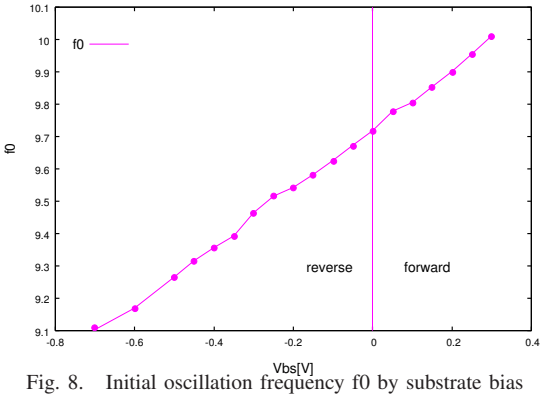

Fig. 8. Initial oscillation frequency f0 by substrate bias

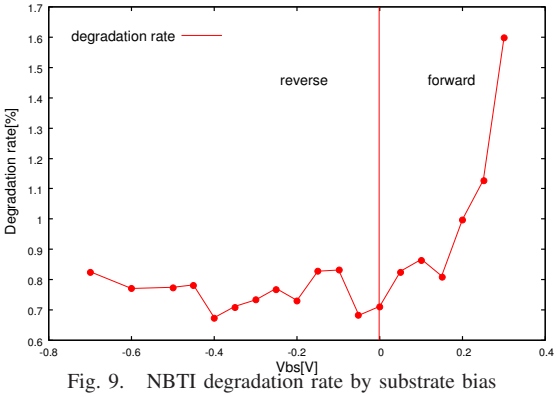

Fig. 9. NBTI degradation rate by substrate bias

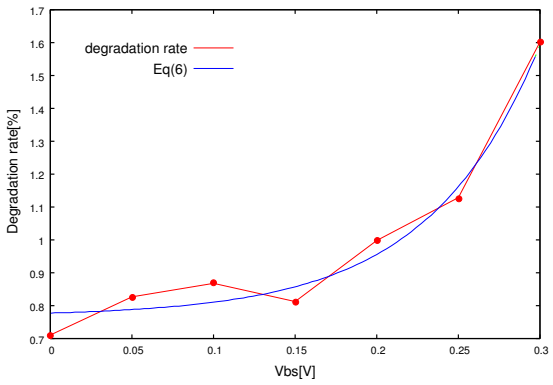

Fig. 10. Fiting results in forward body bias region

IV. CONCLUSION

We measured NBTI degradations by changing the substrate biases of PMOS using 5-stage ROs with four inverters and one NAND gate. The measurement results are consistent with the RD theory, in which the degradation is proportional to the exponential of the stress time. The degradation rate is accelerated according to the forward body bias, while it is almost constant in the reverse body bias. So, the NBTI degradation depends on substrate bias in forward body bias. But it does not depend on substrate bias in reverse body bias. According to these results, there are not interrelation between the NBTI degradation and the operating speed. The degradation rates in forward body bias are proportional to the exponential of the bias voltage.

Acknowledgment: The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

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