Extracting BTI-induced Degradation without Temporal Factors by Using BTI-Sensitive and BTI-Insensitive Ring Oscillators

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***Abstract*—Measuring bias temperature instability (BTI) by ring oscillators (ROs) is frequently used. However, the performance of a semiconductor chip is fluctuated dynamically due to bias, temperature and etc. BTI-sensitive and -insensitive ROs are implemented in order to extract BTI-induced degradation without temporal fluctuation factors. A test chip including those ROs was fabricated in a 65 nm process. BTI-induced degradation without temporal fluctuation was successfully measured by subtracting results of BTI-insensitive ROs from those of BTI-sensitive ones. Performance degradation of NMOS and PMOS transistors mainly due to BTI increases along logarithmic and exponential functions, respectively.**

***Index Terms*—Bias Temperature Instability (BTI), Negative BTI (NBTI), Positive BTI (PBTI), Ring Oscillator (RO)**

I. Introduction

Device sizes of semiconductor chips have been shrinked with the Moore's law [1]. It has brought a lot of advantages, for example, high-performance and low-power electronic gadgets such as smartphones, smart watches and so on. However, reliability problems have appeared in nanometer-scale devices. Particularly, bias temperature instability (BTI) has become a significant concern with the miniaturization of the device size [2]. BTI is one of aging degradation. Transistor performance is degrading with time due to BTI, which results in decreasing timing margins of implemented circuits [3]. BTI-induced degradation accelerates as voltage and temperature increase. BTI is a serious reliability issue that shortens the lifetime of circuits.

There are two types of countermeasures of BTI. One is body bias control during operation [4]. BTI is suppressed with decreasing supply voltage and applying the forward body bias because gate-source voltage ($V_{\rm gs}$) decreases maintaining the same operation speed by forward body bias. However, body bias generators and threshold voltage ($V_{\rm th}$) monitors are required. Another countermeasure is changing circuit topologies. In a previous study, critical path changes and delay time decreases by arranging circuit topologies [5].

BTI measurement circuits to extract BTI-induced degradations without temporal fluctuations are required because measurement results include fluctuation factors from ambient environments. In this paper, BTI-sensitive and -insensitive ring oscillators (ROs) are used to extract BTI-induced degradation without temporal factors. The fluctuation factors are removed by subtracting results of those two type ROs. We explain BTI in section II. Section III shows the structures of those ROs. In section IV, measurement results are presented. Finally, section V shows our conclusion.

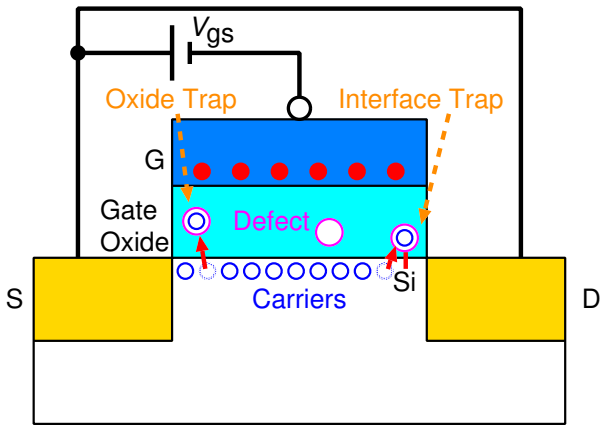

Fig. 1. Atomistic trap-based BTI (ATB) model. BTI occurs when defects trap carriers.

II. Bias Temperature Instability (BTI)

Bias temperature instability (BTI) is one of the aging degradations and transistor performance is degrading with time as voltage and temperature increase [6]–[8]. BTI-induced degradation occurs when defects trap carriers. This degradation can be explained by the atomistic trap-based BTI (ATB) model as shown in Fig. 1 [9], [10]. There are oxygen vacancy defects in the gate oxide and dangling bonds in the interface between the gate oxide and silicon substrate. When these defects trap carriers, the electric field in the gate oxide decreases and drain-source current decreases. Each defect has an individual time constant to trap a carrier. Those time constants are distributed from 10^{-9} s to 10^{9} s [10]. Particularly, defects with large time constants affect aging degradations induced by BTI. BTI-induced degradation is recovered when carrier emission is promoted as $V_{\rm gs}$ is reduced because trapped carriers in the gate oxide are easily emitted to channel.

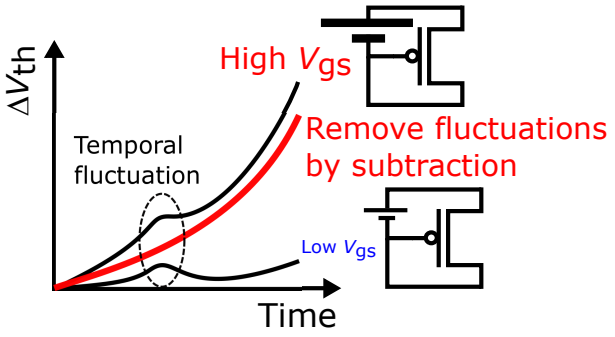

Fig. 2. BTI-induced degradation in Higher and lower gate-source voltage ($V_{\rm gs}$). Temporal fluctuations are removed by subtracting results of Higher and lower $V_{\rm gs}$.

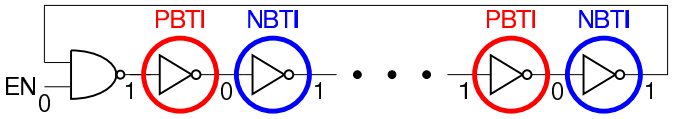

Fig. 3. An inverter-based ring oscillator (RO). PBTI and NBTI occurs in every other inverters when the RO stops. NAND gate is to control oscillation.

There are negative BTI (NBTI) and positive BTI (PBTI). NBTI occurs on PMOS when $V_{\rm gs}$ is negative. Likewise, PBTI is observed on NMOS especially in technologies with high-k (HK) gate dielectrics [11].

BTI-induced degradation is accelerated as $V_{\rm gs}$ increases as shown in Fig. 2. BTI-induced degradation with higher $V_{\rm gs}$ is larger than that with lower $V_{\rm gs}$. However, temporal fluctuations affect both ROs. BTI-induced degradation without temporal factors are extracted by taking difference between BTI-sensitive and -insensitive ROs.

III. Measurement Circuits

An inverter-based RO is shown in Fig. 3. The leftmost NAND-gate controls oscillation by one of input pins (EN) in the NAND-gate. The RO oscillates when EN is high and stops when EN is low. The RO suffers from BTI when it stops oscillation. The nodes between the inverters are alternately fixed to 0 or 1. It means PBTI and NBTI occur every other inverters.

PBTI becomes dominant since all inverters are replaced to NAND-gates as shown in Fig. 4. When EN is high, all outputs of NAND-gates are 1. On the other hand, NBTI becomes dominant in the RO composed of NOR-gates as shown in Fig. 5. Oscillation is controlled by ENB. When ENB is high, all outputs of NOR-gates are 0 to accelerate only NBTI.

Sensitivities to BTI can be changed by changing input connections. Figure 6 shows two-types of NAND ROs in the transistor level. NMOS is connected in series from the output terminal to ground (GND). NMOS connected to the output pin is $\rm NMOS_{OUT}$ and that connected to GND is $\rm NMOS_{GND}$. In Fig 6 (a), the gate terminals of $\rm NMOS_{OUT}$ and $\rm NMOS_{GND}$ are connected to EN and the output pins of previous stages, respectively. When EN is low, all output pins of NAND-gates become 0. PBTI is accelerated in $\rm NMOS_{GND}$ in all stages

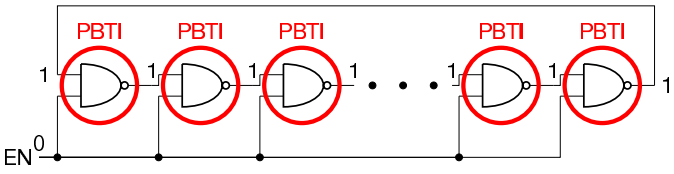

Fig. 4. RO composed NAND gates. PBTI becomes dominant when RO stops.

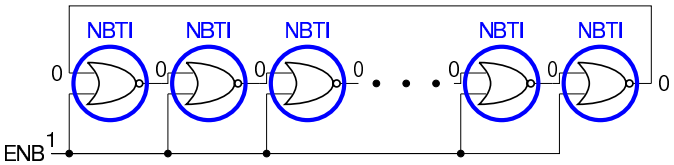

Fig. 5. RO composed NOR gates. NBTI becomes dominant when RO stops.

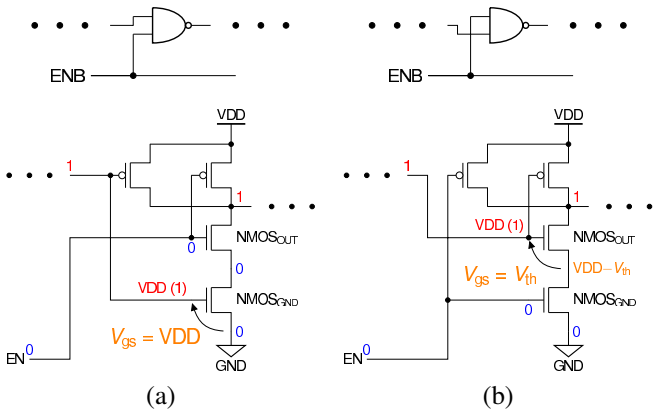

Fig. 6. NAND RO in transistor level. (a) PBTI-sensitive RO. (b) PBTI-insensitive RO.

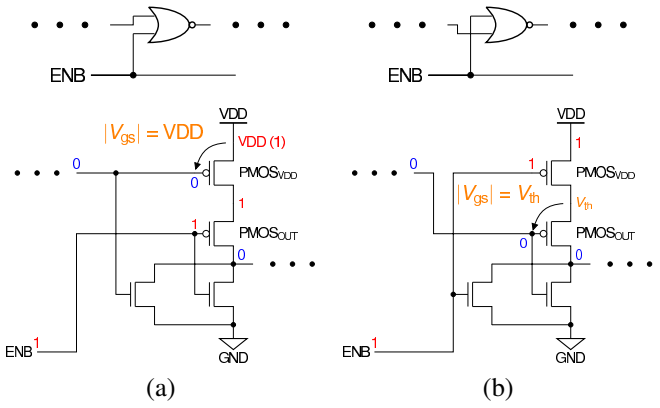

Fig. 7. NOR RO in transistor level. (a) NBTI-sensitive RO. (b) NBTI-insensitive RO.

because the $V_{\rm gs}$ become supply voltage (VDD). Here this RO is called the PBTI-sensitive RO.

PBTI is suppressed by changing input connections on the PBTI-insensitive RO as shown in Fig 6 (b). Gate terminals of those NMOS are exchanged between EN and the output pins of previous stages. When EN is low, $V_{\rm gs}$ of $\rm NMOS_{OUT}$ is decreased to threshold voltage ($V_{\rm th}$) instead of VDD. Although PMOS connected to EN suffers from NBTI, the oscillation frequency does not change because it is determined by delay time in MOSFETs connected to the output pins of the previous

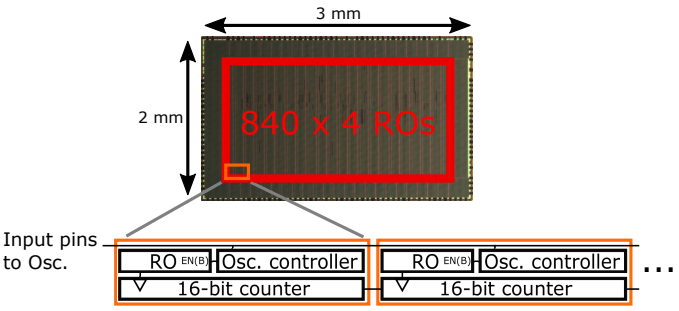

Fig. 8. Test chip micrograph. The number of oscillations is counted by embedded 16-bit counter.

TABLE I
FABRICATED RO STRUCTURES.

Structure	Figure	Number of ROs
PBTI-sensitive	Fig. 6 (a)	840 in all ROs
PBTI-insensitive	Fig. 6 (b)	
NBTI-sensitive	Fig. 7 (a)	
NBTI-insensitive	Fig. 7 (b)	

stages. This PBTI-insensitive RO suppresses PBTI because of lower $V_{\rm gs}$ than that in PBTI-sensitive RO.

Likewise, NBTI is suppressed by arranging the input connections in NOR ROs as shown in Fig. 7. Gate terminals of $\rm PMOS_{OUT}$ and $\rm PMOS_{VDD}$ are connected to ENB and to the output pins of previous stages, respectively as shown in Fig. 7 (a). When ENB is high, $\rm PMOS_{VDD}$ suffers from NBTI. NBTI is suppressed by changing input connections as shown in Fig. 7 (b). $|sV_{\rm gs}|$ of $\rm PMOS_{OUT}$ is decreased to $V_{\rm th}$. These ROs are named as the NBTI-sensitive RO and the NBTI-insensitive RO, respectively.

They were fabricated in a 65 nm fully depleted silicon-on-insulator (FDSOI) process and BTI-induced degradations of them were measured. Table I shows fabricated RO structures.

Figure 8 shows a chip micrograph of the test chip. The chip size is 3×2 mm^2 in which 840×4 11-stage ROs are embedded. Oscillation of ROs is controlled by the oscillation (Osc.) controller and input pins. The number of oscillations is counted by the 16-bit counter. Those controller and counter are mainly composed by standard flip-flops. Each RO has its own controller and counter. They formed a unit that is connected in series. The number of oscillation in counters are measured and oscillation frequencies are calculated by dividing oscillation time.

IV. MEASUREMENT RESULTS

Figure 9 shows a measurement flow to measure BTI-induced degradations. ROs oscillate for 12 μs in the order of gigahertz. Those stop oscillation for over 20 s for BTI stress after measuring frequencies. ROs suffer from BTI stress when it stop oscillation. Frequencies are measured every time after BTI stress. The oscillation and BTI stress are repeated. The measurements are performed at a temperature of 80 °C and a

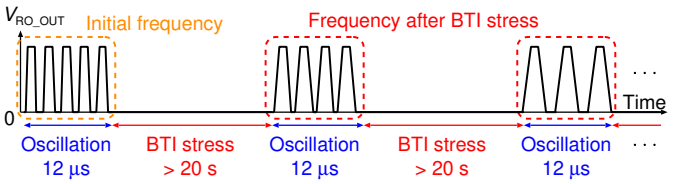

Fig. 9. Measurement flow of BTI-induced degradations.

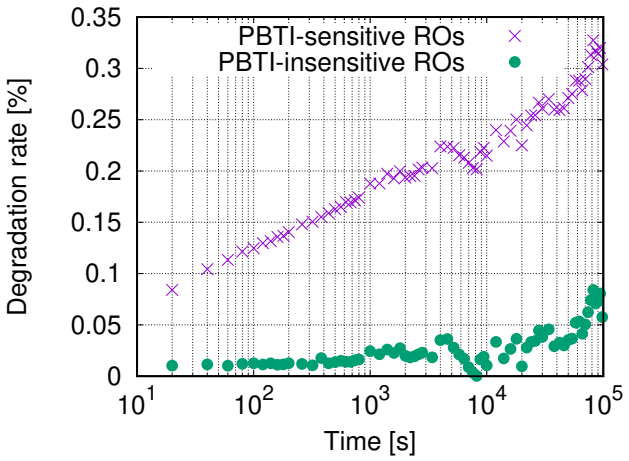

Fig. 10. Measurement results of PBTI-induced degradation.

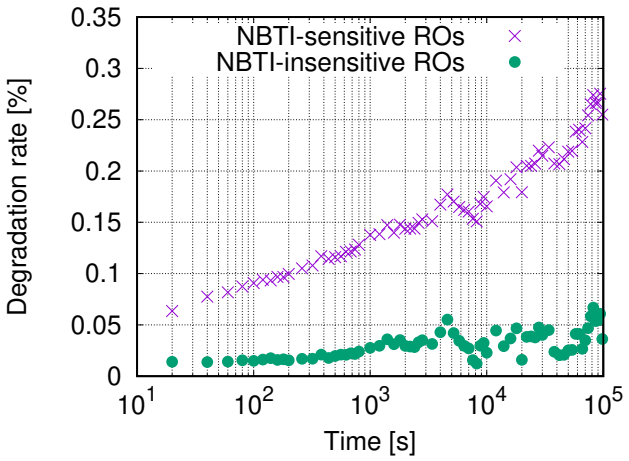

Fig. 11. Measurement results of NBTI-induced degradation.

supply voltage of 2.0 V to accelerate BTI-induced degradation. Degradation rate ($D_{\rm rate}$) is calculated as

$$D_{\rm rate} = \frac{f_0 - f(t)}{f_0}\ , \qquad (1)$$

where f_0 is the initial frequency at $t = 0$ and $f(t)$ is the measured frequency at time t.

Figure 10 shows the measured BTI-induced degradations in NAND ROs for PBTI-induced degradation. The X-axis and the Y-axis show the BTI stress time and $D_{\rm rate}$, respectively. $D_{\rm rate}$ is averaged in 840 ROs. The $D_{\rm rate}$ values of PBTI-sensitive ROs [in Fig. 6 (a)] increase with time. However, The $D_{\rm rate}$ of PBTI-insensitive ROs [in Fig. 6 (b)] is almost constant. The degradation of BTI-sensitive ROs is 5x larger than that of BTI-insensitive ROs at 10^5 s. Figure 11 shows the measurement

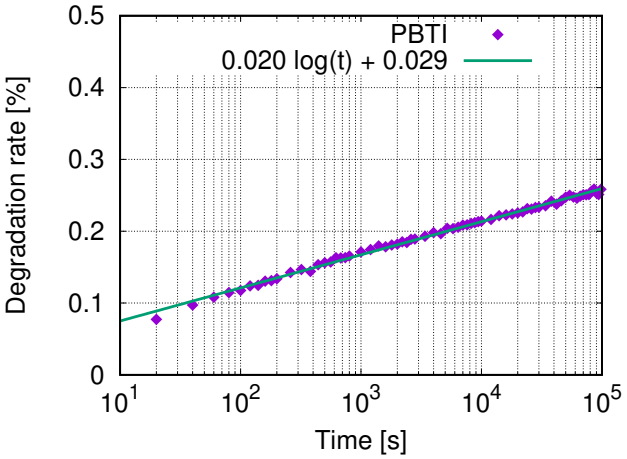

Fig. 12. Difference between PBTI-sensitive and -insensitive ROs.

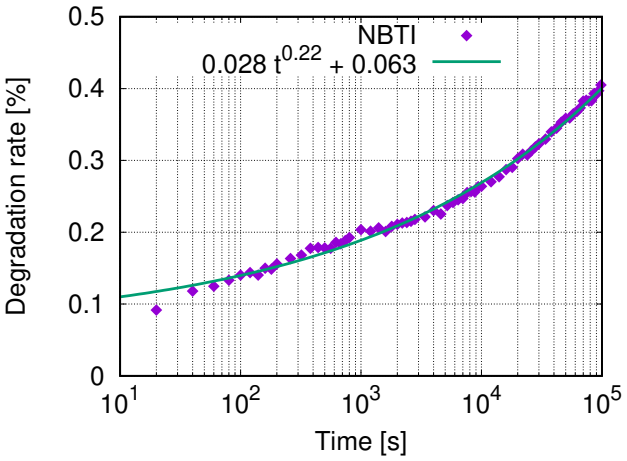

Fig. 13. Difference between NBTI-sensitive and -insensitive ROs.

results in NOR ROs for NBTI stress. NBTI is also suppressed by arranging input connections like NAND ROs.

These results are dynamically fluctuated mainly due to temperature or voltage fluctuations. For example, D_{rate} suddenly increased at 5 ks and decreased at 10 ks. Both results from BTI-sensitive and -insensitive ROs are correlated. Those fluctuation can be removed by subtracting BTI-insensitive results from BTI-sensitive ones. Figures 12 and 13 show the difference in NAND and NOR ROs, respectively. Fluctuations are removed and D_{rate} clearly increases with time. The PBTI-induced degradation increases according to logarithmic functions, while the NBTI-induced degradation exponentially increases with stress time.

V. Conclusions

BTI-sensitive and BTI-insensitive ROs are used to extract BTI-induced degradations without fluctuations of ambient environments. The test chip was fabricated in the 65 nm process and BTI-induced degradations were measured. The degradation of PBTI/NBTI-sensitive ROs is five times larger than PBTI/NBTI-insensitive ROs at 10 ks. Fluctuation originated from ambient environments are successfully removed by subtracting results of BTI-insensitive ROs from those of BTI-sensitive ones. PBTI- and NBTI-induced degradation increases logarithmic and exponential functions, respectively.

Acknowledgments

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