SEU Sensitivity of PMOS and NMOS Transistors in a 65 nm Bulk Process by α -Particle Irradiation

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Abstract—We consider a method to measure the Single Event Upsets (SEU) sensitivity individually for PMOS and NMOS transistors. Using a circuit fabricated in a 65 nm bulk process, we performed α -particle irradiation. The SEU sensitivity of PMOS transistors is approximately 1/50 of that of NMOS transistors. Additionally, we investigated SEU rates by the drain area. The relationship between the area and SEU rates does not follow a linear function. We consider this phenomenon due to the proximity of the drain area to shallow trench isolation (STI), which prevents charge collection by a radiation strike.

Index Terms—flip-flop, soft error, TCAD, device simulation, α -particle, Single Event Upsets (SEU)

I. INTRODUCTION

Reliability issues such as radiation-induced soft errors become more serious with technology down scaling [1]. Soft errors are one of the temporal failures that upset stored values in storage elements such as flip-flops (FFs) or SRAMs caused by a radiation strike. Soft errors are classified into two types based on the location of a radiation strike: Single Event Transients (SET) occurring in combinational circuits and Single Event Upsets (SEU) occurring inside storage elements. To improve the soft error tolerance of storage elements, several redundant circuits such as the dual interlocked storage cell (DICE) [2] [3] have been proposed. However the number of transistors of these FFs is significantly larger than that of a standard FF, and the performance overhead is large. Therefore, it is necessary to take countermeasures without redundancy.

The SEU sensitivity is influenced by the area of the drain region [4]. Additionally, [5] [6] propose the method to enhance soft error tolerance by increasing the critical charge $(Q_{\rm crit})$ on vulnerable nodes. Investigating the correlation between these two factors and soft error tolerance is important for designing radiation-hardened circuits without redundancy.

In previous research, the SEU sensitivity measurement method using the stack structure was proposed [7]. This method compares the SEU sensitivity of PMOS and NMOS transistors by using three types of latches and taking the difference of the generated errors. However, each latch has different load capacitance and different $Q_{\rm crit}$. This measurement method is only applicable to FD-SOI processes that allow the use of the stack structure and cannot be used in planer bulk processes.

In this paper, we consider a method for measuring the SEU sensitivity individually for PMOS and NMOS transistors.



Fig. 1: Structure for measuring SEU sensitivity of the PMOS transistor. If a pulse is generated in the NMOS transistor, the output does not fall below the intermediate voltage.



Fig. 2: Structure for measuring SEU sensitivity of the NMOS transistor. If a pulse is generated in the PMOS transistor, the output does not exceed the intermediate voltage.

Furthermore, we designed measurement circuits using a 65 nm bulk process and evaluated the SEU sensitivity of PMOS and NMOS transistors by α -particle irradiation experiments.

II. MEASUREMENT CIRCUIT

In this study, we used an inverter with a resistor inserted between transistors. Figs. 1 and 2 show the circuit structure for measuring the SEU sensitivity of PMOS and NMOS transistors, respectively. The resistance is set to three times larger than the ON resistance of the target transistor to be measured. Even if a SET pulse is generated from the isolated transistors, the output does not exceed the intermediate voltage (0.6 V = 1/2 VDD). Therefore, we can measure the SEU sensitivity of PMOS or NMOS transistor individually. We construct the latch circuits as shown in Fig. 3 using this structure. PMOS or NMOS transistors to be evaluated are connected to the output node.



(a) Latch for the PMOS transis- (b) Latch for the NMOS transistor. tor.

Fig. 3: Two types of the proposed latches.

We confirmed that the errors can be separated through device simulations using TCAD Sentaurus from Synopsys. For two types of the proposed latch, a heavy ion with linear energy transfers (LET) = $60 \text{ MeV-cm}^2/\text{mg}$ is injected. To demonstrate the proposed structures can block the errors from the isolated transistors regardless of radiation particles, we used high-energy heavy ions in this simulation. The waveforms of the outputs are shown in Fig. 4. The pulses generated in the isolated transistors are attenuated by the resistors, and then the output does not flip.

The fabricated FFs based on the latches in Fig. 3 are shown in Figs. 5 and 6. They are based on the adaptive coupling FF (ACFF) [8] as shown in Fig. 7. ACFF is a circuit designed for low-power operation, and it has no radiation hardness. The secondary latch of ACFF was replaced with the proposed latch. To stabilize the write operation, inverters were added. Furthermore, the addition of output QB balances the load capacitance and symmetrizes the latch. Therefore, in this study, the SEU sensitivity was evaluated only under the condition (Q, CLK) = (0, 0).

For each measurement circuit, we designed three types of FFs by changing the area of the drain regions (standard, 2x, 4x) in Fig. 9 and modifying $Q_{\rm crit}$ (8, 11, 14 fC) by adding capacitance in Fig. 8. $Q_{\rm crit}$ of the standard circuit is 8 fC.

The current source used to evaluate Q_{crit} in simulations is the single exponential model in Eq. (1) [9]. *T* in Eq. (1) refers to the time constant determined by a process node. *T* is set to 20 ps, corresponding to a 65 nm process [4].

$$I(t) = Q \frac{2}{T\sqrt{\pi}} \sqrt{\frac{t}{T}} \exp\left(-\frac{t}{T}\right).$$
(1)

III. EXPERIMENTAL RESULT

A. α Particle Irradiation

All designed FFs were implemented as shift registers. The number of errors generated in all FFs was evaluated through α -particle irradiation tests. The irradiation tests were conducted as follows.

- 1) Initialize serially-connected FFs by all 0.
- 2) Stabilize CLK to 0.



(a) Pulses generated from the PMOS transistor in each latch. Even if a pulse is generated in the latch for the NMOS transistor, the output does not flip.



(b) Pulses generated from the NMOS transistor in each latch. Even if a pulse is generated in the latch for the PMOS transistor, the output does not flip.

Fig. 4: Results of TCAD simulations.

- 3) Expose α -particle to FFs.
- 4) Read out stored data of FFs.
- 5) Count the number of upsets.

The experiments were conducted by placing an α -particle source on the chip, as shown in Fig. 10. The α -particle irradiation tests were conducted under the following conditions:

- 1) Radiation source used: 3 MBq ²⁴¹Am.
- 2) Supply voltage: Standard voltage of 1.2 V.
- 3) Measurement duration: 120 hours.

Figs. 11 and 12 show the number of errors observed in the NMOS or PMOS transistor with error bars of 95% confidence at Vdd = 1.2 V. Comparing the results for an area 4 times larger with relatively small error bars, the SEU rates for the PMOS transistors was approximately 1/50 of those for the NMOS transistors. SEU rates of the NMOS transistors increased by 12 times when the area was doubled and by 25 times when the area was quadrupled. On the other hand, the SEU rates of the PMOS transistors increased by 26 times when the area was quadrupled. The increase rate of SEU rates with respect to the drain area differs between the NMOS and PMOS transistors. It was found that the relationship between the drain area and SEU rates is not linear. Furthermore, in the



Fig. 5: Measurement circuit for the PMOS transistor.



Fig. 6: Measurement circuit for the NMOS transistor.



Fig. 7: ACFF (Adaptive Coupling FF)



Fig. 8: Measurement circuit with modified Q_{crit} by adding capacitance.

circuits with Q_{crit} increased to 11 fC and 14 fC, no error was observed for both the NMOS and PMOS transistors.

B. Discussions

From these results, it was revealed that SEU rates in the PMOS and NMOS transistors do not have linear relationship with the area of the drain region. We investigated the reason of these results by using TCAD. Fig. 13 shows a cross-sectional view of a transistor when a particle hits diagonally. When the particle hits, it generates electron-hole pairs. The higher the LET value of the particle, the greater the amount of charge is generated. We evaluated the threshold LET values of the standard circuit and the circuit with 2x area. Threshold LET values are obtained by irradiating heavy ions vertically at



Fig. 9: Location of expanded the drain area.



Fig. 10: α -particle irradiation test

the center of the drain region under evaluation at 0.1 MeVcm²/mg resolutions. Higher threshold LET values indicate greater soft error tolerance. Threshold LET values of the standard circuit is approximately 6 times larger than that of the circuit with 2x area. The closer the distance between the gate and shallow trench isolation (STI), the more likely the electric charge collection will be blocked by the STI. α -particles emitted from the α -radiation source not only hit perpendicularly to the chip but also diagonally. Therefore, it can be inferred that the SEU rate of the standard circuit is the lowest of all.

In the circuit with increased $Q_{\rm crit}$, no error was observed under α -particle irradiation. Using TCAD, we evaluated the threshold LET values for circuits with increased $Q_{\rm crit}$. The results are presented in Table I. Through TCAD simulations, it was observed that the threshold LET value for these circuits is larger than the LET value of α -particles near the Bragg's peak (1.4 MeV-cm²/mg) [10]. In these measurement circuits, it can be concluded that no error is observed by α -particle radiation for $Q_{\rm crit}$ values greater than 11 fC. These circuits need to be evaluated with other radiation sources, such as neutrons.

TABLE I: TCAD simulation results of threshold LET

$Q_{\rm crit}$ of each circuit [fC]	Threshold LET [MeV-cm ² /mg]
8 (standard)	0.6
11	1.9
14	2.5



Fig. 11: SEU rates of the PMOS transistor measurement circuit. Error bars are within 95% confidence.



Fig. 12: SEU rates of the NMOS transistor measurement circuit. Error bars are within 95% confidence.



(a) Cross-sectional view of the (b) Cross-sectional view of the standard circuit when exposed circuit with 2x area when exto particles. posed to particles.

Fig. 13: Charge collection is blocked by STI. Threshold LET value in the standard circuit is 3.8 MeV-cm²/mg. The STI blocks charge collection. Threshold LET value in the circuit with 2x area is 0.6 MeV-cm²/mg. Compared to the standard circuit, the charge is more easily collected.

IV. CONCLUSION

In this paper, we investigated a method for individually measuring the SEU sensitivity of the PMOS and NMOS transistors. By inserting a resistor between the transistors for isolation, we ensured that even if a SET pulse is generated in the isolated transistor, the output does not flip. Through device simulations using TCAD, we confirm that errors can separated using this structure and designed circuits based on it in the 65 nm bulk process. The results from α -particle irradiation showed that SEU sensitivities to the drain area are different between the NMOS and PMOS transistors. Also the SEU rates for the PMOS transistors were approximately 1/50 of those for the NMOS transistors. Furthermore, we observed that the relationship between drain area and SEU rates was not linear. When the distance between the gate and STI is shorter, charge collection is blocked when a particle hits on a transistor diagonally.

In the circuit with increased Q_{crit} , no error was observed under α -particle irradiation. Through TCAD simulations, it was observed that the threshold LET values for circuits with $Q_{\rm crit}$ = 11, 14 fC are larger than the LET value of α -particle. In these measurement circuits, it can be concluded that no error is observed by α -particle radiation for $Q_{\rm crit}$ values greater than 11 fC. These circuits need to be evaluated with other radiation sources, such as neutrons.

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