Frequency Dependency of Soft Error Rates Based on Dynamic Soft Error Measurements

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***Abstract*—We conducted a study on the frequency dependence analysis of soft error rates using flip-flops (FF) and inverters. The measurement circuit consists of scan FFs and inverters. By irradiating the circuit with alpha particles while the clock was running, the soft error rates were measured. The results showed that soft errors caused by inverters were almost negligible. On the other hand, the soft errors caused by FFs decreased as the operating frequency increased. The time window when the FF cannot capture its input until the rising edge of the clock is fixed at any clock frequency. As a result, as the operating frequency increases, the ratio of where errors are not captured to time in one cycle becomes larger.**

***Index Terms*—flip-flop, inverter, soft error, operating frequency, dynamic soft error measurement, SET, SEU**

I. Introduction

In recent years, the miniaturization of transistors has led to a decrease in reliability, which has become a concern [1]. One of the factors contributing to this reliability degradation is soft errors. Soft errors occur when radiation strikes the transistors within integrated circuits, causing the stored values of latches or flip-flops (FF) to flip [2]. The cause of soft errors can be classified into two types: Single Event Transients (SET) occurring in combinational circuits and Single Event Upsets (SEU) occurring within storage elements. As the operating frequency increases, the proportion of SET in the overall soft errors has increase [3]. Measuring the soft error rate for each operating frequency is crucial for designing better soft error resilient systems.

Conventional static soft error measurements involve stopping the clock of FF for the measurement, allowing observation of only SEUs [4]. However, soft errors that occur in actual operating environments can also be influenced by SET events that happen outside of the FFs. By relying solely on static soft error measurements, it is impossible to observe the error rate that aligns with the actual operation. The dynamic soft error measurement conducted in this study allows for observation of both SET and SEU, as the clock keeps on running during the measurement.

This paper consists of two major parts. First, we propose a circuit structure for measuring soft error rates while keeping the clock operational. We will explain the dynamic soft error measurement circuit, clock signal transmission circuit, and oscillator circuit. In second part, we will present the experimental results using alpha particles and discuss their analysis.

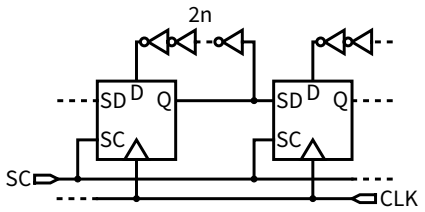

Fig. 1. Dynamic soft error measurement circuit

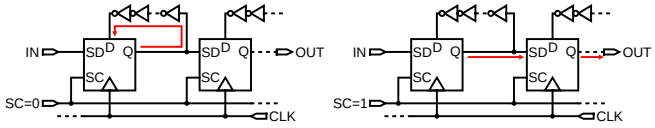

Fig. 2. Circuit operation

II. Measurement Circuit

In this chapter, we describe the circuit structure used for dynamic soft error measurements, composed scan FFs and inverters.

A. Dynamic soft error measurement circuit

In dynamic soft error measurements, the clock(CLK) is continuously applied during the measurement. Simply cascading FFs as in regular soft error measurements would lead to signal propagation to the next stage, preventing signal retention. Therefore, a circuit that loops and retains the signal within the FF is mandatory. In this study, we enabled dynamic soft error measurements by using scan FFs. Scan FFs are circuits in which, when SC = 0, the input D is captured, and when SC = 1, the input SD is captured [5]. Fig. 1 shows the circuit diagram of the dynamic soft error measurement circuit, and Fig. 2 illustrates its operation. When SC = 0, D = Q, the FF's output becomes its own input, enabling signal looping and allowing dynamic soft error measurements. When SC = 1, Q becomes the next stage's SD, making it possible to read out errors.

B. Clock signal transmission circuit

During dynamic soft error measurements, high-speed clocks of the order of GHz are used as input, necessitating circuits capable of transmitting high-speed clocks. When reading out the measurement results during the shift operation, it is essential to avoid hold violations. Furthermore, transmitting

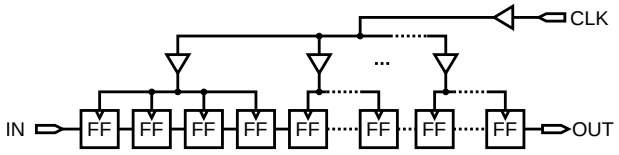

Fig. 3. Clock Tree

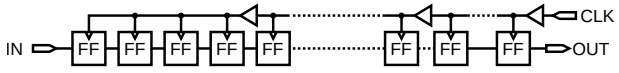

Fig. 4. Buffer chain

the clock to a large number of FFs raises concerns about the timing of clock inputs and dynamic current. Therefore, some kind of a new clock propagation circuit is required in the clock transmission method.

There is also a method of using decap cells to avoid IR drop [6]. However, we did not use this method in this study to integrate as many FFs as possible on the chip.

There are two existing methods for clock transmission: the clock tree and the buffer chain [7] [8]. Fig. 3 illustrates the circuit diagram of the clock tree, while Fig. 4 shows the circuit diagram of the buffer chain.

The clock tree allows simultaneous clock input to all FFs, eliminating the need to consider clock skew. However, a large number of FFs are used in the dynamic soft error measurement circuit, unlike conventional LSIs. Transmitting the clock to all FFs simultaneously would result in a sudden surge of current, causing IR drop and risking the circuit's malfunction. On the other hand, the method of propagation using buffer chains allows for the equalization of instantaneous current by shifting the timing of clock transmission. However, clock skew must be taken into consideration. When multiple stages of buffers are connected to transmit high-frequency signals, the clock may disappear (Fig. 5). Therefore, using a large number of stages in the buffer chain is not feasible. Therefore, in this measurement, we utilized the circuit shown in Fig. 6, which combines the buffer chain and the clock tree.

C. Oscillator circuit

Generally, Phase Locked Loop (PLL) circuits are used in oscillator circuits [9]. However, PLLs have complex circuit structures. In this measurement, a circuit capable of setting finely detailed frequencies at high frequencies is required to

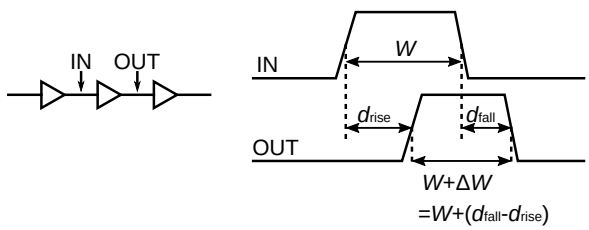

Fig. 5. Pulse width narrowing phenomenon

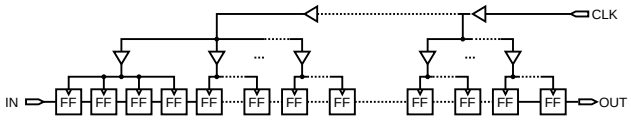

Fig. 6. Implemented clock transmission circuit

measure soft errors at each frequency. Therefore, a circuit combining seven ring oscillators and dividers was employed. The measurable frequencies range from 8.0 to 1812MHz, with 56 steps.

The chip developed this time incorporates 4,600 stages of the dynamic soft error measurement circuit mentioned above. Additionally, the clock tree consists of 128 FF stages each, and we created the clock transmission circuit by connecting each clock tree using a 36-stage buffer chain. The measurement package contains four mounted dies with the above circuit.

III. Experimental Methods

A chip equipped with the circuit described in the previous chapter was fabricated in the 65 nm bulk process, and its soft error torelance was evaluated by alpha particle irradiation. The alpha particle source had a radioactivity of 3 MBq and consisted of ^{241}Am. The V_{DD} for the chip was set to the standard voltage of 1.2 V, and measurements were conducted at each frequency for 30 seconds, with a total of 300 measurements.

Here is an explanation of the measurement procedure.

1) Place the alpha particle source on top of the circuit.
2) Write values into the measurement circuit and leave it for a certain period.
3) For dynamic soft error measurements, keep the clock running during this period.
4) After the designated measurement time has passed, read the stored values and record the number of errors.

IV. Measurement Results

A. Static soft error measurement

The error rates were measured with the clock fixed at 0 and 1, respectively, for cases where the input signal was 0 and 1. This measurement is conducted using a method similar to the conventional soft error measurement [4]. The clock transmission circuit combines the clock tree and the buffer chain. For that reason, we defined "1 block" as 128 FF stages that transmit the clock in a single clock tree, and we aggregated the error rates for each block. The measurement results are shown in Figs. 7 and 8. Fig. 7 shows the error rate for each value of the clock signal CLK and the input signal D. Fig. 8 shows the error rate for each block when both CLK and D are 0.

The measurement results showed slightly different error rates for each block. Even when repeating the measurements, similar trends in the values were observed. Therefore, We consider that these variations are due to process variation.

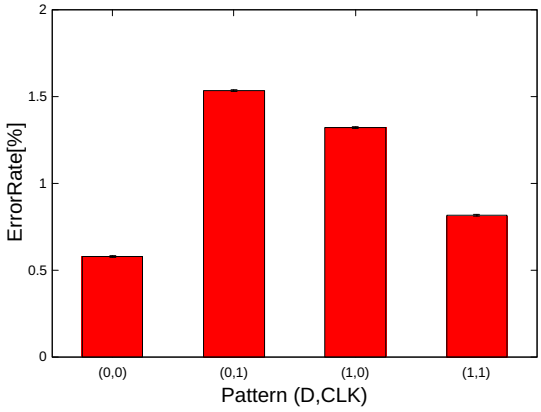

Fig. 7. Results of static soft error measurement

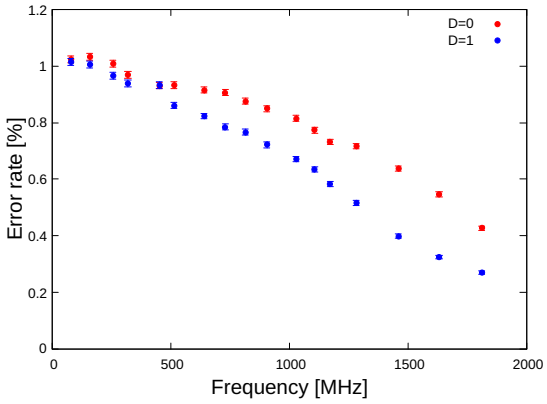

Fig. 9. Dynamic soft error rate within the range of blocks 32 to 36

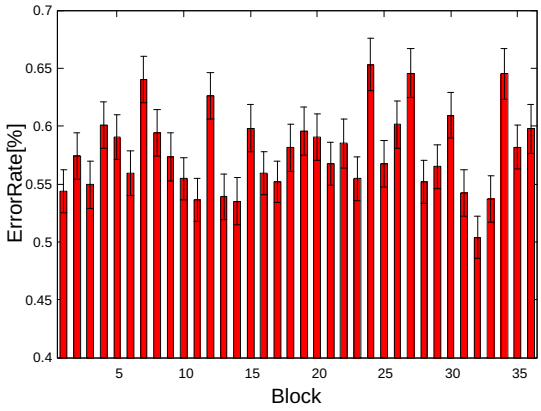

Fig. 8. Error rates for each block when both the input signal and clock signal are 0

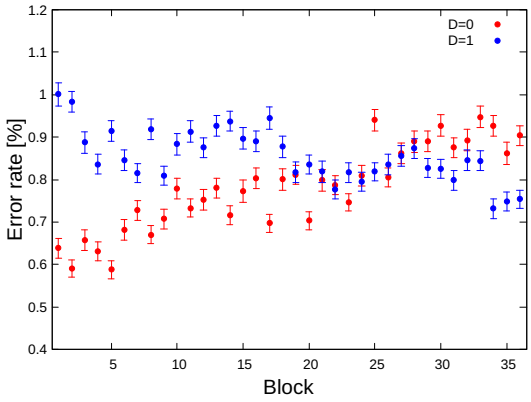

Fig. 10. Error rates for each block at 730 MHz

B. Dynamic soft error measurement

Using an oscillation circuit, we measured the error rate with the clock input to the measurement circuit. Similar to the static soft error measurement, we measured the error occurrence rate for each block. The measurement results for the error rates of five blocks, are shown in Fig. 9. These five blocks were still receiving clock signals even when the operating frequency was set to its maximum for measurement. Regardless of whether the input value was 0 or 1, the error rate decreases as the operating frequency increases. When the operating frequency is 906 MHz, the error rate decreased by approximately 18% under the condition of D = 0 compared to 0 MHz. Under the condition of D = 1, the error rate decreased by about 32%.

Fig. 10 depicts the error rates for each block at 730 MHz, where the clock was transmitted to all blocks. The error rates for each block exhibit a linear change. This is because the duty cycle decreases for each block due to the pulse width narrowing phenomenon.

When a high-frequency clock signal was input to the circuit, the clock signal did not propagate to all blocks. Fig. 11 shows the relationship between the one clock period and the number of transmitted blocks.

As the one-cycle time of the clock signal becomes shorter, the number of blocks where the signal propagates decreases linearly.

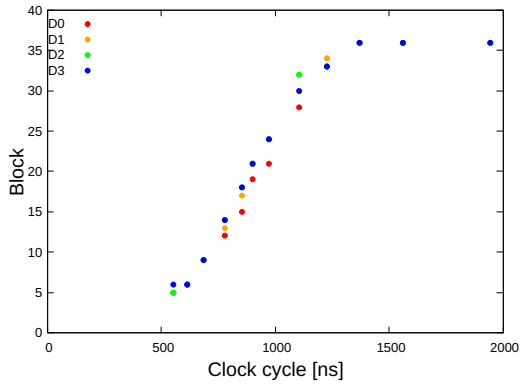

Fig. 11. Clock cycle v.s. the number of transmitted blocks

V. Discussion

The above results alone do not allow us to distinguish between SET and SEU. Therefore, we derive the SEU error rate from the values obtained during static soft error measurements and compare it to obtain the SET error rate.

Here is the procedure for derivation of SEU when D=0. When CLK = 0, the same errors occur as in the static measurement at D = 0, CLK = 0, and when CLK = 1, the same errors occur as in the static measurement at D = 0, CLK = 1. In other words, the duty cycle of the clock signal input to the FF must be obtained to determine the SEU error rate. However, in this circuit, we need to consider the pulse narrowing effect (Fig. 5), which affects the duty cycle. Additionally, we must take into account the delay within the measurement circuit. Errors that occurred just before the rising edge of the clock cannot be saved. This is because the next clock arrives at the FF before the inverted signal is input to D. Moreover, we need to consider the possibility that the duty cycle may vanish rapidly when the clock width becomes smaller than a certain threshold.

In this circuit, the pulse width reduction per stage can be estimated to be approximately 11 ps, based on the variation of error rates for each block in Fig. 10. By SPICE simulations, the delay time between Q and D in the measurement circuit is found to be approximately 300 ps. Using these values, the calculated SEU results are shown in Fig. 12. Up to 1 GHz, the calculated values generally match well with the measured values. However, beyond 1 GHz, there is a significant deviation from the calculated values. In this circuit, a ring oscillator and a frequency divider are used to create the clock signal. For frequencies over 1 GHz, the signal from the ring oscillator is directly input as the clock without passing through the frequency divider. Consequently, at frequencies beyond 1 GHz, the input clock signal does not have a duty ratio of 0.5, which is why the error rate deviates from the calculated value.

From the agreement between the measured values below 1 GHz and the calculated values for SEU, it can be inferred that SET is almost not occurring in this circuit. This is likely due to the low-energy alpha particles used in the experiment, resulting in smaller SET pulse widths during irradiation. In the future, we plan to conduct measurements using higher-energy heavy ions to verify the variation in error rates based on energy levels.

VI. Conclusions

A circuit using scan FFs and inverters was designed, and the soft error rates at each frequency was evaluated through alpha-particle irradiation experiments. In the alpha-particle irradiation, errors due to SET were almost negligible. In the proposed circuit, SEU decreased by approximately 18% under the D=0 condition and by about 32% under the D=1 condition when the operating frequency was 906 MHz compared to 0 MHz. Therefore, in the case of alpha-particle irradiation, if the circuit does not heavily rely on combinational logic, the impact of SET can be ignored. Additionally, SEU is significantly affected by the delay time of combinational circuit. As the operating frequency increases, the SEU decreases linearly, resulting in a lower error rate during circuit operation compared to the value observed in static soft error measurements. In the critical path, the delay time increases, so there is less need to significantly increase soft error tolerance.

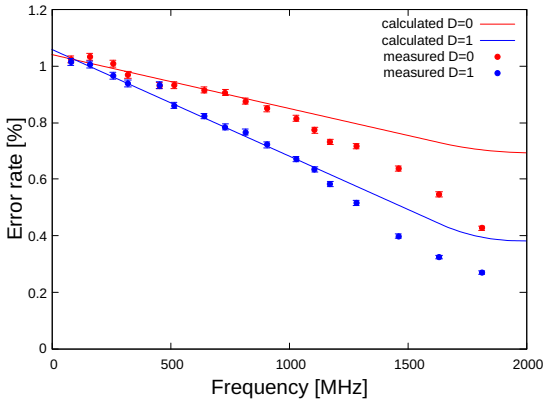

Fig. 12. Comparison between calculated and measured values of SEU

VII. Acknowledgment

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