Circuit-level Simulation Methodology for Random Telegraph Noise by Using Verilog-AMS

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***Abstract*—As device sizes are downscaled to nanometer, Random Telegraph Noise (RTN) becomes dominant. It is indespensable to accurately estimate the effect of RTN. We propose the RTN simulation method for analog circuits. It is based on the charge trapping model. We replicate the RTN-induced threshold voltage fluctuation to attach a variable DC voltage source to the gate of MOSFET by using Verilog-AMS. We confirm that drain current of MOSFETs temporally fluctuates. The fluctuations of RTN are different for each MOSFET. Our proposed method can be applied to estimate the temporal impact of RTN including multiple transistors. We can successfully replicate RTN-induced frequency fluctuations in 3-stage ring oscillators as similar as the measurement results.**

***Keywords*—RTN, Defect, Threshold voltage, Verilog-AMS**

I. Introduction

As the CMOS technology is downscaled, reliability issues are becoming more serious [1]. Random telegraph noise (RTN) is one of those issues caused by scaling. RTN is a phenomenon that fluctuates threshold voltage ($V_{\rm th}$) when the gate bias is applied to MOSFET [2], [3]. It is reported that RTN has a severe impact on semiconductor chips. such as CMOS image sensors [4], flash memories [5] and SRAMs [6]. The impact of RTN is proportional to $1/LW$ where LW is a gate area [7]. Thus we must accurately predict the impact of RTN in the nanometer process design.

In this work, we propose a transient RTN simulation method on the circuit level. RTN is modeled by fluctuation of $V_{\rm th}$ caused by defects in the gate oxide [8]. The fluctuation is modeled by several parameters such as the time constant τ and the threshold voltage difference for each defect $\Delta V_{\rm th_d}$. There are previous works of RTN simulations [9], [10]. They deal only a single defect, although multiple defects exist in the gate oxide. We construct the model for multiple defects. Our model behaves like a voltage source because current fluctuation from carrier trap and emission are represented by the threshold voltage difference ($\Delta V_{\rm th}$). We perform the transient analysis of ring oscillators (ROs) by attaching the voltage source to the gate terminal. It is possible to estimate the impact of widely distributed RTN fluctuation to perform Monte Carlo simulations with our model.

This paper is organized as follows. We explain the physical model of RTN and a circuit simulation method in section II. Section III shows the simulation results of RTN on NMOSFETs and ROs. Section IV concludes this paper.

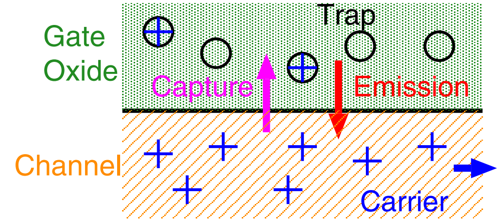


Fig. 1. Mechanism of RTN based on physics in gate oxide.

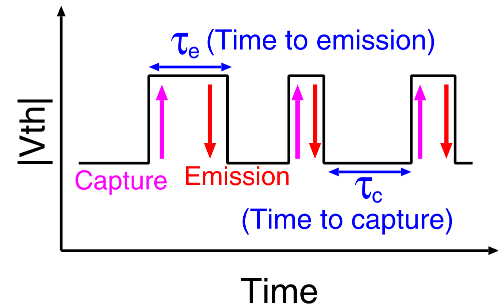


Fig. 2. RTN-induced $V_{\rm th}$ shift by a single defect.

II. Physics Based RTN Model and Application to Circuit Simulation

First, we explain the mechanism of RTN based on physics and modeling of RTN. Section II-B describes how to fluctuate $V_{\rm th}$ by using a variable DC voltage source. The behavior of the voltage source is described in Section II-C.

A. RTN Mechanism and Model based on physics

RTN is caused when a carrier is trapped, then current going through a MOSFET is decreased, which can be represented by the increase of $\Delta V_{\rm th}$ in a transistor model. It occurs when carriers in the channel are captured or emitted to defects in the gate oxide (Fig. 1). Fig. 2 shows a $V_{\rm th}$ fluctuation caused by RTN from a single defect. Time constants $\tau_{\rm c}$ and $\tau_{\rm e}$ are defined as the average time to capture or emit carriers respectively. They depend on gate voltage ($V_{\rm G}$). When $V_{\rm G}$ increases, $\tau_{\rm c}$ and $\tau_{\rm e}$ become short and long respectively [6]. As shown in Fig. 2, $V_{\rm th}$ has two states. When a defect captures or emits a carrier, $V_{\rm th}$ becomes the high or low state respectively. $\Delta V_{\rm th_d}$ is constant in each of defects [11]. If multiple defects exist in the gate oxide, $V_{\rm th}$ fluctuates among multiple-states. This phenomenon is reproduced by the defects called the charge

trapping model (CTM). In this work, we propose the RTN simulation method based on CTM.

CTM has parameters n, $\Delta V_{\mathrm{th_d}}$ and τ_{c} and τ_{e}, where n is the number of defects in the gate oxide. n is different for each transistor and follows the Poisson distribution [12].

The Probability Density Function (PDF) of the distribution $P(n)$ is expressed as in Eq. (1).

$$P(n) = \frac{N^n e^{-N}}{n!} \tag{1}$$

Where N is the expected value of n and explained as in Eq. (2).

$$N = D{\cdot}LW \tag{2}$$

Where D is the number of defects per gate area. We assume $D = 4.0{\times}10^{-3}\ \mathrm{nm}^{-2}$ [2], [12]. $\Delta V_{\mathrm{th_d}}$ follows an exponential distribution and τ follows a logarithm distribution [8], [13]. PDF of the distribution of $\Delta V_{\mathrm{th_d}}$ is described by Eq. (3).

$$P(\Delta V_{\mathrm{th_d}}, \eta) = \frac{1}{\eta} \exp\left(\frac{\Delta V_{\mathrm{th_d}}}{\eta}\right) \tag{3}$$

Where η is the expected value of $\Delta V_{\mathrm{th_d}}$ explained as in Eq. (4).

$$\eta = \frac{s}{LW} \tag{4}$$

Where s is a coefficient of η. We assume $s = 9\ \mathrm{V{\cdot}nm^2}$ [14]. τ follows the logarithm distribution from 10^{-9} to 10^{9}s [13]. It depends on the V_{GS} and changes exponentially as in Eq. (5) [9], [15].

$$\tau = \tau_0 \exp(B{\cdot}V_{\mathrm{GS}}) \tag{5}$$

Where τ_0 is the time constant at $V_{\mathrm{GS}} = 0$ and B is the sensitivity to V_{GS}. As mentioned above, τ_0 distributes from 10^{-9} to 10^{9} s for each defect. The sensitivity B is distributed from 1 to 10 [9], [15].

B. Charge Trapping Model to MOSFET

In the RTN circuit simulation, we must temporally fluctuate V_{th}. Moreover, as mentioned above, τ depends on V_{GS}. It is impossible to use a set of voltage waveforms prepared prior to transient simulations.

V_{th} is shifted by changing device parameters. Standard transistor models are usually used such as BSIM (Berkley Short channel IGFET Model). But in those models, we cannot change device parameters during simulation. As shown in Fig. 3, we replicate the RTN-induced threshold voltage fluctuation to connect the variable DC voltage source implemented by using Verilog-AMS attached to the gate terminal. We call the voltage source the RTN module. It changes V_{GS} by $V_{\mathrm{th}}(t)$

C. RTN Circuit Simulation Method Using CTM

In this section, we explain the detail of the RTN module. Fig. 4 shows the flowchart to compute RTN-induced ΔV_{th}. Parameters to calculate RTN are shown in Table I.

First, n, $\Delta V_{\mathrm{th_d}}$ and τ are initialized. Then, a carrier is emitted or captured according to the Markov process without hysteresis. Finally, ΔV_{th} is increased by $\Delta V_{\mathrm{th_d}}$ if the carrier is trapped. This process is repeated for all defects.

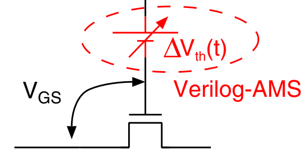


Fig. 3. V_{th} shift method in a circuit-level transient simulation. The variable DC voltage source is connected to the gate of MOSFET implemented by using Verilog-AMS to change V_{OV}.

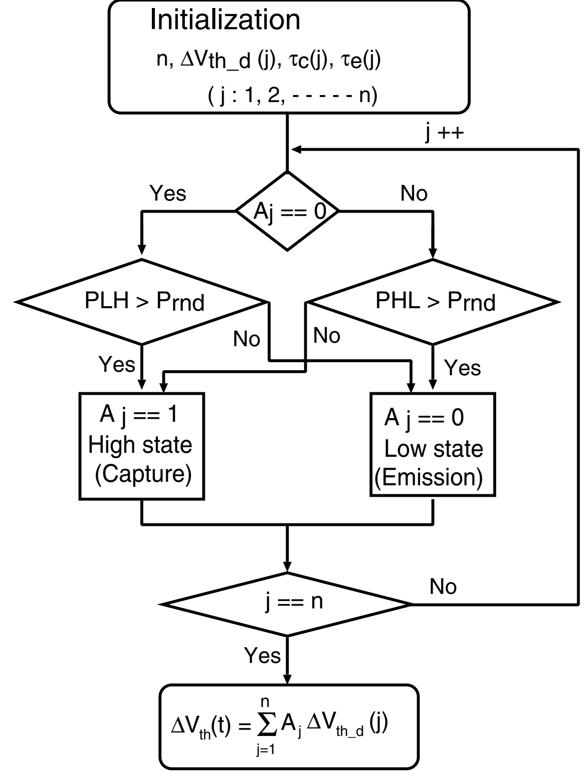


Fig. 4. Flowchart of RTN module.

TABLE I
PARAMETERS TO CALCULATE RTN.

Name	Explanation
L	Gate length
W	Gate width
n	The number of defects in the gate oxide
N	Expected value of n
D	Defects of gate oxide per area
$\Delta V_{\mathrm{th_d}}$	Threshold voltage fluctuation per defects
η	Expected value of $\Delta V_{\mathrm{th_trap}}$
s	Coefficient of η
τ_c	Time to capture of carrier
τ_e	Time to emission of carrier
T_{step}	Time step of transient analysis
P_{LH}	Probability to capture carrier
P_{HL}	Probability to emit carrier

In Fig. 4, A_j stands for the defect-capture state. “High state” and “Low state” mean that a carrier is captured and emitted respectively. If the state is “High”, $A_j = 1$ while the state is “Low” , when $A_j = 0$. P_{LH} is the transition probability to

TABLE II
SIMULATION CONDITIONS OF NMOSFET.

Explanation	Parameters	Value
Gate length	L	60 nm
Gate width	W	1 μm
Gate-Source voltage	V_{GS}	1.0 V
Drain-Source voltage	V_{DS}	1.0 V
Source voltage	V_{S}	0 V
Backgate voltage	V_{B}	0 V
Simulation time		1 μs

change the state from "Low" to "High". P_{HL} is the reverse transition of P_{LH}. P_{LH} and P_{HL} are expressed as in Eqs. (6) and (7).

$$P_{\mathrm{LH}} = 1 - \exp\left(\frac{T_{\mathrm{step}}}{\tau_{\mathrm{c}}}\right) \tag{6}$$

$$P_{\mathrm{HL}} = 1 - \exp\left(\frac{T_{\mathrm{step}}}{\tau_{\mathrm{e}}}\right) \tag{7}$$

Where T_{step} is the time step on transient analysis. The defect state is determined by comparing P_{LH} (P_{HL}) with P_{rnd}, which is a random digit of 0 or 1. When the states of all defects are fixed, ΔV_{th} is calculated by Eq. (8).

$$\Delta V_{\mathrm{th}} = \sum_{j=1}^{n} A_j \Delta V_{\mathrm{th_d}}(j) \tag{8}$$

Where $V_{\mathrm{th_d}}(j)$ is the threshold voltage fluctuate value of jth defect.

III. SIMULATION RESULTS OF RTN-INDUCED DRAIN CURRENT AND FREQUENCY FLUCTUATION

In this section, we analyze RTN-induced drain current fluctuations of NMOSFETs and frequency fluctuations in ROs. Model parameters of a 65 nm Fully-depleted Silicon on Insulator (FDSOI) are used.

A. Replicate Drain Current Fluctuation of NMOSFET

We perform transient analysis to replicate RTN-induced current fluctuation. The simulation conditions are shown in Table II.

Fig. 5 is simulation results of drain currensts in a single NMOSFET. The upper figure shows the drain current fluctuations and the lower one is the number of defects capturing carriers. Drain current fluctuates when the number of captured defects changes. Fig. 6 shows RTN-induced drain current fluctuations in three NMOSFETs. The amplitudes of RTN and timing of fluctuation are different. Therefore, we confirm that our proposed RTN model can successfully replicate drain temporal current fluctuation.

B. Frequency Fluctuation in RO

We simulate the frequency fluctuations of 300 ROs by the Monte Calro simulation. Fig. 7 shows the RO constructed by CMOS inverters. We choose the 3-stage RO because we obtain relatively huge RTN-induced fluctuation in the small stage and

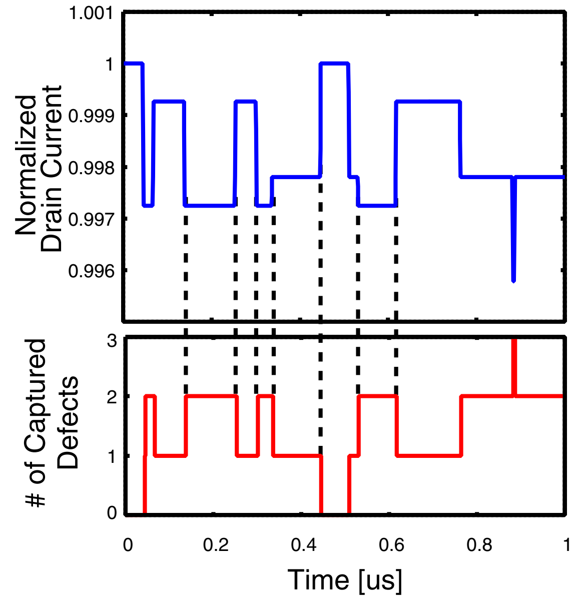


Fig. 5. Simulation results of drain currents (upper) and the number of captured defects (lower) in a single NMOSFET.

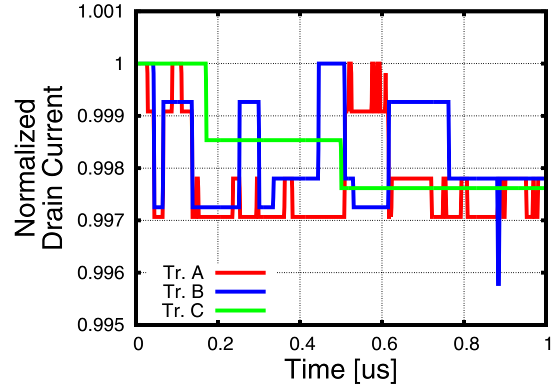


Fig. 6. Simulation results of RTN-induced drain current fluctuations in three NMOSFETs.

minimize simulation time [11]. The RTN-module is connected to gate terminals of all MOSFETs. The simulation conditions are shown in Table III.

Fig. 8 (a) shows the measurement results and Fig. 8 (b) shows the simulation result in two ROs among 300. The vertical axis of Fig. 8 is normalized by the maximum frequency. The fluctuation of Fig. 8 (b) is caused by RTN because the waveform in Fig. 8 (b) has the same tendency as the measurement results in Fig. 8 (a).

Fig. 9 shows the power spectral density (PSD) of the frequency fluctuations in Fig. 8 (b). PSD is the distribution of power in the frequency components including the signal. It is reported that the PSD is $1/f^2$-shaped by RTN [10]. We confirm that both PSDs from RO A and B follow $1/f^2$.

TABLE III
SIMULATION CONDITIONS OF RO.

Explanation	Parameters	Value
Gate length	L	60 nm
Gate width of NMOS	W_{n}	260 nm
Gate width of PMOS	W_{p}	450 nm
Power supply Voltage	V_{DD}	0.5 V
Simulation time		1 μs

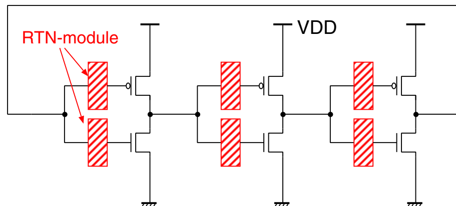
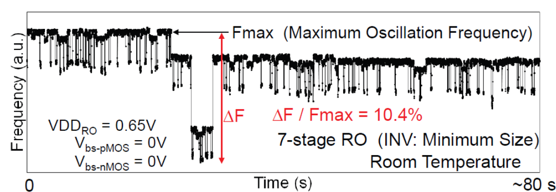
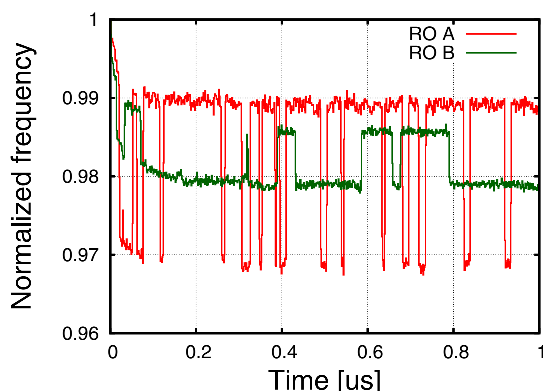


Fig. 7. 3-stage ring oscillator. The RTN-module is connected to gate teminals of all MOSFETs.



(a) Measurement results [11]



(b) Simulation results

Fig. 8. Results of RTN-induced frequency fluctuations.

IV. CONCLUSION

We propose the RTN simulation method to implement a variable DC voltage source which fluctuates temporally by using Verilog-AMS. We obtain the RTN-induced drain current fluctuation of NMOSFETs to simulate transient analysis. The impact of RTN and the timing flcutuations are different in each NMOSFET. In ROs, we obtain the RTN-induced frequency fluctuation. Our proposed method can be applied to estimate the temporal impact of RTN for analog and degital circuits including multiple transistors.

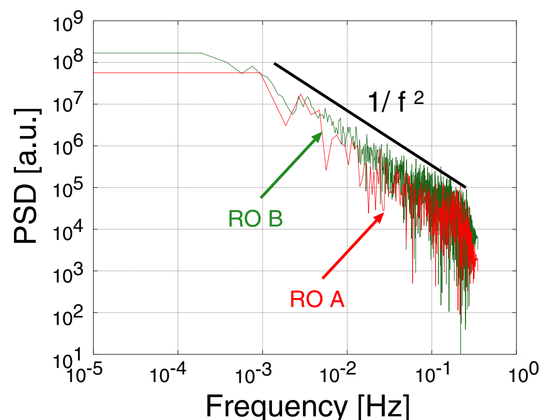


Fig. 9. Power power spectral density from Fig. 8 (b).

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