Student Paper

Impact of Random Telegraph Noise on Ring Oscillators Evaluated by Circuit-level Simulations

Azusa Oshima[1], Pieter Weckx[2], Ben Kaczer[2], Kazutoshi Kobayashi[1], Takashi Matsumoto[3]
Kyoto Institute of Technology[1], imec[2], VDEC[3]
Department of Electronics[1]
Kyoto, Japan[1], Leuven, Belgium[2], Tokyo, Japan[3]
aoshima@vlsi.es.kit.ac.jp[1]

***Abstract*—Random Telegraph Noise (RTN) has become dominant with transistor rapid scaling in recent years. We simulate RTN-induced frequency fluctuation of Ring Oscillators (ROs) using a circuit-level simulator to replicate measurement results from previous works. Consequently, we can predict dependences of frequency fluctuation on operating voltages, number of ROs stages, gate widths, and body biases.**

Keywords—Reliability, Variability, Random Telegraph Noise, Ring Oscillator

I. Introduction

The variability issues in MOSFET devices can be classified into static (as-fabricated or time-zero) and dynamic (time-dependent). The latter is due to degradation effects such as HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), BTI (Bias Temperature Instability) and RTN (Random Telegraph Noise). Both static and dynamic variations have random and systematic (process-induced) components [1]. A major source of random variation, both static and dynamic, is random dopant fluctuation (RDF) [2]. With the rapid downscaling of the MOSFET devices, dynamic variation is becoming serious. In this paper, we deal with dynamic variations caused by transistor gate oxide defects. When a voltage is applied to the transistor gate, threshold voltage and delay increase with time due to BTI [3], which is accelerated under increased temperature. Even at constant bias, threshold voltage increase randomly by RTN [4]. Recently, it has been argued that the same mechanism is responsible for RTN and the recoverable component of BTI (Fig. 1) [5, 6]. When gate oxide defects capture carrier between source and drain, the channel current decrease and the threshold voltage changes. The degradation recovers when oxide defects emit carriers. In BTI, traps continue to capture carriers while the stress is applied. Soon after the stress removed, traps emit carriers. During RTN, capture and emission occur alternately while the operating voltage is applied, with the time constants defined as τ_c and τ_e [4, 5].

Since the RTN magnitude is sensitive for device size [7], it is becoming a new threat not only to analog circuits but also to digital circuits, for instance, SRAMs [8], flash memories [9] and image sensors [10]. Some works show threshold voltage variation of RTN is due to RDF [7, 11].

In this paper, we focus on RTN. To predict the impact of RTN, we simulate RTN-induced frequency fluctuation of ROs and replicate measurement results in a previous work [4].

II. Measuement Results of RTN in Previous Work

Our first goal is to replicate the experimental results of RTN on ROs in [4]. Frequencies of 7 stage ROs are measured for 80 s. Fig. 2 shows frequency time dependence of one of 12,600 ROs. $F_{\max}$ and ΔF of each RO are defined as the maximum frequency and the maximum frequency fluctuation respectively. Fig. 3 shows the measured time-zero, $F_{\max}$ distribution [4]. The distribution of measured (normalized) frequency fluctuation ΔF is given by in Fig. 4. Both quantities are distributed due to static and dynamic (RTN) variations. In the following, we simulate these distributions, and discuss the impact of operating voltage, number of ROs stages, device gate widths and body bias.

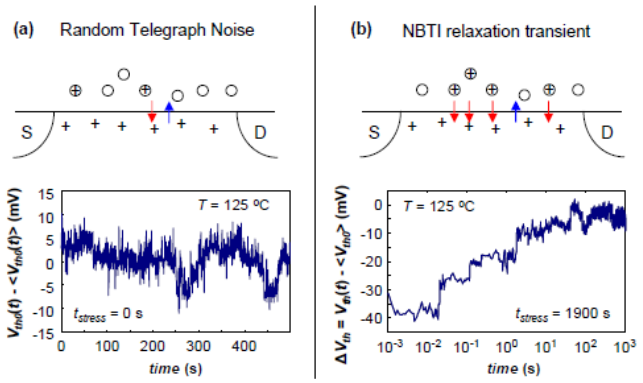

Fig. 1. Mechanism of RTN and BTI [5].

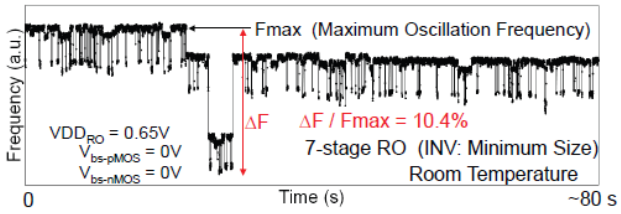

Fig. 2. Time dependency of frequency [4].

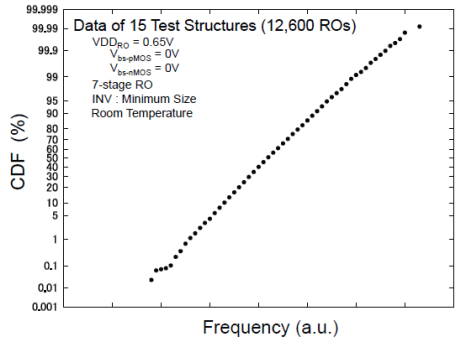

Fig. 3. Normal CDF plot of measured $F_{\max}$ caused by time-zero variations [4].

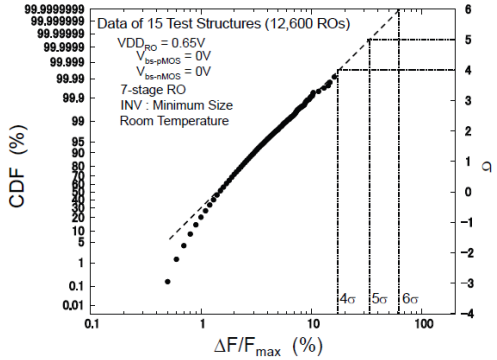

Fig. 4. Log-normal CDF plot of measured frequency fluctuation ($\Delta F/F_{\max}$) [4].

III. Simulation Method to Evaluate Impacts of RTN

To evaluate the impact of RTN on circuit performance, we simulate ROs in a circuit-level simulator with static and dynamic (RTN) variations. We will show how to calculate RTN-induced ΔV_{th}.

A. RTN-induced single trap ΔV_{th} distribution

RTN-induced ΔV_{th} distribution has two parameters : the number of captured traps N in the MOSFET gate oxides and the mean ΔV_{th} per single trap η. In this section, we first assume the captured trap on a device is equal to one ($N = 1$) and discuss the distribution of η. Several works show that ΔV_{th} per trap follows an exponential distribution [5, 12]. The Probability Density Function (PDF) of ΔV_{th} is described as

$$f_\eta(\Delta V_{\text{th}}, \eta) = \frac{1}{\eta} e^{\frac{\Delta V_{\text{th}}}{\eta}} \qquad (1)$$

The Cumulative Distribution Function (CDF) of ΔV_{th} is then

$$F_\eta(\Delta V_{\text{th}}, \eta) = 1 - e^{\frac{\Delta V_{\text{th}}}{\eta}} \qquad (2)$$

η scales inversely with the device channel area [13].

$$\eta \propto \frac{1}{W\sqrt{L}} \qquad (3)$$

where L and W are the device gate length and width, respectively.

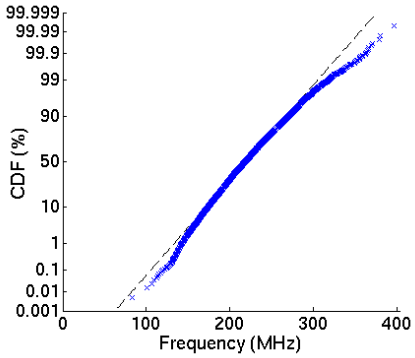

Fig. 5. Normal CDF plot of simulated time-zero frequency.

B. RTN-induced N traps ΔV_{th} distribution on a device

We now assume the number of captured traps on a device is the constant N. The ΔV_{th} distribution can be expressed as a convolution of N individual-trap exponential distributions (see the previous section) [5], and the PDF g_η and CDF G_η of ΔV_{th} are respectively

$$g_\eta(\Delta V_{\text{th}}, \eta) = \frac{e^{\frac{\Delta V_{th}}{\eta}}}{(n-1)!} \frac{\Delta V_{\text{th}}{}^{n-1}}{\eta^n} \qquad (4)$$

$$G_\eta(\Delta V_{\text{th}}, \eta) = 1 - \frac{\Gamma\left(n, \frac{\Delta V_{\text{th}}}{\eta^n}\right)}{(n-1)!} \qquad (5)$$

C. RTN-induced total ΔV_{th} distribution on a chip

An actual device will contain a Poisson-distributed number of defects n, with mean value N [5, 6, 14]

$$P_N(n) = \frac{e^{-N} N^n}{n!} \qquad (6)$$

The average number of captured traps N is related to the oxide trap density N_{ot} as $N = WLN_{ot}$. The total ΔV_{th} CDF is given by the convolution of Eqs. 5 and 6.

$$H_{\eta,N}(\Delta V_{\text{th}}, \eta) = \sum_{n=0}^{\infty} P_N(n)\, G_\eta(\Delta V_{\text{th}}, \eta) \qquad (7)$$

D. Simplified model of RTN-induced ΔV_{th} distribution

In the actual simulation, a Monte Carlo method is used combining Eqs. 2 and 6. Each $\Delta V_{\text{th,k}}$ sample is consisting of the sum of a Poisson distributed number of single defect $\Delta V_{\text{th},i}$, which are exponentially distributed.

$$\Delta V_{\text{th},k} = \sum_{i=1}^{N_k} \Delta V_{\text{th},i} \qquad (8)$$

Using Eq. 8 a ΔV_{th} table is created for $k = 1 \ldots m$, where m is the number of Monte Carlo runs, N_k is Poisson-distributed around the mean value N (Eq. 6) and $\Delta V_{\text{th},i}$ follows an exponential distribution with mean η (Eq. 2). The final ΔV_{th} distribution is then entirely characterized by the mean number of occupied traps N and the mean impact per trap η, described by Eq. 7.

E. Time-zero ΔV_{th} distribution

Since time-zero variations have also a serious impact on circuits, they have to be considered together with RTN. Assuming time-zero variation induced-ΔV_{th} in both of NMOS and PMOS is normally distributed [16], we can generate the time-zero distribution of frequencies in the simulated ROs. The simulated distribution in Fig. 5 has the same shape as the measured distribution in Fig. 3.

F. Comparision with Measurement Results

Measurement results of F_{max} (Fig. 3) and $\Delta F/F_{\mathrm{max}}$ (Fig. 4) are calculated from the frequency time dependence shown in Fig. 2 [3]. In our simulations we generate the impact of time-zero variation and RTN on frequency of 10,000 ROs at a fixed moment in time. ROs are simulated using 45 nm BSIM Predictive Technology Model (PTM). Each RO instance is simulated with (i) time-zero variation only and with (ii) the same time-zero variation and RTN, resulting in F_0 and $F_{\mathrm{RTN+0}}$, respectively. Specifically,

(i). PMOS and NMOS in all RO stages have time-zero-induced normal-distributed ΔV_{th} and this distribution has the mean μ=52 mV and the standard deviation σ =31 mV.

(ii). PMOS and NMOS in all RO stage have same process variation as (i) and RTN-induced ΔV_{th}. RTN-induced parameters η and N, as well as the devices dimensions.

Finally, we calculate the main metrics of [3] as

$$\frac{\Delta F}{F_{\mathrm{max}}} = \frac{F_0 - F_{\mathrm{RTN+0}}}{F_0} \qquad (9)$$

IV. Simulation Results of RTN on Logic Circuit

We now discuss the results of our simulations.

A. RTN-induced Frequency Fluctuation

Fig. 6 shows the distribution of $\Delta F/F_{\mathrm{max}}$ calculated for 10,000 ROs at V_{dd} =0.65 V. Both of simulation and measurement results is in the log-normal distribution. Note the simulation predicts a concave-up tail of distribution at *low percentiles*. This is because in the simulation, there is always a (small) probability that no defect is present in the RO with strong impact on ΔV_{th} and the frequency. The measurement results in Fig. 4, however, show *low-percentile* tail to converge to a constant minimum value. We speculate that this minimum value of $\Delta F/F_{\mathrm{max}}$ is due to a finite resolution of the frequency measurement. The *high-percentile* tail of the $\Delta F/F_{\mathrm{max}}$ is, however, crucial for the reliability predictions of real CMOS applications.

B. Discussion of parameter dependences

Figs. 7-10 show the dependences of frequency fluctuation on operating voltages, number of ROs stages, gate widths and body biases calculated for 840 ROs. As V_{dd} increases, the mean of $\Delta F/F_{\mathrm{max}}$ decreases in Fig. 7. This tendency, due to increase of F_{max} with V_{dd} is the same as in the experimental results [3]. Fig. 8 then shows the impact of RTN decreases with the number of stages, also corresponding to measurement results [4]. Specifically, the mean of $\Delta F/F_{\mathrm{max}}$ is fixed but their distribution widths become small. Fig. 9 also shows the distribution widths of $\Delta F/F_{\mathrm{max}}$ become smaller when gate widths increase corresponding to measurement results. This is because the number of captured traps N increases and ΔV_{th} per trap η decreases with increased device channel area following to Eq. 3.

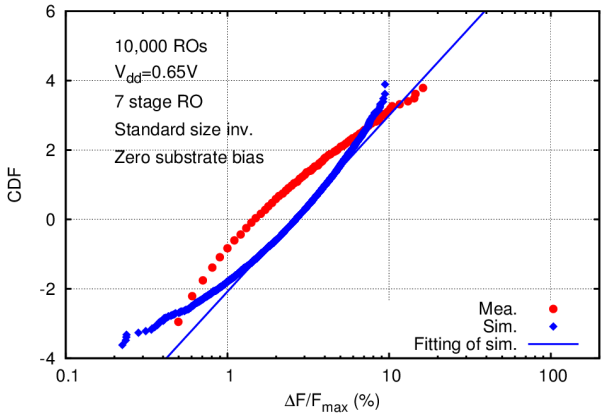

Fig. 6. Log-normal CDF plot of simulated RTN-induced frequency fluctuation ($\Delta F/F_{\mathrm{max}}$).

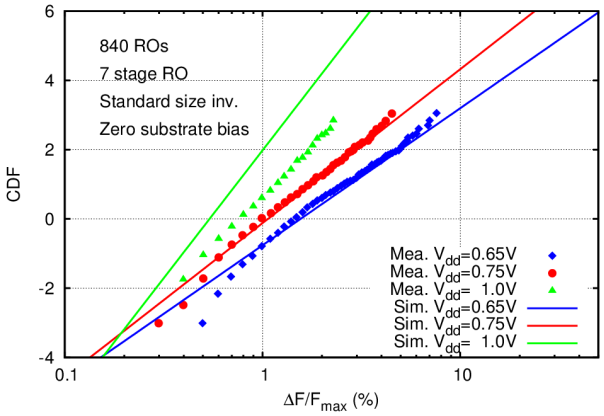

Fig. 7. Simulated V_{dd} dependence of RTN-induced frequency fluctuation.

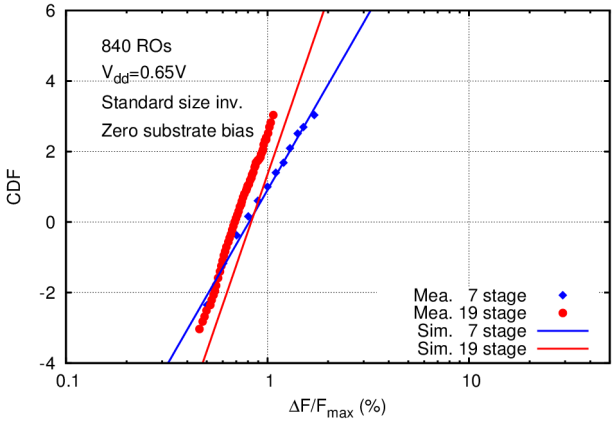

Fig. 8. Simulated the number of RO stages dependence of RTN-induced frequency fluctuation.

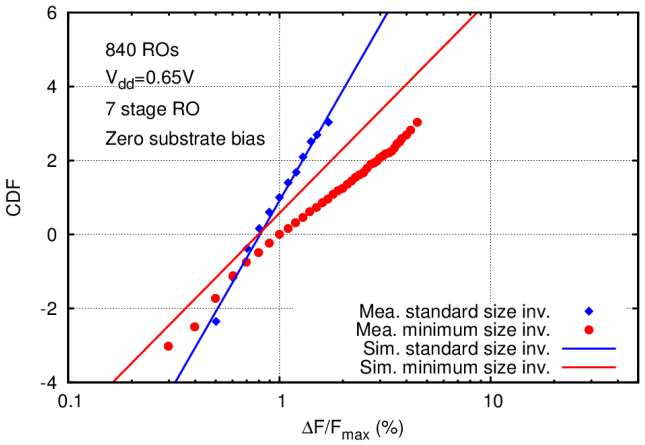

Fig. 9. Simulated gate width dependence of RTN-induced frequency fluctuation.

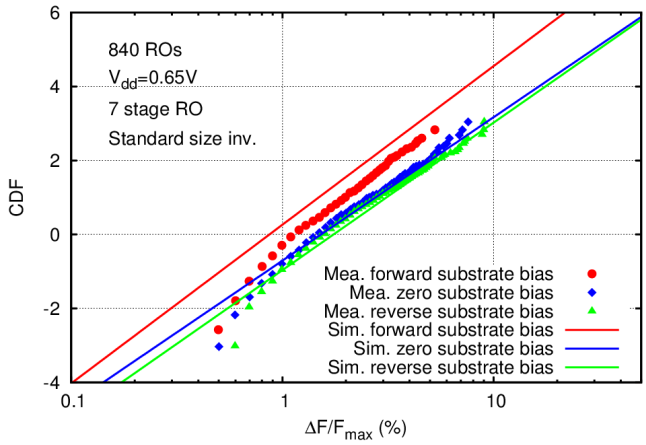

Fig. 10. Simulated body bias dependence of RTN-induced frequency fluctuation.

The ratios of PMOS and NMOS gate areas (W×L) of the minimum size inverters to the standard size inverters are 0.21 and 0.30 respectively. Fig. 10 shows forward and reverse bias dependence of $\Delta F/F_{\max}$. Forward bias means the body bias for PMOS $V_{\mathrm{bs\_pmos}} = +0.2\,\mathrm{V}$, the body bias for NMOS $V_{\mathrm{bs\_nmos}} = +0.2\,\mathrm{V}$. Reverse bias means $V_{\mathrm{bs\_pmos}} = -0.2\,\mathrm{V}$, $V_{\mathrm{bs\_nmos}} = 0\,\mathrm{V}$. When forward bias is applied to PMOS and NMOS, it has been previously observed that η decreases and impact of RTN decreases [17]. On the other hand, reverse bias increases the mean of $\Delta F/F_{\max}$ since η increases with reverse bias [16]. The body bias dependency of RTN is corresponding to the measurement results.

V. Conclusion

We have simulated the distributions of RTN-induced frequency fluctuations of ROs to replicate trends in on-chip previous measurements. We assume RTN-induced ΔV_{th} to be described as a convolution of η (ΔV_{th} of per trap) and N (number of captured traps). Simulation results have the same dependence of frequency fluctuation $\Delta F/F_{\max}$ on the operating voltage, the number of RO stages, gate widths and body bias as measurement results. Because of the gate width and body bias dependence of η, the impact of RTN becomes smaller with increased gate widths and forward biasing. Impact of RTN can be reduced by increasing the operating voltage or increasing the number of RO stages.

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