「依頼講演」 C-elementのソフトエラー耐性を強化した65nm Bistable Cross-coupled Dual Modular Redundancy (BCDMR) FF.

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あらまし 本稿では, ソフトエラー耐性を大幅に高めたBistable Cross-coupled Dual Modular Redundancy (BCDMR) Flip-Flopを提案する．これは, インテル/スタンフォード大により提案されたBISER FFを改良したもので, クロスカップル構造をとるために, 面積, 遅延, 電力のオーバーヘッドなしに, ソフトエラー耐性を大幅に高めることができる．60,480bitのBCDMR-FFを集積したLSIを65nmプロセスにて試作した．α線源によるの試験では, 160MHzのクロック周波数を与えた場合に, エラー耐性はBISERに比べて150倍となった.
キーワード ソフトエラー、信頼性、多重化、フリップフロップ

[依頼講演] A 65nm Bistable Cross-coupled Dual Modular Redundancy Flip-Flop Capable of Protecting Soft Errors on the C-element

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Abstract We propose a Bistable Cross-coupled Dual Modular Redundancy (BCDMR) Flip-Flop to enhance soft--error immunity. It is based on a BISER FF but its cross-coupled structure enhances soft-error immunity without any area/delay/power overhead. We fabricated a 65nm LSI including 60,480bit shift registers with the BCDMR and BISER structures. Experimental results using alpha-particles reveals that the soft-error immunity of the BCDMR is enhanced by 150x at 160MHz clock frequency compared with the BISER FFs.
Key words Soft Error, Reliebility, Multiple Modular Redundancy, Flip-Flop

1. Introduction

To protect FFs from soft errors caused by α particles or neutrons, several redundant flip-flop structures are proposed such as TMR, DICE [1] or BISER [2]. The DICE has four redundant storage nodes to prevent an SEU (Single Event Upset). The TMR (Triple Modular Redundancy) is the supreme solution to prepare three FFs for voting by paying the huge area penalty, while the BISER (hereafter we call it DMR, Dual Modular Redundancy) structure has two FFs with a small weak keeper for voting to reduce large area-overhead of the TMR. The DMR structure can protect SEUs caused by particle hits on storage nodes. However, they are very weak to a SET (Single Event Transient) pulse caused by a particle hit on the C-elements. We propose a modified DMR flip-flop called “Bistable Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR-FF).” It contains cross-coupled C-elements and weak keepers to prevent an unnecessary flip caused by a particle hit on the C-element. We have fabricated a 65nm LSI including 60,480bit shift registers with the BCDMR and DMR structures.

2. Bistable Cross-coupled Dual Modular Redundancy FF

Fig. 2 shows the conventional DMR(BISER) FF. It duplicates master and slave latches with the C-element and a weak keeper. The delay element τ is used to remove the simultaneous flip caused by an SET (Single Event Transient) pulse from combinational circuits connected to FFs. If one of a master, slave latch or weak keeper is flipped by a particle hit, the other two prevent the output of the FF to be flipped as shown in the slave latch section of Fig. 2. The DMR FF outputs the wrong value if two storages flip simultaneously within a clock cycle, the possibility of which becoming

weaker by increasing the clock frequency. However, there is a possibility of a particle hit on the C-element, at which an SET pulse may flip both of two redundant latches as shown near the left weak keeper in Fig. 2. The possibility of capturing an incorrect value is becoming stronger by increasing the clock frequency as in Fig. 1. As the result, the conventional DMR structure is becoming vulnerable to soft errors caused by SET pulses on the C-element at the high clock frequency.

To mitigate vulnerability of the C-element, we propose the Bistable Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR-FF) as shown in Fig. 3, in which C-elements are duplicated to prevent multiple latches to be flipped by an SET pulse from the C-element. Table I compares area, delay and power of the DMR and proposed BCDMR FFs without τ normalized by those of the conventional FF in a 65nm CMOS. BCDMR achieves same area and better power and delay at 0.5V compared with the DMR. It is mainly because its cross-coupled structure reduces the size of the C-element that must have enough strength to flip the weak keeper.

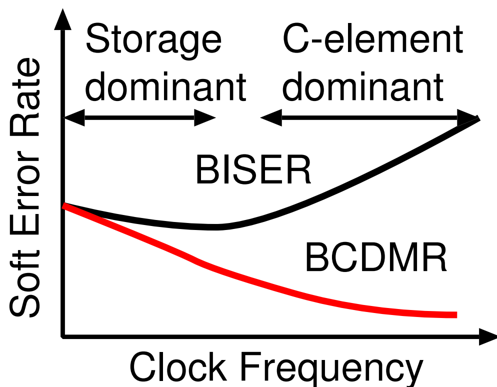

図 1 Soft Error Rate by Clock Freq.

Table I: Area/Power/Delay normalized to Conv. FF.

	DMR	BCDMR
Area	3.00	3.00
D@1.2V	1.47	1.45
P@1.2V	2.15	2.20
D@0.5V	1.96	1.57
P@0.5V	2.39	2.23

3. Test Chip Design

In order to examine the error resiliency of FFs, Large number of FFs constructing a shift register are exposed to neutron beams or alpha particles without clock. It can only capture SEUs induced by the particle hits on storage nodes. If an SEU induced by an SET pulse is going to be captured, clock signal must be applied to FFs. However unwanted shift operations arise by the clock, which wipes out all flipped values along the shift register. Fig. 4 depicts the shift register with a local-loop structure to keep SEUs induced by SET pulses. The local loop contains 8 FFs constructing a 8bit shift register. Fig. 6 shows a chip micrograph with floorplan. Two 30,240bit shift registers with the DMR and BCDMR FFs are implemented with a PLL at the left side. As described in the previous section, transistor sizes of the BCDMR can be reduced. However those of both shift registers are equivalent to equalize the experimental conditions. The shift-in (SI) signal is given from the bottom of the shift register, while the clock signal is given from the top of the shift register. Such structure simplifies the clock circuitry. The clock signal is connected in series from the tail to the head of the shift register. Clock frequency must be slower on the shift operation. However, higher clock can be applied during irradiation experiments since all local-loops can be operated asynchronously. We implement SET pulse capture circuits including four different inverter chains with 5,000 stages to investigate the dependency of SET pulses on transistor size, drain area as in Fig. 5. If an SET pulse from the inverter chain reaches the SR latch, Hold signal is becoming high to capture the pulse inside of the D latch array [3]. We have fabricated the shift registers with the DMR and BCDMR FFs, SET pulse capture circuits and 168,000bit shift registers with ordinal FFs on a 2.1mm×4.2mm die as in Fig. 6 in a 65nm bulk CMOS.

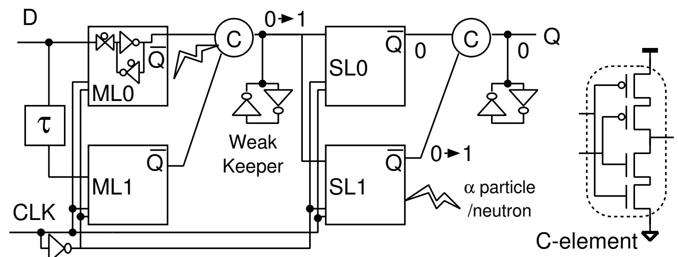

図 2 Conventional DMR (BISER) FF with the C-element.

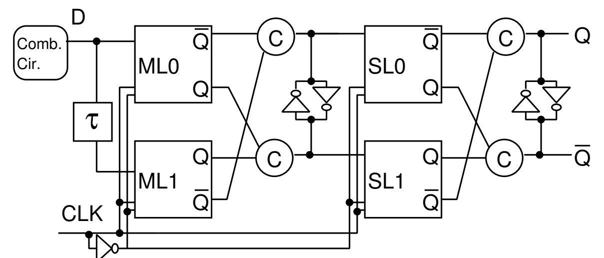

図 3 Proposed Bistable Cross-coupled DMR (BCDMR) FF.

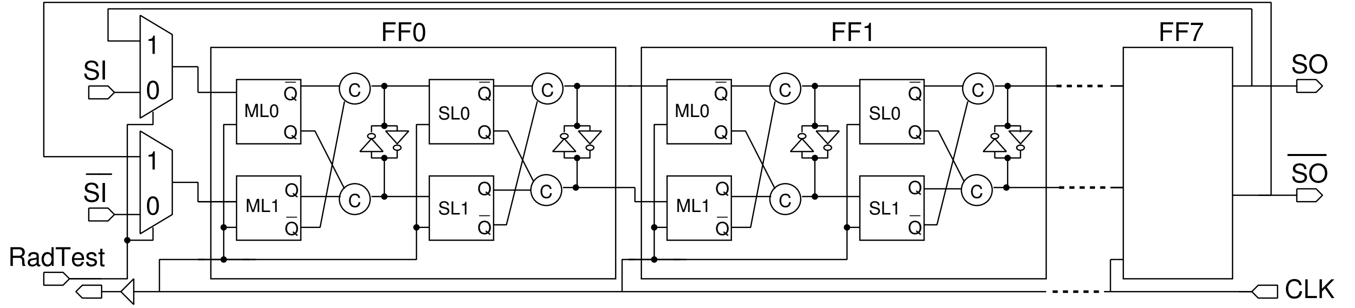

図 4 Shift register with a local-loop structure to keep SEUs inside the loop induced by SET pulses.

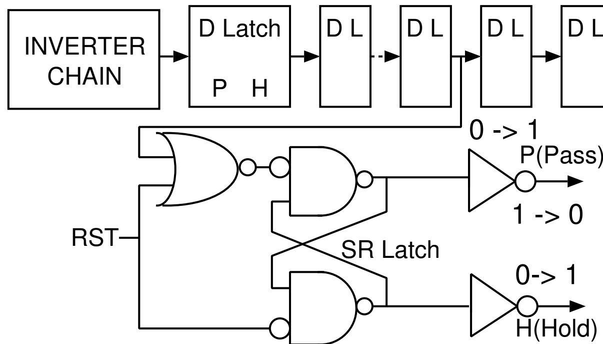

図 5 SET pulse capture circuit [3].

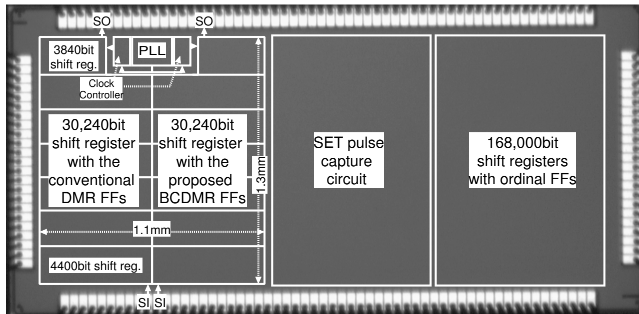

図 6 Chip photo and floorplan.

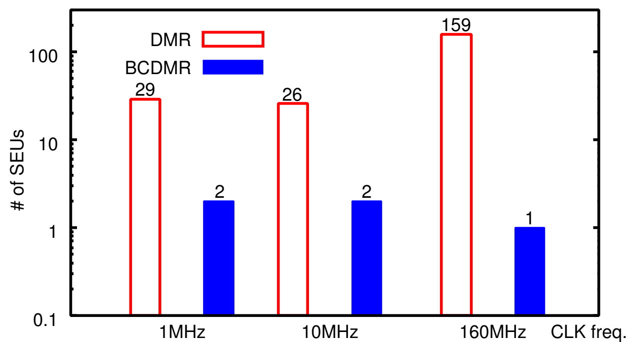

図 7 Number of SEUs according to clock frequency by 500 min. α particle irradiation.

4. Results and Discussions

We have done two experiments as follows. One is the accelerated white neutron-beam irradiation at RCNP of Osaka University for the inverter chains and the shift registers with the ordinal FFs, whose average accelerated factor is 1.84×10^8. The other is alpha particles irradiation by ^{241}Am for the shift registers at the left side. Table II shows the rate of SET pulses and average SET pulse widths for the four inverter chains. It reveals that the number of SET pulses does not depend on the transistor size but on the drain area. The number of SET pulses is smallest on the 0.5x inverter chain of the smallest drain area. The proposed BCDMR FF have duplicated C-elements with smaller transistor sizes since its cross-coupled structure can reduce transistor size to flip the weak keeper. which can also reduce the number of SETs.

Table II: SET statistics of the inverter chains by neutron irradiation

Transistor size ratio	2x	1x	0.5x	
Drain area ratio	1.25	1.00	0.51	1.04
# of SET pulse[n/hour]	11	4.9	7.9	17
Avg. SET pulse width[ps]	250	250	N/A	300

The number of SEUs of the ordinal FFs on the neutron-beam irradiation without giving clock is 342/Mbit/hour. If a 2x inverter chain with 11 stages is attached to the ordinal FF, SET pulses are generated 27 times more frequently than that of SEUs. Experimental results in Table II show that the average pulse width on 2x is 250ps. If 1GHz(1ns) clock is applied to the FF, 25% of these SET pulses are captured as SEUs. Thus SEUs induced by SET pulses are more frequent than those induced by particle hits on storage nodes on the ordinal non-redundant FF.

Fig. 7 shows the error rates according to the clock frequency of 1, 10 and 160MHz by α particle irradiation of the shift registers with the DMR and BCDMR FFs. They are almost equivalent to Fig. 1. SEUs induced by a particle hit on storages are dominant at the lower clock, while SEUs induced by a particle hit on the C-element are dominant at the higher clock. The C-element on the DMR structure is vulnerable to soft errors at the higher clock. The proposed BCDMR FF exhibits 150x better error resiliency at 160MHz

clock frequency than the DMR FF with almost same or better area, delay and power. Due to the limitation of the PLL and clock network, our experiments are limited to 160MHz. But the error resiliency of the BCDMR is much better than the DMR according to the increase of the clock frequency. The BCDMR has $1.2e^{-24}$x better resiliency than the DMR at 1GHz from circuit-level simulations on the neutron irradiation, at which SET pulses are more frequently generated than the α particle irradiation.

5. Conclusion

We propose a dual modular redundancy flip-flop called "Bistable Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR-FF)." Experimental results on a 65nm LSI by α particle irradiation shows that the BCDMR-FF has 150x better soft-error resiliency than the conventional BISER FF at 160MHz clock frequency since the vulnerability of the C-element is dominant at higher clock frequency. The proposed BCDMR-FF with the cross-coupled C-elements prevents two redundant flip-flop to be simultaneously flipped by a particle hit on the C-element. It also exhibits almost equivalent or better area, delay and power because of its cross-coupled structure.

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