Evaluation of FPGA Design Guardband Caused by Inhomogeneous NBTI Degradation Considering Process Variations

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***Abstract*—**
We show NBTI delay degradation considering variations in a 65nm process. We evaluate these two models. The homogeneous degradation model (HDM) assumes that NBTI degradation is constant at any variation and the inhomogeneous degradation model (IDM) assume that it is larger at the fast condition. In the usual logic gates on ASICs, delay degradation becomes much smaller on IDM. Circuit design guardbands can be reduced to 1/3 from the conventional pessimistic evaluations. As for FPGAs, we evaluate routing paths including level restorers and tristate inverters. The delay time after NBTI degradation is almost constant because of the pull-up PMOS in the level restorer.

I. Introduction

Recent years, performance of FPGAs is becoming comparable to that of Application Specific Integrated Circuits(ASICs). FPGAs has many good features such as short development period, inexpensive development cost and easy designing. Vendors can fabricate FPGAs with the latest process. But some problems, for example variations, are exposed at scaling process.

Negative Bias Temperature Instability(NBTI) was first reported in 1967 [1]. NBTI is a well-known LSI degradation as well as Hot Carrier Injection(HCI) and Time Dependant Dielectric Breakdown(TDDB). Threshold voltage($V_{\rm th}$) of PMOS increases with time caused by negative bias voltage, which is called stress condition. NBTI is known as one of the dominant factors that determine the life time of circuits after 65nm process [2]. NBTI degradation depends on temperature, supply voltage, frequency and device parameters. $V_{\rm th}$ degradation is recovered when negative bias is removed, which is called relax condition. NBTI degradation includes both recoverable and permanent parts. According to the latest work, they have various origins. Because of recovery of degradation, it is difficult to measure NBTI for modeling. Several measurement methods are proposed in [3]–[5]. Some NBTI models are suggested in [6], [7]. An accurate NBTI model is still discussed, because it critically depends on the stress condition and process node.

Variations are becoming another issue after 90nm process. It is the phenomenon that fluctuate $V_{\rm th}$ caused by fluctuation of doped impurities and line edge roughness. Device $V_{\rm th}$ follows Gaussian distribution. Hereafter we define the mean(μ), $\mu+3\sigma$ and $\mu-3\sigma$ as typical (TT), slow (SS) and fast (FF) conditions. We assume that the NBTI degradation differs according to process variations. It is important to investigate how NBTI affects circuit performance considering variations effect. We investigate that for FPGAs. We evaluate frequency degradation of aged ROs mapped on FPGAs and delay time degradation of aged circuit elements on FPGAs.

This paper is organized as follows. Related works are introduced in section II. Experimental methodology and NBTI model are explained in section III. We show the result from simulation experiments in section IV. We discuss results in section V. And the conclusion is in section VI.

II. Related Works

[8] discusses NBTI degradation effect on several circuit elements of FPGAs. They propose Relaxing Bitstream Technique to gain back lost stability and performance. A survey paper about reliability in FPGAs [9], explains various faults and detection/repair methods. The latest paper of NBTI on FPGAs [10], also considers HCI and evaluate both DC and AC NBTI effects. NBTI and variations are related to each other [11]–[13]. But they do not evaluate circuit performance degradation, only $V_{\rm th}$ degradation models are proposed.

III. NBTI Considering Variations

In this section, we explain our experimental methodology. There are many models which show how NBTI or variations affect PMOS $V_{\rm th}$. We apply $V_{\rm th}$ degradation($\Delta V_{\rm th}$) calculated by those models to circuit netlists. NBTI degradation models considering recovery effect were proposed by [14], [15]. We use the approximation formulae, Eq. (1, 2) [16], [17].

$$\Delta V_{\rm th,stress} = A \times t^n \quad (1)$$
$$\Delta V_{\rm th,relax} = \Delta V_{\rm th0}(1 - B \times \log{(t - t_0)}) \quad (2)$$

Eq. (1, 2) are degradation amount of $V_{\rm th}$ at stress and relax conditions respectively. Parameters A and B are determined as follows. We assume that $V_{\rm th}$ will degrade by 10% after 10 years continuous stress. In that case, it will degrade by 8.9% after 5 years continuous stress. We also assume it will recover by 3% after 5 years continuous relaxation. NBTI under continuous stress is called static NBTI. NBTI alternating between stress and relax is called dynamic NBTI. Dynamic NBTI degradation is fluctuated by frequency and duty cycle. We ignore frequency dependency since degradation is almost constant above 10kHz clock frequency [16]. We assume that duty cycle is 0.5. n is a time exponent that is considered as $1/6$. t_0 is total stress time. Static and dynamic NBTI degradation models are shown in Fig. 1. It is based on parameters of a 65nm process typical PMOS device.

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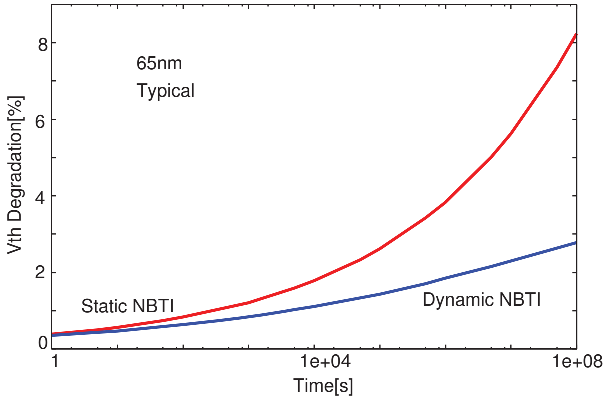

Fig. 1. Static and Dynamic NBTI Degradation Models

TABLE I
HOMOGENEOUS AND INHOMOGENEOUS DEGRADATION MODELS OF NBTI. STATIC AND DYNAMIC NBTI DEGRADATION FOR A DECADE.

Degradation	Type	INIT	Static [%]	Dynamic [%]
Homogeneous (HDM)	S	1.08	10	3
	T	1.00	10	3
	F	0.92	10	3
Inhomogeneous (IDM)	S	1.08	3	1
	T	1.00	10	3
	F	0.92	30	9

We use three parameter sets of variations, typical(TT), slow(SS) and fast(FF). We propose two models considering both NBTI and variations. The first model assume that each condition of variations causes constant degradation amount calculated using Eq. (1, 2). We call it Homogeneous Degradation Model(HDM). The upper part of Table I shows the parameters on HDM. Under the NBTI effect, fast PMOS devices degrade much faster than slow PMOS devices [7]. The second model is proposed under the situation, which is called Inhomogeneous Degradation Model(IDM). In this paper, we assume different degradations for each variations as in the lower part of Table I. V_{th} calculated by those models are shown on Fig. 2. V_{th} can be changed lineally with the device parameter, V_{TH0} in standard MOS models such as BSIM [18]. Positive Bias Temperature Instability(PBTI) occurs in NMOS device. V_{th} of NMOS increases with time caused by positive bias voltage. PBTI is ignorable at 65nm process because its effect appears much later than NBTI. Therefore we ignore PBTI effects in this paper.

IV. NBTI EFFECT ON ASICS AND FPGAS

We estimate NBTI effects of several logic gates on ASICs and FPGAs by oscillation frequency of ring oscillators (ROs) and routing paths on FPGAs.

A. 4 Types of Ring Oscillators

We predict degradation of 4 types of ROs, inverter (INV), NAND, NOR and Tri-State Inverter (TSI) gates. We evaluate frequency degradation of 5-stage ROs (RO5s) for 10^8sec. ($\simeq$ 3 years) and 10 years.

We evaluate frequency degradation affected by dynamic NBTI on three types of variations, TT, SS and FF. We use the two models explained in section III. We assume that all

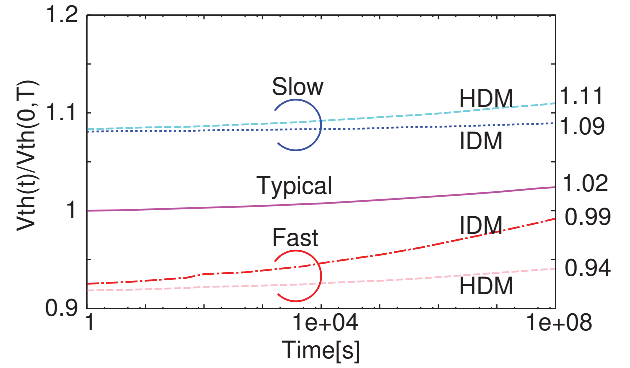

Fig. 2. Comparing Two Models of V_{th} Degradation

TABLE II
FREQUENCY DEGRADATION OF 4 TYPES OF RO5S. FREQUENCY AT $t = 1$sec. , $t = 10^8$sec. AND 10years ARE INCLUDED.

Gate	V.	Initial frequency[GHz] HDM	Initial frequency[GHz] IDM	Degradation ($t = 10^8$s)[%] HDM	Degradation ($t = 10^8$s)[%] IDM	Degradation ($t = 10$y)[%] HDM	Degradation ($t = 10$y)[%] IDM
INV	F	6.18	6.15	1.58	4.92	1.76	5.36
	T	4.56		1.92		2.19	
	S	3.68	3.69	2.16	0.733	2.34	0.769
NAND	F	4.62	4.60	1.32	4.10	1.46	4.48
	T	3.43		1.49		1.65	
	S	2.78	2.78	1.61	0.526	1.78	0.609
NOR	F	3.99	3.97	2.19	6.63	2.42	7.21
	T	2.83		2.59		2.86	
	S	2.25	2.26	2.83	0.941	3.08	1.05
TSI	F	3.57	3.55	1.86	5.63	2.03	6.16
	T	2.60		2.21		2.43	
	S	2.01	2.01	2.39	0.797	2.60	0.878

of PMOS devices uniformly degrade. The result is shown in Table II. The oscillation frequency of RO5s at the initial point ($t = 1$sec.) on the typical variations are 4.56GHz, 3.43GHz, 2.83GHz and 2.60GHz respectively. Degradations on HDM and IDM have different tendencies. In HDM, degradations on the SS condition are worse than those on the FF condition, while in IDM degradations on the SS condition are much smaller than those on the FF condition.

B. Level Restorer Circuits

We focus on the circuits including PMOS devices for pull-up called level restorers on FPGAs. We evaluate rise and fall delay time (T_{dr}, T_{df}) degradations of level restorers. The simulation circuit is shown in Fig. 3. It consists of two inverters(INV1 and INV2) connected through an NMOS path transistor(MNP) and a pull-up PMOS(MLR). MLR pulls up the output of INV1 to VDD and also prevents INV2 from floating. We assume input voltage rise/fall time is 1ns. The transistor size of MLR is defined to satisfy $T_{\mathrm{df}} = T_{\mathrm{dr}}$ at the TT condition.

We evaluate delay degradation affected by dynamic NBTI on three types of variations, TT, SS and FF. We use these two models, IDM and HDM explained in section III. We assume that all PMOS devices uniformly degrade. The results are shown in Fig. 4-5.

At $t = 1$sec. typical T_{df} is 0.161ns, slow T_{df} is 0.284ns and fast T_{df} is 0.833ns with IDM. T_{df} of the FF condition on IDM

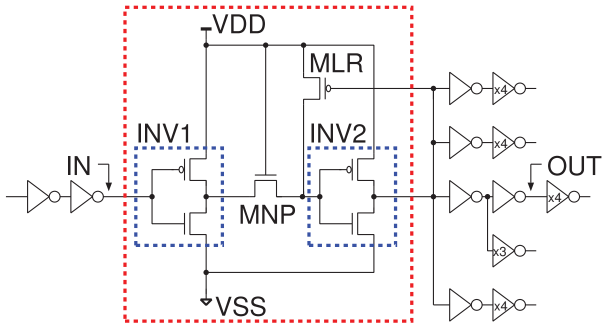

Fig. 3. Level Restorer Circuit on FPGAs

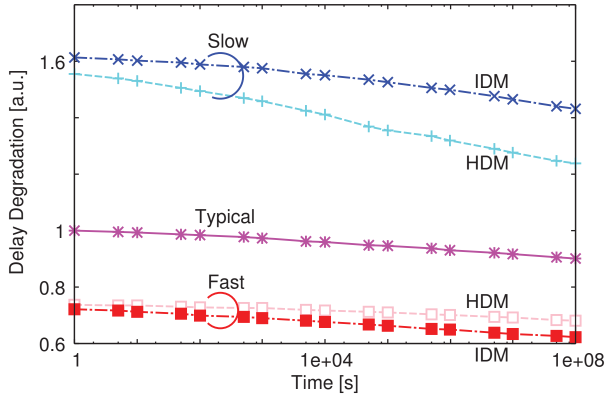

Fig. 4. T_{dr} Degradation on Dynamic NBTI of Level Restorer Circuit

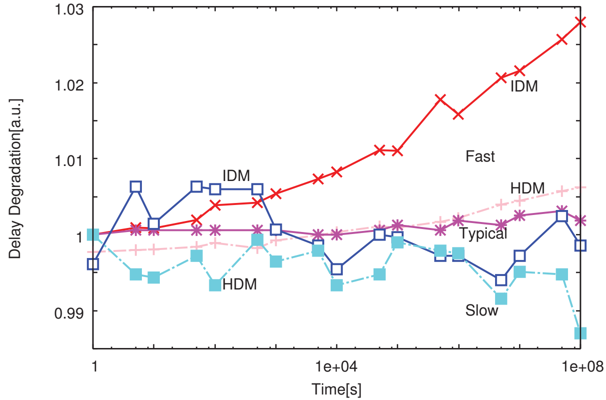

Fig. 5. T_{df} Degradation on Dynamic NBTI of Level Restorer Circuit

increases 2.80% for 10^8sec. , while that on HDM is almost constant.

C. NBTI Degradation of Routing Path on FPGAs

We estimate delay degradations of routing paths by tri-state inverters and level restorers on conventional FPGAs. We assume that a routing path includes four tri-state inverters and two level restorers as in Fig. 6. We evaluate rise and fall time delay (T_{df}) degradation affected by dynamic NBTI on three types of variations, TT, SS and FF. We use the two models explained in section III. The results are shown in Fig. 7-8.

Note that rise delay time is decreasing at all models and variations. It is due to the structure of the level restorer. When the input of the level restorer (IN) rises, the output of INV1 falls and that of INV2 rises. Because of NBTI degradations, the fall time of INV1 becomes faster, while the rise time of INV2 becomes slower. MLR turns off when INV2 rises. When INV2 rises, MLR turns off since V_{gs} of MLR becomes less than V_{th}. It turns off faster since V_{th} increases after NBTI degradation. Two PMOSs, in INV1 and MLR, decreases delay time and one PMOS in INV2 increases delay time. As the result, rise time delay becomes smaller at any conditions.

As for fall delay time, behaviors are little bit complicated. The rise time of INV1 decreases, while the fall delay time of INV2 increases because of the NBTI degradation. MLR turns on if $|V_{\mathrm{gd}}| > V_{\mathrm{th}}$ and $|V_{\mathrm{gs}}| > V_{\mathrm{th}}$. If IN is high, MLR is on since $|V_{\mathrm{gd}}| > V_{\mathrm{th}}$. When IN is rising, It will be turn off if $|V_{\mathrm{gd}}| < V_{\mathrm{th}}$ or $|V_{\mathrm{gs}}| < V_{\mathrm{th}}$. It is very difficult to qualitatively estimate if the delay time increases or decreases. As in Fig. 8, fall delay time is fluctuated. In the FF condition, fall delay time increases by 3.0% and 0.7% on IDM and HDM. But in the SS condition, fall delay time is almost constant on both IDM and HDM.

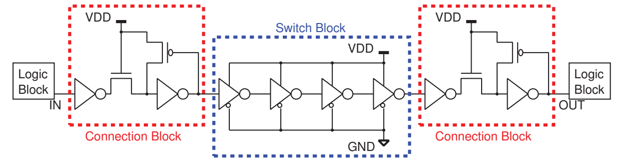

Fig. 6. Routing Path Circuit on FPGAs. We Assume Pulse Passes Through 4 Tri-State Inverters and Two Level Restorer Circuits from Logic Block to Logic Block.

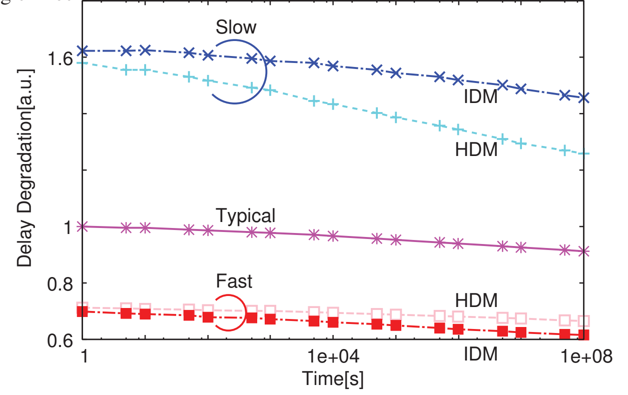

Fig. 7. Rise Delay Time on FPGA Routing Path

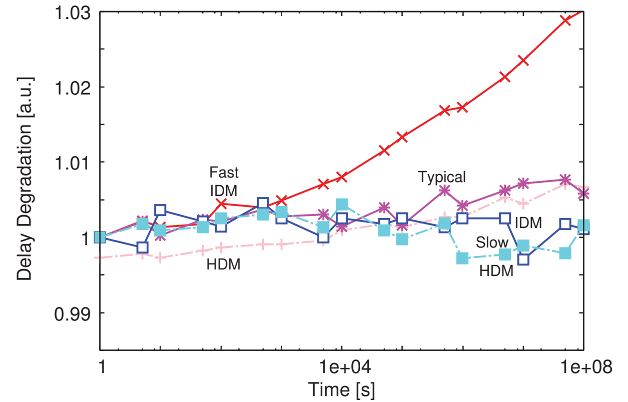

Fig. 8. Fall Delay Time on FPGA Routing Path

V. Discussion

We propose the Inhomogeneous Degradation Model (IDM) considering that fast PMOS devices are the most sensitive to NBTI [7]. Table II shows that fast PMOS devices cause bigger performance degradation than other two variations. But fast PMOS devices are not dominant factors determining the critical path delay. Circuit design guardbands do not care about degraded fast PMOS. Slow PMOS devices determining the critical path delay are robust to NBTI on the IDM. Circuit performance is not degraded by slow PMOS. In Table II, evaluations with IDM are 1/3 of those with HDM after 10 years on slow variations. According to this, we are able to reduce circuit design guardbands of ASICs to 1/3 from the conventional pessimistic value assuming the HDM.

As for FPGAs, we evaluate NBTI delay degradation of the level restorer. It only becomes slower in the IDM and the FF conditions. We also evaluate the delay degradations of the typical routing path on FPGAs consisting of the level restorers and tristate inverters. Unlike the conventional logic gates on ASICs, there is no delay degradation in the HDM. In the IDM, the delay time of the routing path becomes slower only under the FF condition. It can be concluded that the pull-up PMOS in the level restorer relieves NBTI degradations.

VI. Conclusion

We estimate circuit performance degradation affected by NBTI considering variations. We evaluate these two models: Homogeneous Degradation Model(HDM) and Inhomogeneous Degradation Model(IDM). HDM assumes that V_{th} degradation are equivalent at any variation, while IDM assumes that V_{th} degradation are different by variations. Oscillating frequency decreases by 6.63% on the ring oscillators of NOR gate under the FF condition after 10^8sec. (about 3 years) in the dynamic NBTI where stress and recover are alternately applied to PMOS. Performance of circuits on fast transistors caused by variations is more sensitive to NBTI than that on slow ones in the IDM. We assume that NBTI degradation on slow devices is 1/10 than fast devices in the IDM, in which circuit design guardbands can be reduced to 1/3 compared with the HDM.

As for the level restorer circuits widely used in conventional FPGAs, the delay time is increased under the very limited condition. It becomes slower in the IDM under the FF condition. The pull-up PMOS in the level restorer relieves NBTI degradations. The routing paths on FPGAs including level restorers and tristate inverters have the same tendency with the level restorer. The delay time of the routing path is almost constant at any condition except for the IDM under the FF condition. The timing yield of FPGAs is defined by slow transistors on the critical path. Thus, NBTI degradation considering variations is not critical since it is serious in faster devices which do not influence circuit performance.

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