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LETTER

Frequency Dependence of Soft Error Rates Induced by Alpha-particle and Heavy Ion

Haruto Sugisaki[1, a)], Ryuichi Nakajima[1, b)], Shotaro Sugitani[1, c)], Jun Furuta[2, d)], and Kazutoshi Kobayashi[1, e)]

Abstract We conducted a study on the frequency dependence analysis of soft error rates using the test circuit composed of scan flip-flops (FFs) and inverters. By irradiating the circuit with alpha particles while the clock was running, soft error rates were measured. During alpha-particle irradiation, soft errors caused by inverters were almost negligible. Soft errors caused by FFs decreases as the operating frequency increases. On the other hand, during Ar irradiation, soft error rate was nearly constant with varying frequency. This is because, the increase in soft errors caused by inverters was roughly equal to the decrease in soft errors caused by FFs unlike alpha-particle irradiation.

key words: Soft error, Single Event Transients, Single Event Upsets, Frequency Dependence, Dynamic Irradiation

Classification: Integrated circuits

1. Introduction

In recent years, the miniaturization of transistors has led to a decrease in reliability, which has become a concern [1, 2, 3]. One of the factors contributing to this reliability degradation is the soft error [4]. Soft errors occur when a radiation strikes a transistor in an integrated circuits, causing a stored value of a latch or flip-flop (FF) to flip [5]. On Earth, alpha particles and neutrons, while in space, heavy ions are the main factors causing soft errors.The cause of soft errors can be classified into two types: a Single Event Transient (SET) occurs in combinational circuits and Single Event Upset (SEU) occurs within a storage element [6]. As an operating frequency increases, soft errors induced by SETs increase [7, 8]. Measuring soft error rates depending on operating frequency is crucial for designing better soft-error-resilient systems.

So far, various radiation-tolerant FFs have been proposed [9, 10, 11, 12, 13, 14]. However, these designs only address SEU. Soft errors that occur in actual operating environments can also be influenced by SET events that happen outside of FFs. Various characteristics related to SET have been reported as well [15, 16, 17]. In static soft error tests, the clock of flip-flops is stopped for test, so only SEUs can be observed [18]. Therefore, the soft error rate corresponding to actual operation cannot be observed. To approach real environmental conditions, a circuit capable of simultaneously measuring SET and SEU is necessary.

However, there are several issues in designing such a measurement circuit. When using high-speed signals in conventional static soft error measurement circuits, the clock disappears. The pulse width narrowing phenomenon causes the clock pulses to shorten each time they pass through a buffer as shown in Fig. 1. Additionally, there is an issue of increasing momentary current, and a circuit is needed to retain the errors.

To address these issues, two types of clock-distribution circuits were made in this study. A circuit combining buffer chains and a clock tree are used [19, 20]. This prevents the disappearance of the clock signal by reducing the number of buffers through which the signal passes. By shifting the timing of clock distribution to all FFs, the momentary current can be reduced. Additionally, detected errors can be stored by using scan-type FFs to loop the signal.

Using the designed circuit, irradiation experiments were conducted to measure SEUs induced by a SET pulse from outside and inside of FFs. Measurements were taken under irradiation from alpha particles, the main cause of soft errors on Earth, as well as from secondary particles originating from neutrons, namely Ne and Ar. By determining each value, it is possible to understand how SET and SEU change depending on the operating frequency. SET occurred only under Ar irradiation test.

This paper consists of two major parts. First, we propose a circuit structure for measuring soft error rates while applying clock signals the clock operational. We explain the dynamic soft error test circuit, clock signal transmission circuit, and oscillator circuit. In the second part, we present the experimental results using alpha particles and heavy ions, and discuss their analysis [21].

[1]Graduate School of Science and Technology, Kyoto Institute of Technology, Matsugasaki Sakyo-ku, Kyoto 606–8585, Japan

[2]Graduate School of Computer Science and Systems Engineering, Okayama Prefectural University, Soja-shi, Okayama 719-1197, Japan

a) hsugisaki@vlsi.es.kit.ac.jp

b) rnakajima@vlsi.es.kit.ac.jp

c) ssugitani@vlsi.es.kit.ac.jp

d) furuta@c.oka-pu.ac.jp

e) kobayashi@vlsi.es.kit.ac.jp

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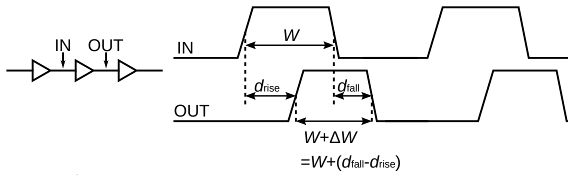


Fig. 1: Pulse width narrowing phenomenon

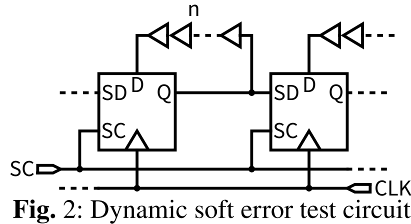


Fig. 2: Dynamic soft error test circuit

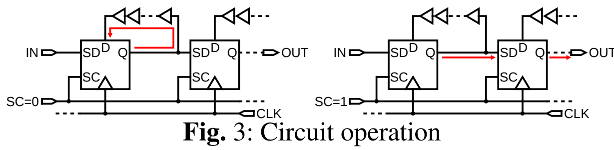


Fig. 3: Circuit operation

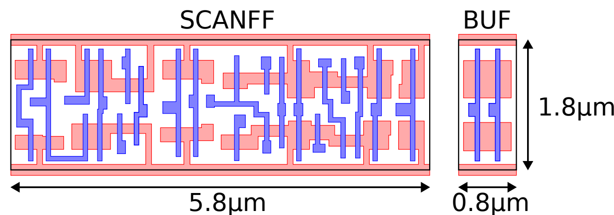


Fig. 4: Layout of the standard cells of a scan FF and a buffer

2. Test Circuit

In this section, we describe the circuit structure used for dynamic soft error tests, composed scan FFs and inverters.

2.1 Dynamic soft error test circuit

During dynamic soft error tests, the clock signal (CLK) must be continuously applied. One of conventional soft error tests is to cascade FFs. However, captured errors in FFs disappear. Therefore, it is mandatory to construct a circuit that can store captured errors while applying a clock signal. In this study, we mused dynamic soft error tests by using scan FFs. Scan FFs are circuits in which, when SC = 0, the input D is captured, and when SC = 1, the input SD is captured [22]. Fig. 2 shows the circuit diagram of the dynamic soft error test circuit, and Fig. 3 illustrates its operation. In contrast to previous research, inverters were placed within the signal loop [23]. When SC = 0, the output Q of FF becomes its own input D, and the signal loops to enable dynamic soft error test. When SC = 1, Q becomes the next stage's SD, making it possible to read out errors.
The design was conducted with a total of 10 buffers. The layout and dimensions of the standard cells used on the chip are depicted in Fig. 4.

2.2 Clock signal transmission circuit

During dynamic soft error tests, high-speed clocks of the

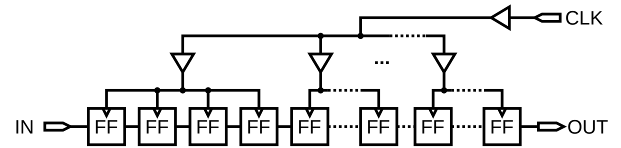


Fig. 5: Clock Tree

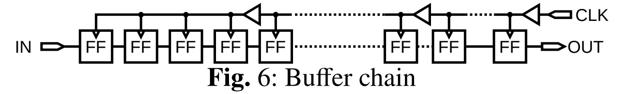


Fig. 6: Buffer chain

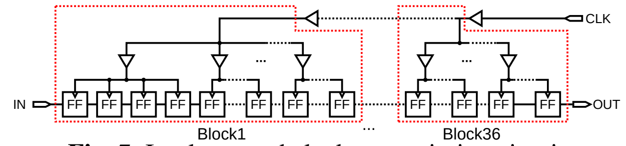


Fig. 7: Implemented clock transmission circuit

order of GHz are injected, to drive circuits capable of transmitting high-speed clocks. When reading out the test results during the shift operation, hold violations must be avoided. Furthermore, transmitting the clock to a large number of FFs raises concerns about the timing of clock inputs and dynamic current. Therefore, some kind of a new clock propagation circuit is required in the clock transmission method.
There is also a method of using decap cells to avoid IR drop [24, 25]. However, we did not use this method in this study to integrate as many FFs as possible on the chip.
There are two existing methods for clock transmission: the clock tree and the buffer chain [19, 20]. Figs. 5 and 6 illustrates the circuit diagram of the clock tree, and the circuit diagram of the buffer chain respectively.
The clock tree allows simultaneous clock input to all FFs, minimizing clock skew. Since, a large number of FFs are used in the dynamic soft error test circuit, transmitting the clock to all FFs by the clock tree would result in a sudden surge of current, causing IR drop and risking malfunctions. On the other hand, clock propagation using buffer chains equalizes current by shifting the timing of clock transmission. However, clock skew must be taken into consideration. When multiple stages of buffers are connected to transmit high-frequency signals, the clock may disappear. Therefore, using a large number of stages in the buffer chain is not feasible. Therefore, in this test, we utilized the circuit shown in Fig. 7, which combines the buffer chain and the clock tree.

2.3 Oscillator circuit

Generally, Phase Locked Loop (PLL) circuits are used in oscillator circuits [26]. However, PLLs have complex circuit structures. In this test, a circuit capable of setting finely detailed frequencies at high frequencies is required to measure soft errors at various clock frequencies. Therefore, a circuit combining seven ring oscillators and dividers was employed. The measurable frequencies range from 8.0 MHz to 1.8 GHz, with 56 steps.

3. Alpha-particle irradiation

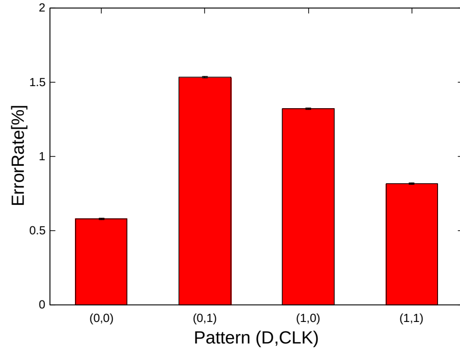


Fig. 8: Results of static soft error test during alpha-particle irradiation

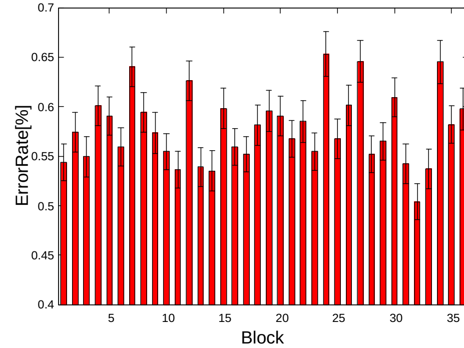


Fig. 9: Error rates for each block when both the input signal and clock signal are 0

3.1 Experimental methods with alpha-particle

A chip equipped with the circuit described in the previous chapter was fabricated in the 65 nm bulk process, and its soft error torelance was evaluated by alpha particle irradiation. Alpha particles are the main source of soft errors occurring on the ground. The alpha particle source had a radioactivity of 3 MBq and consisted of ^{241}Am. The core voltage for the chip was set to the standard voltage of 1.2 V, and tests were conducted at each frequency for 30 seconds, with a total of 300 tests.

Here is an explanation of the test procedure.

1) Place the alpha particle source on top of the circuit.
2) Write values into the test circuit and leave it for a certain period.
3) For dynamic soft error tests, keep the clock running during this period.
4) After the designated test time has passed, read the stored values and record the number of errors.

3.2 Static soft error test

Soft error rates were measured with the clock fixed at 0 or 1, respectively, for cases where the input signal was 0 or 1. This test is conducted using a method similar to the conventional soft error test [18, 27]. Since the clock transmission circuit combines the clock tree and the buffer chain. We defined ”1 block” as 128 FF stages in which the clock signal is distributed in a single clock tree. The test results are shown in Figs. 8 and 9. Fig. 8 shows the error rate for each value of the clock signal CLK and the input signal D. Fig. 9 shows the error rate for each block when both CLK and D are 0.

The test results showed slightly different error rates for each block. Even when repeating the tests, similar trends in the values were observed. Therefore, We consider that these variations are due to process variation.

3.3 Dynamic soft error test

Using an oscillation circuit, we measured the error rate with the clock input to the test circuit. Similar to the static soft error test, we measured the error rate for each block. The test results for the error rates of five blocks, are shown in Fig. 10. These five blocks can still receive clock signals even

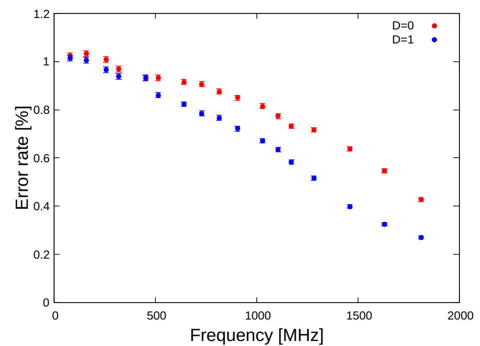


Fig. 10: Dynamic soft error rate during alpha-particle irradiation within the range of blocks 32 to 36

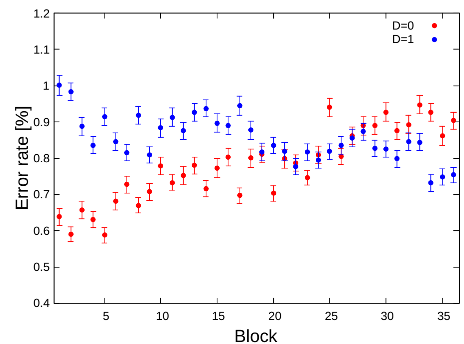


Fig. 11: Error rates for each block at 730 MHz

when the operating frequency was set to its maximum for test. Regardless of whether the input value was 0 or 1, the error rate decreases as the operating frequency increases. When the operating frequency is 906 MHz, the error rate decreased by approximately 18% under the condition of D = 0 compared to 0 MHz. Under the condition of D = 1, the error rate decreased by about 32%.

Fig. 11 depicts the error rates for each block at 730 MHz, where the clock was transmitted to all blocks. The error rates for each block linearly increses. This is because the duty cycle decreases for each block due to the pulse width narrowing phenomenon.

When a high-frequency clock signal was input to the circuit, the clock signal did not propagate to all blocks. Fig. 12

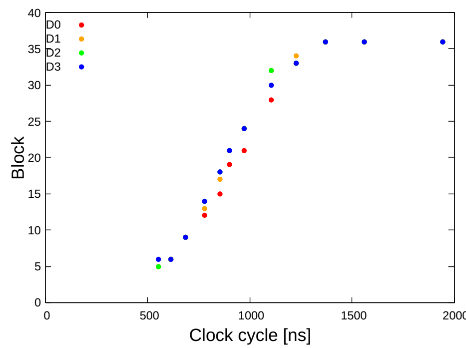


Fig. 12: Clock cycle v.s. the number of transmitted blocks

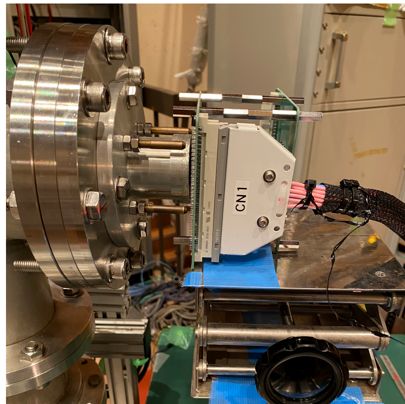


Fig. 13: Process of heavy-ion irradiation experiments

shows the relationship between the one clock period and the number of transmitted blocks.

As the one-cycle time of the clock signal becomes shorter, the number of blocks where the signal propagates decreases linearly.

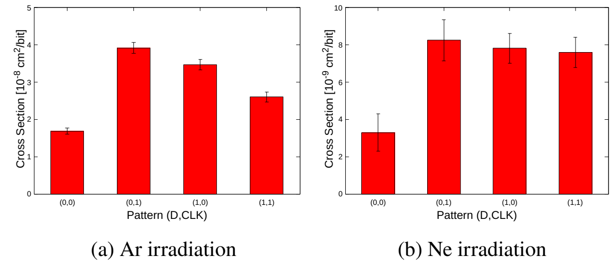
4. Heavy-ion irradiation

4.1 Experimental methods with heavy ion

We conducted a resilience evaluation using heavy-ion irradiation at Cyclotron and Radioisotope Center (CYRIC) at Tohoku University. Ne and Ar were irradiated. Soft error tolerance is often assessed using Ar [28, 29].

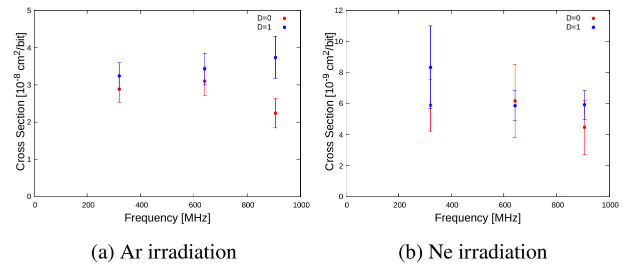
The maximum LET (Linear Energy Transfer) of secondary ions produced by neutron collisions is approximately 18 MeV-cm^2/mg [30]. The energy transferred to a material by charged particles is known as LET. The charge density generated is proportional to LET. When particles with a high LET value pass through, the charge density also increases. The resilience on the terrestrial region is sufficient if there are no soft errors caused by heavy ions with LET = 18 MeV-cm^2/mg. Therefore, in this experiment, Ne with an LET of 6.5 MeV-cm^2/mg and Ar with an LET of 15.8 MeV-cm^2/mg were used. Fig. 13 shows the process of heavy-ion irradiation experiments.

VDD was set to the standard voltage of 1.2 V, and tests were performed for 30 seconds at each frequency, repeated 10 times. Here is an explanation of the test procedure.



(a) Ar irradiation (b) Ne irradiation

Fig. 14: Results of static test



(a) Ar irradiation (b) Ne irradiation

Fig. 15: Results of dynamic test

1) Position the board to ensure that heavy ions hit the circuit.
2) Irradiate heavy ions.
3) Write the values in the test circuit and allow them to sit for a certain amount of time.
4) Leave the clock running for dynamic soft error test.
5) After the test time has expired, read the retained values and record the number of errors.

4.2 Static soft error test

We measured the error rates by setting the clock and data input signal to 0, or 1, similar to alpha-particle irradiation. As Fig. 14 Ar and Ne irradiation results, respectively. The results were similar to those obtained during alpha-particle irradiation.

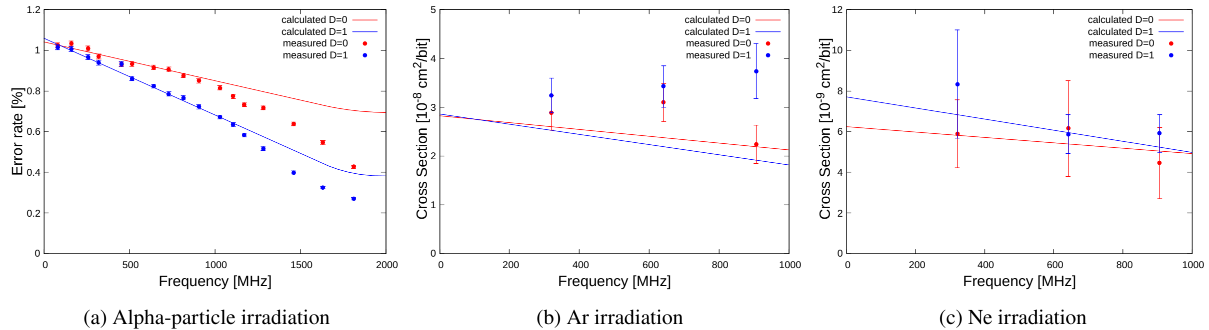
4.3 Dynamic soft error test

We measured the error rates by applying the clock to the test circuit using one of the embedded oscillators. To compare with alpha-particle irradiation results, we obtained results for 5 blocks out of the 32 to 36 blocks. These five blocks can still receive clock signals even when the operating frequency was set to its maximum for test.

Fig. 15 show the test results of Ar and Ne irradiation. Unlike alpha-particle irradiation, the error rate remained almost unchanged even when the operating frequency increased during Ar irradiation. Ar has higher energy than alpha-particle. Therefore, the increase rate of SETs is almost same as the decrease rate of SEUs.

5. Discussion

Then we are going to distinguish SEUs and SETs. We extract the SET error rates from the dynamic test by subtracting the SEU rates during static soft error tests. The procedure for



(a) Alpha-particle irradiation (b) Ar irradiation (c) Ne irradiation

Fig. 16: Comparison between calculated and measured values of SEU

deriving SEU when D = 0 is as follows. The error rates when clock is 0 or 1 during the dynamic test are equivalent to those of the same clock states during the static test. To determine the SEU error rate, it is necessary to obtain the duty cycle of the clock signal to the FF. In this circuit, we have to consider the pulse width narrowing phenomenon (Fig. 1), which affects the duty cycle. Furthermore, we must consider the delay in the test circuit. Errors that occurred just before this, rising edge of CLK cannot be captured due to the setup time violation. Furthermore, we should take into account the possibility that the clock signal may disappear when the clock width falls below a certain threshold. In this circuit, the pulse width reduction per stage can be estimated to be approximately 11 ps, based on the variation of error rates for each block in Fig. 11. By using SPICE simulations, it was found that the inverter delay between FF output and input in the test circuit is approximately 300 ps. Using these values, the calculated SEU results are shown in Fig. 16.

The calculated values up to 1 GHz are closely aligned with the results of alpha particle irradiation. However, there is a significant deviation from the calculated values beyond 1 GHz. In this circuit, a ring oscillator and a frequency divider are used to generate the clock signal. For frequencies exceeding 1 GHz, the signal from the ring oscillator is directly injected as the clock without the frequency divider. Therefore, the signal that has passed through pulse width narrowing within the oscillator circuit, particularly within inverters, is output as the clock without passing through the frequency divider. The reason why the error rates are different from the calculated values is that the duty cycle of CLK is not exactly 0.5. The measured values below 1 GHz have higher correlation with the calculated SEU values, indicating that in this circuit, there is only a minimal amount of SET occurrence. The reason for this is the low energy of the alpha particles used in our experiment, which leads to narrow SET pulse widths during irradiation. Additionally, when the generated SET pulse width is small, it may disappear due to the pulse width narrowing phenomenon before reaching the FF. Therefore, SETs almost never occurred. Similarly, during Ne irradiation, SETs were hardly observed. As the operating frequency increases, Ar irradiation results in a deviation from the calculated values. The reason for this is the significant presence of SET, unlike with alpha particle irradiation. With high LET values characteristic of Ar, the generated SET pulse width is large. Therefore, the SET pulses are less likely to disappear due to the pulse width narrowing phenomenon and more likely to reach the FF. As a result, errors are more easily captured by the FF, leading to an increased occurrence of SETs. The difference between calculated and measured values is presumed to be due to SET. Therefore, at 906 MHz, approximately one-third of the total soft errors during Ar irradiation are considered to be SETs.

6. Conclusions

We implemented a circuit for soft error assessment using scan flip-flops and inverters, and evaluated the soft error rates at various frequencies using alpha-particle and heavy-ion irradiation experiments. There were almost no errors caused by SET during alpha-particle irradiation. At 906 MHz and D=0, the error rate decreased by 18%, and D=1 led to a 32% decrease. Similar trends were observed during Ne irradiation as well.

Unlike alpha-particle irradiation, the error rate remained almost unchanged even when the operating frequency increased during Ar irradiation. SET is estimated to be responsible for approximately one-third of the total soft errors during Ar irradiation at 906 MHz.

SEU is significantly affected by the delay times of the circuit. As the operating frequency increases, the error rate during circuit operation decreases as compared to that measured statically, given the linear decrease in SEU. The influence SET can be almost ignored in alpha-particle irradiation, particularly for circuits that do not heavily rely on combinational logics. Considering the impact of SET is crucial for high-energy particles like Ar ions.

7. Acknowledgment

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