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LETTER

An E-mode p-GaN HEMT monolithically-integrated three-level gate driver operating with a single voltage supply

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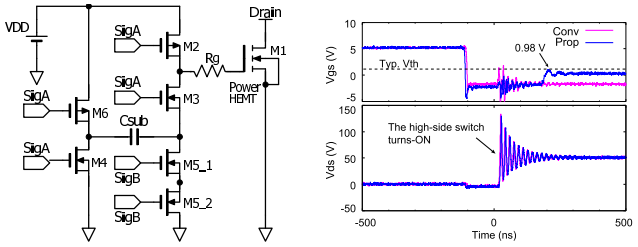
Abstract A three-level gate driver and a power Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) were monolithically integrated to prevent false turn-on, reduce reverse conduction loss and realize fast switching. The proposed gate driver works with an external and an integrated capacitor which supply negative gate voltage. Monolithic integration makes power conversion circuits smaller in size and improves circuit performance due to its lower parasitics. The integrated MIM (Metal-Insulator-Metal) capacitor improves dv/dt immunity. Measurement results showed that the proposed GaN-IC realized fast switching speed of 3.7 ns t_{on} and 6.1 ns t_{off}, and improved efficiency of an SR buck-converter.

Keywords: GaN HEMT, monolithic integration, three-level gate driver, false turn-on, reverse conduction loss, high-speed switching

Classification: Power devices and circuits



(a) Circuit structure. (b) Measurement waveforms of a half-bridge switching test circuit.

Fig. 1 Proposed 3-level gate driver [16].

1. Introduction

Nowadays, GaN HEMTs are gaining more attention due to its intrinsic benefits such as high switching speed, high breakdown voltage, high thermal conductivity and low on-resistance [1, 2, 3, 4, 5, 6]. They offer a great advantage in downsizing the power electronics circuits. Despite all these, GaN HEMTs suffer from false turn-on phenomena and reverse conduction loss. Owing to the low threshold voltage (V_{th}) and high switching speed, false turn-on more frequently occurs than Silicon (Si) devices [7, 8, 9, 10, 11]. In bridge-circuits like an SR buck converter, false turn-on loses a large amount of power by shoot-through current [12]. The conventional 2-level gate driving method applies negative voltage to the gate terminal of a power GaN HEMT. The reverse conduction characteristics comes from their lateral structure in the absence of a body diode [13, 14]. Reverse conduction loss is increased during the freewheeling operation. The 3-level gate driving method, in which negative voltage is applied during turn-off to eliminate false turn-on, is effective to address those problems [15]. However, in conventional methods, an additional circuit is required to generate negative voltage, resulting in a larger circuit area and more power loss. Therefore, we proposed a capacitor-based 3-level gate driver [16]. The capacitor works as a voltage source to supply negative gate voltage without any additional voltage source. The proposed gate driver was first implemented by discrete components with Si MOSFETs. Fig. 1 presents the 3-level gate driver to overcome the false turn-on and reverse conduction loss in a half-bridge switching test circuit.

In order to take advantage of the lateral structure and high breakdown field of GaN HEMTs, monolithic integration of GaN circuits (GaN-IC) is very promising due to its reduced parasitic inductance, smaller circuits area and its superior switching performance [17, 18, 19, 20]. In conventional circuits consisting of discrete components, switching speed is limited by gate resistance, which is required to suppress the switching noise induced by parasitic inductance. On the other hand, monolithic integration fully utilizes the fast switching capability of GaN HEMTs because the parasitic inductance on the gate terminal is significantly minimized, resulting in improvement of power efficiency [21, 22].

In this work, we monolithically integrated the proposed 3-level gate driver and a power GaN HEMT by an E-mode (Enhancement-mode) GaN-on-SOI process [23]. We aim to achieve further high-speed switching and stable operation with small circuit area by integrating the proposed gate driver and the power HEMT on a chip. Measurement results confirmed that the proposed GaN-IC operated at 3 levels and improved the efficiency of an SR buck-converter.

This paper is organized as follows: the motivation of our research is explained in Section 2. Section 3 describes the design and operation principle of the proposed GaN-IC. Section 4 presents the measurement results and finally Section 5 concludes this paper.

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2. Motivation

2.1 Problems of GaN HEMTs and previous works

GaN HEMTs have some disadvantages such as false turn-on and high reverse conduction loss. False turn-on, in a bridge-circuit, is serious problem for GaN HEMTs. The false turn-on consumes a large amount of power. Fig. 2 depicts mechanism of false turn-on at the low-side switch. When the high-side switch turns on, high dv/dt noise appears at the drain terminal. After then, Miller current flows to the gate driver through C_{GD} causing gate voltage ringing. If this ringing voltage reaches V_{th} , the low-side switch is turned on, then the shoot-through current begins to flow. This is the false turn-on phenomena, which more frequently appears in GaN HEMTs owing to its low V_{th} . Usually, negative voltage is used to address this phenomenon, which is called the 2-level method in this paper. However, an additional power supply to generate negative voltage is required. In the case of GaN HEMTs, negative gate voltage during dead time increases the reverse conduction loss, because they have reverse conduction characteristics as shown in Fig. 3 [24]. If GaN HEMTs are driven with a negative voltage during dead time, the voltage drop V_{SD} becomes larger than the forward voltage of the body diode of MOSFETs.

To overcome these problems, several gate drivers have been proposed. Some companies recommend a gate driver using a speed-up capacitor (Fig. 4) [25, 26]. It is driven by

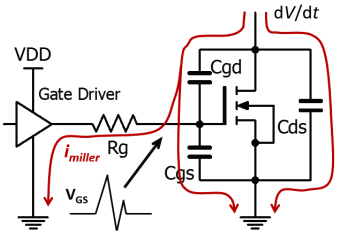


Fig. 2 Mechanism of false turn-on.

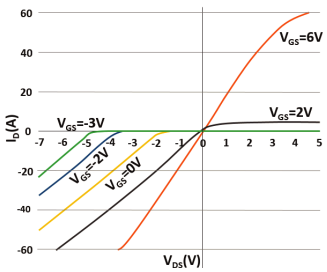


Fig. 3 I-V curve of GaN HEMTs [24].

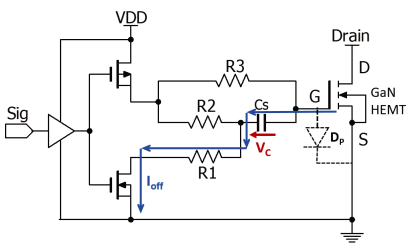


Fig. 4 Gate driver using speed-up capacitor.

negative voltage at turn-off, and V_{GS} becomes 0 V just before the high-side switch turns on. However, this circuit is only applicable to GaN HEMTs which have diode characteristics between gate and source terminals. In [27], a 3-level gate driver has been proposed. However, an additional power supply to generate the negative voltage is required, increasing circuit area. Therefore, we proposed a 3-level gate driver without any additional power supply to generate the negative voltage. Instead of that, the capacitor in the gate driver works as a negative voltage source.

2.2 Monolithic integration

The great advantage of GaN HEMTs is that the power HEMT is monolithically integrated with a gate driver in the same chip. This method offers smalller circuit area and superior switching performance compared to conventional discrete driving methods due to the reduction of parasitic inductance. Therefore, it is expected to be a promising candidate and also the related works have been reported the same in [28, 29, 30]. However, there are still few papers that take into account the problems of GaN HEMTs. In this work, to overcome the problems of the GaN HEMTs and improve switching performance, we integrated the proposed 3-level gate driver and a power HEMT on a single chip.

3. Design of monolithic GaN integrated circuit

3.1 Proposed 3-level GaN-IC

Figures 5 and 6 show the proposed 3-level GaN-IC with an external MOSFET (M6) and its control waveforms, respectively. The capacitor C_{sub} works as a voltage source to supply negative voltage to the gate terminal during turn-off transient. C_{sub} is implemented by an integrated small MIM capacitor and an external large discrete capacitor. Its operation principle is as follows (Fig. 7)

a). Current flows along the blue line to the gate terminal, and then the power HEMT turns on. During on-state,

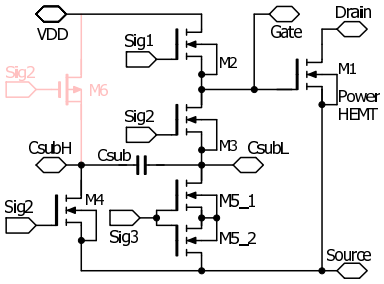


Fig. 5 Structure of proposed 3-level GaN-IC with external MOSFET (M6).

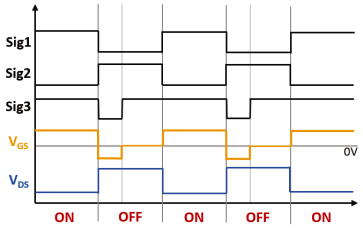


Fig. 6 Control waveforms of proposed 3-level GaN-IC.

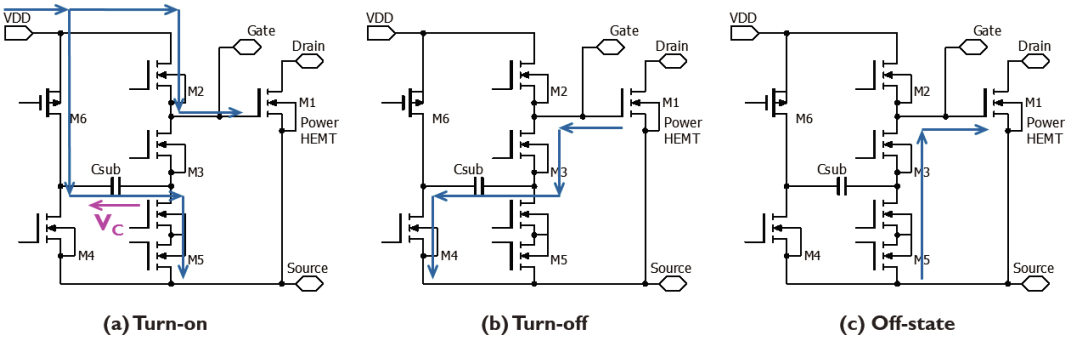


Fig. 7 Operation principle of the proposed GaN-IC.

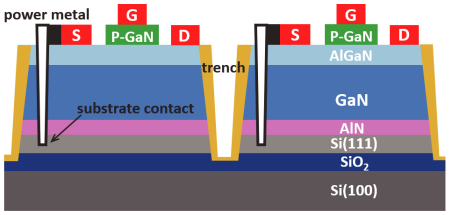


Fig. 8 Cross section of two isolated HEMTs by GaN-on-SOI process.

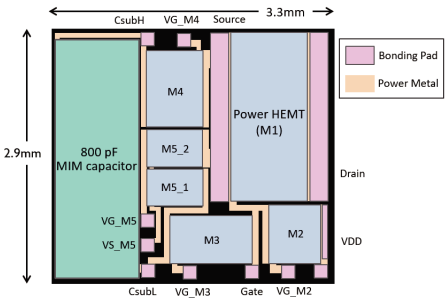


Fig. 9 Layout of proposed 3-level GaN-IC.

current flows to the ground through M6, C_{sub} and M5 and charges C_{sub}. Then, V_c is generated.

b). When power HEMT turns off, current flows to the ground through C_{sub}. Then, C_{sub} operates as a voltage source, the power HEMT is driven by negative gate voltage ($-V_c$).

c). Current flows from the ground to the gate terminal. Then, input capacitance C_{iss} is charged, V_{GS} settles to 0 V to reduce reverse conduction loss.

The three signals (Sig 1-3) must be independently controlled to perform the above operation. Owing to C_{sub}, it can operate at the three gate voltage levels (V_{DD}, $-V_C$, and 0 V) by using only a single voltage supply. The two HEMTs (M5_1 and M5_2) driven by Sig 3 form a common-source-type bidirectional switch to flow current bidirectionally [31].

3.2 Fabrication and layout of the proposed GaN-IC

The GaN-IC was fabricated using the E-mode p-GaN HEMT process on a GaN-on-SOI substrate [32]. Fig. 8 shows the cross section of the HEMTs by the GaN-on-SOI process. Each substrate of HEMTs is isolated by deep trench reaching the buried oxide in order to suppress the back-gating effect and stable operation.

The layout and gate width W_g of the GaN-IC are shown in Fig. 9 and Table I, respectively. Here, a part of the total

Table I Size of HEMTs on GaN-IC.

	M1	M2	M3	M4	M5_1, 2
Wg [mm]	100.0	20.2	28.7	30.0	12.5

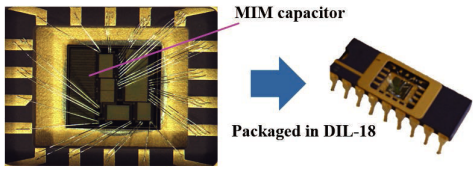


Fig. 10 Photomicrograph of GaN-IC packaged in DIL-18.

C_{sub} capacitance (800 pF) is integrated on chip. According to the previous paper [16], C_{sub} is required larger than a few nF or about 10 nF of the capacitor, to apply enough negative voltage to the gate. Therefore, the 800 pF MIM capacitor is not enough as a negative voltage source but is effective for the stable operation at turn-off and to improve dv/dt immunity by reducing the parasitics. The fabricated chip size is 3.3 mm × 2.9 mm. As shown in Fig. 10, the fabricated GaN-IC was implemented in a DIL-18 package.

4. Measurement results

In this section, measurement results are presented when the proposed GaN-IC is applied to a resistor-load type measurement circuit and an SR buck-converter, and compared with a conventional discrete method.

4.1 Resistor-load type measurement circuit

The resistor-load type measurement circuit for the proposed GaN-IC is shown in Fig. 11. The bootstrap circuit to drive M2 of the GaN-IC consists of a 0.1 µF capacitor (C_{boot}) and a schottky barrier diode (D_{boot}). Because the proposed gate driver requires about 10 nF or more of the capacitor for C_{sub}, a 22 nF ceramic capacitor is externally attached in parallel with the integrated 800 pF MIM capacitor. The pre-driver for the propsed GaN-IC is an isolated gate driver IC (Silicon Labs, SI8275GB). Fig. 12 shows the measured the photograph of the measurement circuit for the GaN-IC. We compare the switching characteristics of the proposed gate driver that composed of the Si MOSFETs and the GaN-IC. In the discrete method, the power GaN HEMT (GaNsystems, GS66504B) was used for the power HEMT and the measurement circuit for the discrete implementation. Switching characteristics are evaluated by switching time as shown in

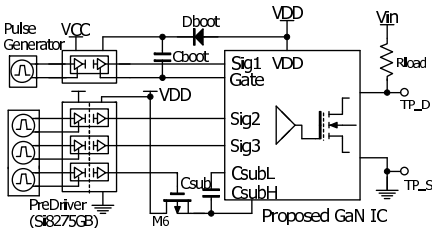


Fig. 11 Resistor-load type measurement circuit for GaN-IC.

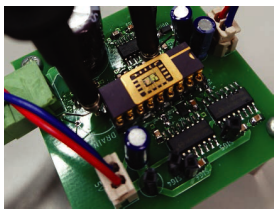


Fig. 12 Photo of measurement circuit for GaN-IC.

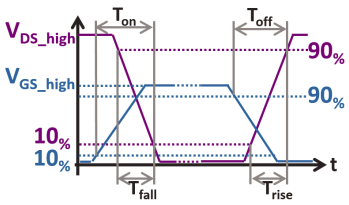


Fig. 13 Definition of switching time.

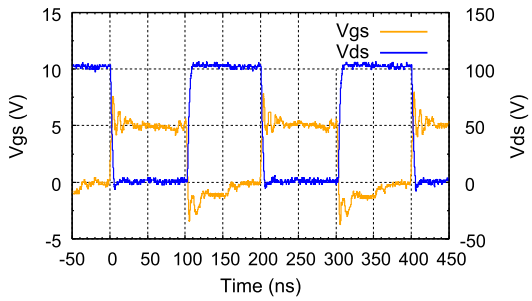


Fig. 14 5 MHz switching waveforms of the proposed GaN-IC at 100 V/4 A obtained by measurement.

Fig. 13.

Figure 14 shows continuous switching waveforms of the proposed GaN-IC at 100 V of V_{in}, 25 Ω of Rload at 5 MHz frequency. It demonstrates that the proposed GaN-IC successfully generates 3-level gate voltage levels without any additional voltage supply under high frequency operating condition of 5 MHz. Thanks to the 3-level operation, the proposed GaN-IC has dv/dt immunity and reduces reverse conduction loss during the freewheeling operation in bridge circuits.

Figure 15 shows the measurement waveforms of the V_{GS} and the V_{DS} of the GaN-IC and the discrete implementation at 50 V of V_{in}, 25 Ω of Rlaod at 1 MHz frequency. Evaluation results are shown in Table II. Thanks to monolithic integration, the GaN-IC achieved 3.7 ns t_{on} and 6.1 ns t_{off}, which are 23% and 51% faster than the discrete one, respectively.

4.2 SR buck-converter

To verify the effectiveness of the proposed GaN-IC, both

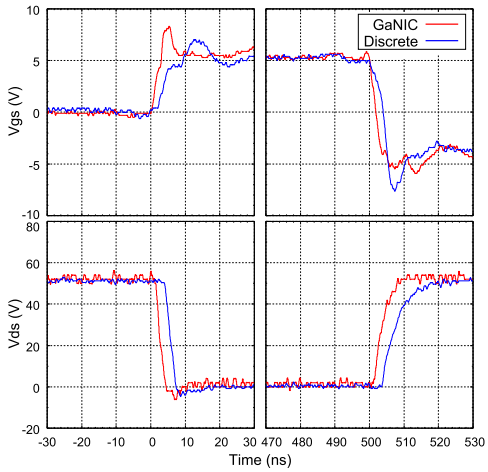


Fig. 15 1 MHz switching waveforms of power HEMT at 50 V/2 A (discrete method vs. proposed GaN-IC) obtained by measurement.

Table II Evaluation results of the switching time.

	Discrete	GaN-IC
t_{on}	4.8 ns	3.7 ns (−23%)
t_{fall}	2.6 ns	2.2 ns (−15%)
t_{off}	12.4 ns	6.1 ns (−51%)
t_{rise}	8.6 ns	4.3 ns (−44%)

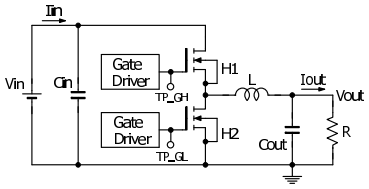


Fig. 16 Simplified schematic of SR buck-converter.

methods (the 3-level GaN-IC and the conventional 2-level method) were evaluated with an SR buck-converter (Fig. 16). This circuit has a half-bridge configuration, and the low-side switch has a reverse conduction mode. We compared efficiency when the proposed GaN-IC and the 2-level method are used for the low-side switch, respectively. Si8275GB and GS66504B were used for the conventional 2-level method, and the negative gate voltage was set to −3 V. In both measurements, Si8275GB is used to control the high-side switch GS66504B. When the GaN-IC is also applicated to the high-side, the switching loss and dv/dt are different from the GS66504B driven by the Si8275GB (conventional 2-level method), and the effectiveness of the driving method of the low-side cannot be evaluated. Therefore, in this paper, the GaN-IC is applicated to only the low-side and the high-side switch is driven by the conventional 2-level method for comparison. The circuit parameters of the designed SR buck-converter are shown in Table III.

Figure 17 shows the measurement waveforms of the proposed GaN-IC at the output power of 48 W. As shown in Table IV, the proposed GaN-IC improved the efficiency compared to the conventional method, owing to lower switching loss and reverse conduction loss by 3-level driving and monolithic integration. In addition, the proposed GaN-IC has capability to overcome false turn-on as shown in Fig. 18 (a).

Table III Circuit parameters of the SR buck-converter.

Circuit Paramiter		Value
Input Voltage	V_{in}	48 V
Output Voltage	V_{out}	12 V
Output Power	P	48, 24 W
Load Resistance	R	3, 6 Ω
Inductor	L	10 µH
Input Capacitance	C_{in}	22 µF
Output Capacitance	C_{out}	47 µF
Dead Time	T_{dead}	50 ns
Switching Frequency	f_{sw}	1 MHz

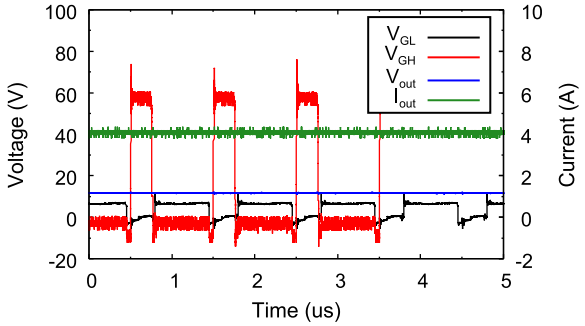


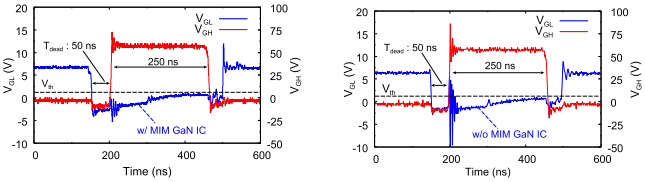
Fig. 17 Measurement waveforms of the 48 V - 12 V/4 A SR buck-converter using a proposed GaN-IC for the low-side switch.

Table IV Evaluation results of the SR buck-converter.

	Conventional		GaN-IC	
Power	24 W	48 W	24 W	48 W
Vin [V]	50.2	50.6	50.3	51.1
Iin [A]	0.62	1.02	0.52	0.97
Vout [V]	12.0	11.3	11.8	11.7
Iout [A]	2.04	3.82	1.99	4.07
Pin [W]	31.1	51.7	26.0	49.8
Pout [W]	24.5	43.3	23.5	47.5
Efficiency	78.9%	83.8%	90.2%	95.4%

In order to investigate the effectiveness of the integrated MIM capacitor, we also fabricated another type of the proposed GaN-IC without the integrated MIM capacitor, and applied to the SR buck-converter. As shown in Fig. 18, the GaN-IC without the integrated MIM capacitor suffers from larger gate voltage ringing over V_{th} when the high-side switch turned on. When the MIM capacitor is integrated, the Miller current flows to the ground through the M3, M4 and MIM capacitor instead of the external capacitor due to the large parasitic components along it. When the MIM capacitor is not integrated, the current flows only through the external capacitor. There are larger parasitics on the current path, resulting in increase of the ringing. Therefore, the ringing caused by the Miller current can be suppressed by the MIM capacitor.

From the experimental results, the proposed GaN-IC exhibits the high switching capability with the 3-level gate driving operation, without any additional voltage supply. It overcomes the problems such as false-on and high reverse conduction loss of the GaN HEMTs. Therefore, it is highly beneficial to reduce power loss and miniaturize power conversion circuit. Furthermore, dv/dt immunity is improved by integrating the MIM capacitor. Despite a Large integrated MIM capacitor, more stable operation can be realized.



(a) With MIM capacitor. (b) Without MIM capacitor.

Fig. 18 Measurement waveforms of an SR buck-converter using the proposed GaN-IC.

5. Conclusion

This paper proposed a monolithically integrated GaN power circuit with the 3-level gate driver to address the problems of the GaN HEMTs by a p-gate GaN-on-SOI technology. The capacitor in the proposed gate driver behaves as a voltage source to supply negative voltage at turn-off transient to avoid false turn-on. The small integrated MIM capacitor is effective for stable operation. Fast switching and stable 3-level gate drive operation of the proposed GaN-IC were demonstrated experimentally using a single voltage supply. Compared to the proposed gate driver consisting of discrete transistors, the GaN-IC reduces the switching time by 23% at turn-on and by 51% at turn-off, respectively. Thanks to the 3-level operation and high-speed switching, the proposed GaN-IC improved the efficiency of the SR buck-converter compared to the conventional 2-level method. Although the size of the driver circuit is bigger than the power HEMT, the driver circuit successfully generates three different level of voltage level along with high efficiency and fast, smooth switching transition. However, in future we will further look into this.

Acknowledgments

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