

Monolithic integration of gate driver and p-GaN power HEMT for MHz-switching implemented by e-mode GaN-on-SOI process

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Abstract Reducing parasitic coupling components can improve switching performance in electric circuits. A two-stage gate driver and power Gallium Nitride High Electron Mobility Transistors (GaN HEMT) were monolithically integrated for MHz-switching. The monolithic integration improves switching performance owing to minimized parasitic inductance. The proposed GaN-IC was fabricated using an enhancement-mode GaN-on-Insulator process technology. Experimental results showed that the GaN-IC had faster transition and less energy loss than a conventional circuit using a discrete gate driver. The proposed GaN-IC reduced switching time by 86% at turn-off and by 45% at turn-on under off-state $V_{\rm DS}$ of 100 V and on-state $I_{\rm D}$ of 10 A.

 ${\bf key}$ words: GaN-HEMT, monolithic integration, gate driver, high-speed switching, 10 MHz, bootstrap

Classification: Power devices and circuits

1. Introduction

Various GaN (Gallium Nitride) monolithic integrated circuits have been designed [1, 2, 3, 4, 5, 6, 7], to take advantage of a lateral structure and high breakdown field. In particular, commercial products on the market with integrated circuits (a gate driver and a power HEMT) have been drawing much attention [8]. This is because the monolithic integration (Fig. 1 (a)) is very promising due to its superior switching capabilities. In conventional circuits, switching speed is limited by gate resistance to suppress noise induced by peripheral parasitic inductance as shown in Fig. 1 (b). However, in monolithic integration, parasitic inductance is minimized and switching is fast and noiseless; this leads to improved power efficiency [9, 10, 11, 12]. Additionally, it reduces volume of power converters by decreasing the weight and volume of the passive components at high frequency switching [13]. Owing to those advantages, GaN-HEMTs application in chargers and electric vehicles [14, 15, 16, 17]

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DOI: 10.1587/elex.XX.XXXXXXXX Received October 10, 2019 Accepted October 10, 2019 Published December 31, 2019



show great promise.

In this study we monolithically integrated a power GaN-HEMT and a two-stage gate driver by enhancement-mode (e-mode) GaN-on-Insulator substrate called Qromis Substrate Technology (QST®, [18, 19]). Prior studies in [20] have already simulated the function of the proposed monolithic GaN integrated circuit (hereinafter referred as "GaN-IC"). This paper builds on prior research by presenting results of experiments of the proposed GaN-IC at 10 MHz switching frequency. GaN-on-QST process enables the isolation of substrate between high-side and low-side HEMTs, and realizes stable operation. Such an isolation would not be possible for normal GaN-on-Si technology, as this technology may lead to back-biasing effect in monolithic integration due to conductive nature of Si carrier substrate [21, 22, 23] while being generally used in previous monolithic integration research.

This paper is organized as follows: the design of the proposed monolithic GaN integrated circuit is explained in Section 2. In Section 3, experimental characterization results are studied and discussed. Finally, Section 4 concludes this paper.

2. Design of monolithic GaN integrated circuit

2.1 Fabrication

The integrated circuit was fabricated using p-GaN gate enhancement-mode HEMT transistors on insulating substrate called QST. It has a top Si layer with buried oxide layer underneath. An SiO₂ (Silicon Dioxide) layer is embedded in the QST substrate. By processing oxide filled



Fig. 2. Cross section of GaN HEMT on QST substrate.



Fig. 3. Proposed monolithic GaN integrated circuit (IC).



Fig. 4. Input and output signals for switching operation.



Fig. 5. Whole system schematic.

trenches reaching the buried oxide, the HEMT devices can be isolated from each other, allowing a different substrate bias per device. The cross section of the HEMTs is shown in Fig. 2.

2.2 Structure of proposed integrated circuit

The proposed GaN-IC illustrated in Fig. 3 consists of a power HEMT and a two-stage gate driver [24]. The operating waveforms of the GaN-IC can be found in Fig. 4. It works as follows:

1) The complementary input signals, V_{sigL} and V_{sigH} , are

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Table I. Size of HEMTs and resistance.							
	Wg	$L_{\rm gd}$	$L_{\rm gs}$	$L_{\rm fp}$	$L_{\rm g}$		
Power HEMT	70	4	0.75	0.65	1.3		
Q_SH	24	1.5	0.75	0.25	1.3		
Q_SL	24	1.5	0.75	0.25	1.3		
Q_FH	8	1.5	0.75	0.25	1.3		
Q_FL	8	1.5	0.75	0.25	1.3		



 W_{g} : gate width (mm) L_{gd} : gate-drain distance (μ m)

 L_{gs} :gate-source distance (μ m) L_{fp} : gate field plate (μ m)





applied to the gate driver.

- In the first stage, input signals are inverted because the HEMTs Q_FH and Q_FL and resistors configure a pair of logic inverters.
- 3) In the second stage, HEMTs Q_SH and Q_SL form an inverter to drive the power HEMT. When Q_SH is on, V_{GS} is pulled up to V_{DD} . On-state Q_SL pulls V_{GS} down to 0 V.

For the above operation, the GaN-IC requires a pulse generator and a voltage supply employing a bootstrap circuit as shown in Fig. 5. The pulse generator should provide complementary input signals to control switching state. The bootstrap circuit boosts the reference point of VDD, and this enables to remove additional voltage supply.

2.3 GaN-IC layout

Table I shows the dimensions of HEMTs and the resistance values that correspond to the components in the proposed GaN-IC in Fig. 3. The HEMTs in the first stage are designed to have small input capacitance for fast transition, while the HEMTs in the second stage have relatively large gate width to charge and discharge the power HEMT quickly. Owing to this structure, the gate driver is capable of driving the power HEMT at MHz-level switching frequency.

Resistors RH and RL are formed by 2-DEG sheet resistance. The power HEMT in the GaN-IC has 67 m Ω on-resistance $R_{\text{DS(ON)}}$ and can be used at 100 V drain-source voltage.

The simplified layout of the GaN-IC is shown in Fig. 6. Parasitic elements in the GaN-IC were extracted from the layout as seen in Fig. 7.

The parasitic inductance in on-state and off-state paths are 0.43 nH and 0.12 nH respectively. On the other hand, the

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Fig. 7. Parasitic components in IC.

gate-source loop in the discrete implementation method results in much larger parasitic inductance values (Fig. 1 a). For instance, the wire on PCB (Print circuit Board) has 4.0 nH/cm assuming that it has 5 mm of width and 35 μ m thickness. If parasitic inductance in bonding wires and pins on an IC package, as well as in PCB wires is also considered, the discrete implementation method results in even higher parasitic inductance. From the calculation in this study, it is clear that the proposed method greatly reduces parasitic inductance over a higher order of magnitude compared to the conventional discrete implementation.

3. Experimental evaluation of the GaN-IC

This section compares the switching characteristics of the power GaN-HEMT when driven by the gate driver in the proposed GaN-IC (hereinafter referred as "proposed method") and when driven by a commercial discrete gate driver (hereinafter referred as "conventional method").

3.1 Measurement setups

The measurement circuits for the proposed method and the



Fig. 8. Measurement circuit for the proposed method (GaN-IC).



Fig. 9. Measurement circuit for the conventional method (discrete gate driver).



Fig. 10. Measurement system.



Fig. 11. DUT implemented in DIL18 package.

conventional method are shown in Figs. 8 and 9, respectively. The bootstrap circuit in the GaN-IC measurement circuit consists of 1 μ F of C_{BS} and a Schottky barrier diode (Panasonic DB2J20900L). The measurement system is shown in Fig. 10.

Control signals to the gate drivers were generated by an FPGA (Field Programmable Gate Array) (Intel EP1C6Q240) and was programmed to function as a pulse generator. The control signals to the DUT (Device Under Test) were supplied via an isolator (Texas Instruments ISOI7831). In experiments of the proposed method, the gate driver was embedded in the GaN-IC therefore control signals were directly supplied from the isolator. For the conventional method, a discrete gate driver (Maxim Integrated MAX5048) amplified the input signal. Gate resistance $R_{\rm GP}$ and $R_{\rm GN}$ were 2 Ω .

The DUT for the proposed method is shown in Fig. 11. It was implemented in a DIL-18 (Dual-In-Line 18) package. More than 10 bonding wires were attached to the source and drain terminals to reduce resistance to high current and decrease parasitic inductance. The DUT for the conventional method is the power-HEMT in the GaN-IC. The gate driver in the GaN-IC was removed by using focused ion beam (FIB) to cut off the metal power wire between the power HEMT and the gate driver. This made it possible to evaluate the power HEMT which has the exactly same layout patterns as the one used in the GaN IC.

An oscilloscope used in the measurement was Lecroy HDO6054. Voltage was measured at the test points TP_G, D, S and R in Figs. 8 and 9. I_D was obtained from voltage drop in Rload. VH determines off state V_{DS} , and Rload



Fig. 12. 10 MHz switching waveforms of power HEMT at 100 V/4 A (conventional method vs. proposed method) obtained by measurement.



Fig. 13. 10 MHz switching waveforms of power HEMT at 100 V/10 A (conventional method vs. proposed method) obtained by measurement.

determines on-state $I_{\rm D}$ during the measurement.

3.2 Evaluation results and discussion

3.2.1 Switching waveforms

Fig. 12 shows 10 MHz switching waveforms measured by the proposed method (GaN-IC) and the conventional method (discrete implementation) at 100 V of VH, and R_{load} of 24.9 Ω . Fig. 13 shows the switching waveform at 100 V/10 A. Results reveal that the proposed GaN-IC achieves faster transitions than the conventional method. The highest slew rate of V_{DS} is 77.3 V/ns at turn-off and 45.2 V/ns at turn-on transition.

Undershoot and overshoot peaks appeared at transient in both the proposed and the conventional method due to voltage drop at parasitic inductance in the drain-source loop. The DUT had parasitic inductance of 0.4 nH at least for each drain and source terminal by bonding wires.

For V_{GS} waveform in the proposed method, 9 V of undershoot appeared at turn-off unexpectedly during experiments. There are two possible reasons for the noise. The first is that the GaN-IC has low resistance in the gate-source loop formed during off-state which makes convergence worse and results in high peak overshoot. Table II gives comparison of IEICE Electronics Express, Vol.VV, No.NN, 1-6

Table II. RL values in gate-source loop during off-state.

	U	1 0
	Conventional	Proposed
	(Discrete)	(Integration)
R	450 mΩ	280 mΩ
$L_{\rm p}$	8.5 nH	0.12 nH

Parameters	Typical value		Definition
w	-		Width per finger
$L_{\rm gd}$	-		Gate-drain distance
L_{gs}	0.75	μ m	Gate-source distance
$r_{\rm sh}$	500	Ω/sq	2-DEG sheet resistance
$v_{\rm xo}$	1.3×10^{5}	m/s	Source injection velocity
μ	0.1	$m^2/(V \cdot s)$	Low field mobility
SS	0.15	V/dec	Subthreshold voltage



Fig. 14. DC characteristics fitting results comparing with measurement results.

total RL values in the gate-source loop. However, it should also be noted that parasitic inductance in the gate-source loop is significantly reduced in the GaN-IC.

Another possible reason for noise output is that the connection to the oscilloscope creates an external parasitic loop. During the experiment, the oscilloscope is attached to the gate, source and drain terminals of the power HEMT via bonding wires, oscilloscope probes and cables. The external loop includes parasitic elements that can induce noise. Combining these hypotheses suggests that the noise originates in the external loop, and it remains at transient as high-peak undershoot because small resistance is not capable of suppressing the noise.

These hypotheses were verified by simulating the extraction of the equivalent circuit for the external loop. In the simulation, MVSG-HV (MIT Virtual Source GaNFET-High Voltage) compact model [25, 26, 27, 28, 29] was used as the GaN-HEMT model[30]. The parameters in MVSG-HV were calibrated based on experimental characterization results of discrete GaN-HEMTs fabricated by Interuniversity Microelectronics Centre, Belgium (Table III). DC characteristics of the HEMT model were evaluated by the Advanced Design System circuit simulator from Keysight. The DC characteristics obtained from the simulation correspond well with actual measurements (Fig. 14). The RMSPE (Root Mean Square Percentage Error) of I_D - V_{GS} characteristics was 13.0% in which V_{GS} is over threshold voltage.

Fig. 15 shows V_{GS} waveforms at turn-off transient obtained by simulation and measurement; the resonance frequency of ringing in the measurement result coincides with the one



Fig. 15. Comparison of V_{GS} waveforms during turn-off.



Fig. 16. I_D dependency of switching performance evaluated at 100 V of off-state V_{DS} .

in the simulation result considering oscilloscope loop. The difference of the convergence between measurement and simulation may be caused by process variation, accurancy of the HEMT model, and mismatches of the paraisitc elements between measurement and simulation.

3.2.2 Evaluation at various conditions

 $I_{\rm D}$ dependence of the switching characteristics was examined. The switching characteristics were measured at 100 V of off-state V_{DS} and one of various on-state I_D conditions: 1, 2, 4, 5 or 10 A. The results are shown in Fig. 16. Switching time t_{ON} and t_{OFF} are defined in Fig. 17. E_{HEMT} is energy loss in the power HEMT per switching cycle. The results show that the proposed GaN-IC improves switching speed and reduces energy loss under all condition. The superiority of the proposed method in t_{ON} , t_{OFF} and E_{HEMT} is particularly evident at high power conditions. Taking the evaluation results at off-state V_{DS} of 100 V and on-state I_D of 10 A for example, the proposed GaN-IC achieved 1.6 ns turn-off time and 3.4 ns turn-on time, which are 86% and 45% smaller than the discrete implementation respectively. Under these conditions, the fabricated GaN IC reduces energy loss E_{HEMT} by 52%. E_{HEMT} of the proposed method is 2.1 μ J/cycle compared to 4.4 μ J/cycle in the conventional discrete implementation.

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Fig. 17. Definition of switching time in switching waveforms.

4. Conclusion

This paper proposed a monolithic integrated circuit with a two-stage gate driver and a power HEMT for MHz-switching by p-gate GaN-on-QST technology. Fast and low energy loss switching of the GaN-IC was demonstrated in experiments at 100V and at various drain current conditions up to 10 A. Compared to conventional method using a discrete gate driver, the GaN-IC decreased switching time by 86% for turn-off and by 45% for turn-on, and energy loss in power HEMT by 52% at 100 V/ 10 A.

Acknowledgements

This research is supported by the Super Cluster program from Ministry of Education, Culture, Sports, Science and Technology and Consortium for GaN Research and Applications.

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