Degradation Caused by Negative Bias Temperature Instability Depending on Body Bias on NMOS or PMOS in 65 nm Bulk and Thin-BOX FDSOI Processes

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Abstract

Reverse Body Bias (RBB) control on Fully Depleted Silicon On Insulator (FDSOI) with thin Buried OXide (BOX) layer mitigates power consumption on the stand-by mode. However, Degradation caused by Negative Bias Temperature Instability (NBTI) is changed by RBB. We measure aging degradation of ring oscillators by applying RBB to NMOS or PMOS. In bulk, RBB to PMOS suppresses NBTI-induced degradation because increasing threshold voltage reduces carriers in channel. However, RBB to NMOS does not suppress NBTI-induced degradation because Positive BTI (PBTI) is not dominant in NMOS. In FDSOI, RBB to not only PMOS but also NMOS suppresses NBTI-induced degradation because BOX layer intercepts carriers to flow to substrate.

I. Introduction

In recent years, low power consumption is mandatory to reduce power density and to prolong battery life. Thin Buried OXide (BOX) Fully-Depleted Silicon On Insulator (FDSOI) is one possible candidate to operate in the low voltage of 0.4 V [1]. Reverse Body Bias (RBB) can reduce power consumption further more. However, degradation caused by Negativec Bias Temperature Instability (NBTI) is changed by RBB [2], [3]. NBTI causes aging degradation and become significant concern in nano-scaled devices [4]. The same amount of RBB is generally applied to NMOS and PMOS. However, it requires additional voltage source for RBB to NMOS. Our purpose is to optimize RBB voltage in NMOS and PMOS to suppress NBTI-induced degradation. We measure aging degradation of Ring Oscillators (ROs) by periodically counting the number of oscillation during stress conditions.

II. BTI-induced Degradation by RBB

Fig. 1 shows how to control body bias. N-well in PMOS and P-well in NMOS are connected to source terminals on the standard mode as shown in Fig. 1 (a). Fig. 1 (b) shows the RBB conditions. N-well and P-well are biased to positive and negative for source terminals of PMOS and NMOS respectively. Fig. 2 shows an example how to use RBB. RBB suppresses power consumption on the stand-by mode because threshold voltage (V_{th}) increases and leakage current decreases. Body bias cannot be controlled in SOI with conventional thick BOX. However, thin-BOX FDSOI can control the body bias as shown in Fig. 3 [1]. We evaluate BTI-induced degradation by changing RBB in bulk and thin-BOX FDSOI with 10 nm BOX layers. RBB suppresses aging degradations and V_{th} increases with time as voltage and temperature increase [4]. The atomistic trap-based BTI (ATB) model [5] is one of proposed theories of BTI as shown in Fig. 4. BTI occurs and V_{th} increases since defects in a gate oxide trap carriers as shown in Fig. 4 (a). The number of carriers in channel decreases by applying RBB as shown in Fig. 4 (b). Probability to trap carriers decreases because the number of carriers induced in the channel decreases. Therefore, it becomes harder to trap carriers to the defects as RBB increases. There are Negative BTI (NBTI) and Positive BTI (PBTI). NBTI occurs on PMOS when gate-source voltage is negative. Likewise, PBTI is observed in NMOS especially in technologies with high-k gate dielectrics [6].

III. Measurement Setup

We fabricated a chip including 11-stage ROs composed of NOR gates to dominate NBTI as shown in Fig. 5. PMOS of NORs are stressed by NBTI when ENB is high to stop oscillation. Fig. 6 shows our measurement flow. During frequency measurement, ENB becomes low only for 28 μs and RBB is restored to 0 V to oscillate in the same condition. RBB is applied while ROs stop oscillation for 50 s. ROs suffer from NBTI in the low-power mode. NBTI measurement condition is at 1.6 V power supply voltage and 120 °C temperature to accelerate NBTI-induced degradation. Fig. 7 shows the test chip fabricated in 65 nm bulk and thin-BOX FDSOI processes. Layout patterns are same in both processes.

IV. Measurement Results

Fig. 8 shows measurement results by the body bias. X-axis is stress time and Y-axis is degradation rate based on initial frequencies. Dots represent average of measurement data and curves are drawn by the fitting function along $S_{\mathrm{NBTI}}\log(t+1)$. S_{NBTI} is the fitting parameter indicating degradations caused by NBTI. This function comes from the ATB model since defects have a time constant distributed uniformly on the log scale from 10^{-9} s to 10^{9} s [7]. Fig. 8 (a) and (b) show the measurement results in bulk when RBB is applied to NMOS or PMOS. V_{BN} and V_{BP} are defined body bias of NMOS and PMOS respectively. Difference of degradation rate at 0 and 1 V of V_{BN} is only less than 0.05%. While in PMOS, degradation rate decreases by 38% when V_{BP} of 1 V is applied. NBTI-induced degradation is suppressed by applying V_{BP} in bulk because NBTI is more dominant than PBTI in 65 nm process. Fig. 8 (c) and (d) show the measurement results in FDSOI when V_{BN} or V_{BP} are applied. Degradation rate decreases as RBB increases in RBB of both MOSFETs. We assume oscillation frequencies increase because carriers are captured in channel by RBB. BOX layer intercepts carriers to flow to substrate. We also evaluate degradation factor S_{NBTI} from fitting functions. Fig. 9 (a) and (b) show S_{NBTI} in bulk by applying V_{BN} or V_{BP}. Fig. 9 (c) and (d) show those in FDSOI. S_{NBTI} are almost constant in any V_{BN} of bulk, which means NBTI is not suppressed by V_{BN} in bulk. Likewise, S_{NBTI} decreases by 40% at V_{BP} of 1 V. S_{NBTI} in FDSOI is about twice as large as that in bulk because V_{th} of FDSOI is lower than that of bulk. Electric field in the gate oxide is higher in lower V_{th} and aging degradation is accelerated. In FDSOI, S_{NBTI} decrease as RBB on both MOSFETs and are almost equivalent. Applying RBB on PMOS is enough to suppress NBTI-induced degradation without RBB on NMOS and negative voltage sources are not required.

V. Conclusion

We fabricated ring oscillators in 65 nm bulk and thin-BOX FDSOI processes and measured aging degradation applied RBB to NMOS or PMOS. RBB on NMOS cannot suppress degradation in bulk, while RBB on PMOS, the degradation is suppressed. The degradation factor decreases by 40% from 0 to 1 V of RBB on PMOS. In FDSOI, the degradation factor decreases by RBB on both NMOS and PMOS. Applying RBB to PMOS is enough to suppress NBTI-induced degradation.

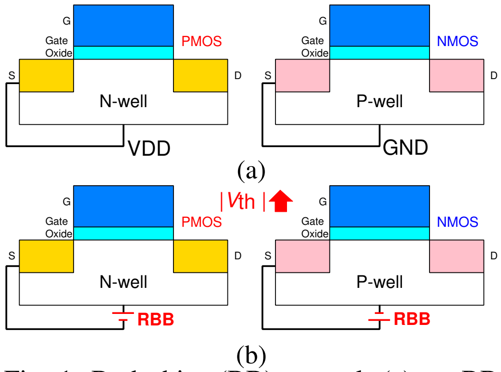


Fig. 1: Body bias (BB) control. (a) no BB and (b) reverse BB (RBB).

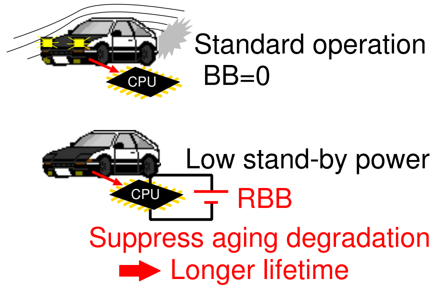


Fig. 2: RBB to suppress power consumption and aging degradation for chips on cars.

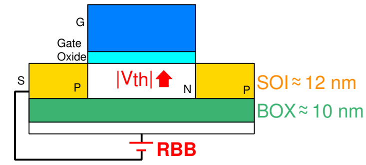


Fig. 3: Cross section of thin-BOX FDSOI on PMOS. It can control BB through 10 nm thin-BOX layers.

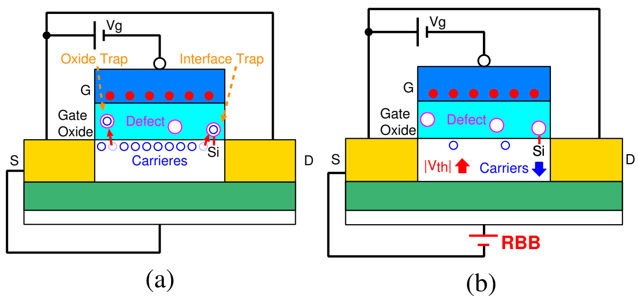


Fig. 4: BTI mechanism. (a) Atomistic trap-based BTI model. V_{th} increases when carriers are trapped. (b) Suppression of NBTI by RBB. V_{th} increases and the number of carries decrease.

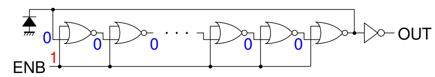


Fig. 5: 11-stage RO composed NOR gates.

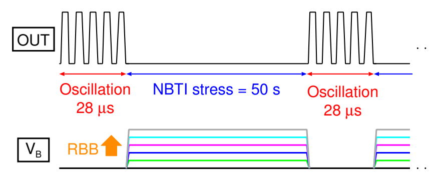


Fig. 6: Measurement flow.

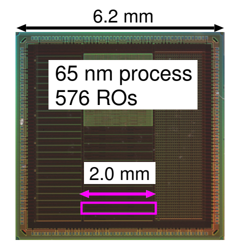
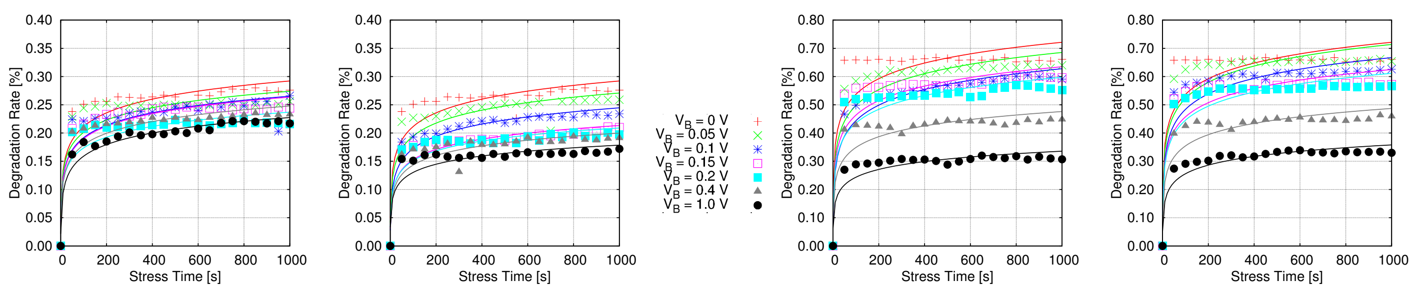
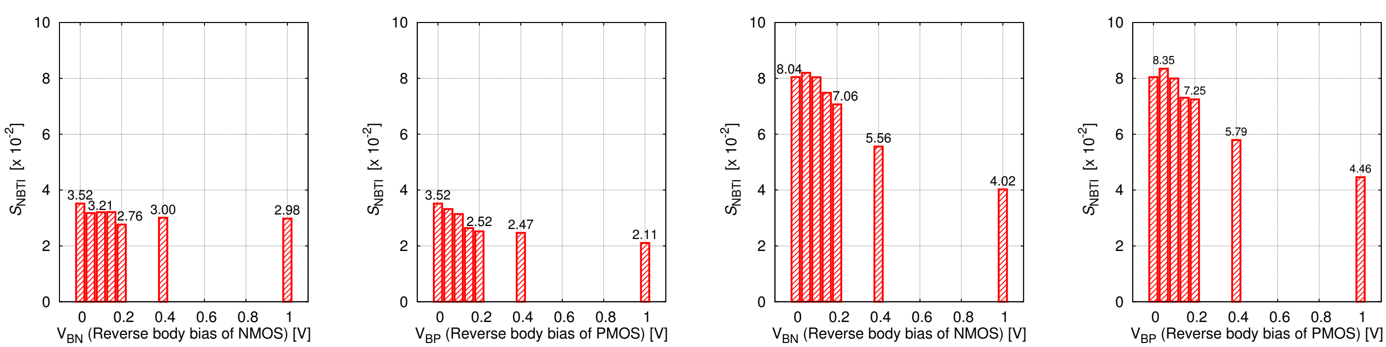


Fig. 7: Test chip.



(a) NMOS RBB in bulk. (b) PMOS RBB in bulk. (c) NMOS RBB in FDSOI. (d) PMOS RBB in FDSOI.

Fig. 8: Measurement results of NBTI.



(a) NMOS RBB in bulk. (b) PMOS RBB in bulk. (c) NMOS RBB in FDSOI. (d) PMOS RBB in FDSOI.

Fig. 9: Degradation factor S_{NBTI}.

Acknowledgments

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References

[1] R. Tsuchiya et al., *IEDM*, pp. 631-634, 2004.
[2] R. Kishida et al., *SSDM*, pp. 711-712, 2016.
[3] J. Franco et al., *IEDM*, pp 18.5.1-18.5.4, 2011.
[4] V. Huard et al., *IRPS*, pp. 289-300, 2008.
[5] H. Kukner et al., *IEEE Trans. on Dev. & Mat. Rel.*, pp. 182-193, 2014.
[6] S. Zafar et al., *VLSI Tech.*, pp. 23-25, 2006.
[7] B. Kaczer et al., *IRPS*, pp XT.3.1-XT.3.5, 2011.