The Impact of RTN-induced Temporal Performance Fluctuation against Static Performance Variation

Takashi Matsumoto[1], Kazutoshi Kobayashi[2] and Hidetoshi Onodera[3]
[1] VLSI Design and Education Center (VDEC), The University of Tokyo, Tokyo, Japan
[2] Department of Electronics, Kyoto Institute of Technology, Kyoto, Japan
[3] Department of Communications and Computer Engineering, Kyoto University, Kyoto, Japan
Phone: +81-3-5841-6764, Email: takashi.matsumoto@cad.t.u-tokyo.ac.jp

Abstract

Random telegraph noise (RTN) is one of major recent transistor reliability concerns in designing reliable systems. In a circuit that contains a large number of small transiostors, the impact of RTN-induced fluctuation is considered to increase when it is compared with the static frequency variation caused by manufacturing process. The impact of RTN on process variation is described based on our measurement results from 40 nm test chip.

1. Introduction

Physical feature size of transistors has been minimized continually over time. One of the dominant issues on realizing reliable systems is transistor performance variations. In this paper, we discuss the impact of Random Telegraph Noise (RTN) affecting transistor performance variations. It was predicted in the past that the impact of RTN-induced drain current fluctuation might exceed manufacturing process variation in 22 nm technology[1]. The horizontal axis in Fig. 1 is the drain current fluctuation in linear scale. The vertical axis is the normal quantile. The dotted line is a large MOSFET case and the solid line is a small MOSFET case. Process variation usually follows a normal distribution. RTN does not follow normal distribution and its distribution has a long-tail part. The impact of RTN dominates process variation at the cross point depicted as red circle in Fig. 1.

2. Test Structure for RTN measurement

Figure 2 shows the test structure for RTN measurement [2][3]. Combinational logic circuit delay is measured by ring oscillator (RO) oscillation frequency. The power supply for RO ($\mathrm{VDD_{RO}}$) and DFF ($\mathrm{VDD_{DFF}}$) can be independently supplied. All logic gates except NAND2 with EN input are homogeneous. RTN-induced delay fluctuation is measured by the RO frequency fluctuation. There are 840 same ROs on 2 mm^2 area and the statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at room temperature. Figure 2 also shows measurement result example of 7-stage RO oscillation frequency for about 80 s at $\mathrm{VDD_{RO}} = 0.65\mathrm{V}$. The transistor width of the inverter (INV) is smallest in this technology. Measurement results show the large step-like frequency fluctuation caused by RTN. Here, $F_{\max}$ is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation. $\Delta F/F_{\max}$ is a good reference for the impact of RTN-induced frequency fluctuation for logic delay.

3. Impact of RTN on Process Variation

It is confirmed in [3] that the distribution of $\Delta F/F_{\max}$ follows a log-normal distribution above 50% level in cumulative probability when data are collected over 15 chips (12,600 ROs) under 0.65 V operation. The distribution of RO frequencies ($F_{\max}$) for the same ensemble is confirmed to follow normal distribution as expectedt[3]. In a circuit with a large number of small transiostors, the impact of RTN-induced temporal fluctuation is considered to increase when it is compared with the static frequency variation caused by manufacturing process. Figure 3 shows ΔF versus $F_{\max}$ plot over 12,600 ROs. The vertical axis is plotted with log scale. Figure 4 shows $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs. It represents how the distribution of the impact of RTN correlates with process variation distribution. The triangle shape distribution suggests that there is no or weak correlation between RTN and process variations. Figure 5 can be obtained by plotting the vertical axis of Fig. 4 with log scale. The circle shape distribution suggests that there is no or weak correlation between the variation of the impact of RTN and process variation. Figure 6 shows the impact of RTN when it is compared with that of process variation. The impact of RTN on process variation is defined as

$$\frac{(\Delta F/F_{\max})_{\mathrm{n}\sigma}}{(\mathrm{n}\sigma/\mu)}. \tag{1}$$

The plot for the minimum size 7-stage RO at 0.65 V ($\times$) can be obtained as follows. $\Delta F/F_{\max}$ follows log-normal distribution. $(\Delta F/F_{\max})_{\mathrm{n}\sigma}$ can be obtained for each σ using the log-normal distribution. $F_{\max}$ follows normal distribution. $(\mathrm{n}\sigma/\mu)$ can be obtained for each σ using the normal distribution. The dotted line is estimated from measured distributions of both RTN and process variation when log-normal distribution for RTN is assumed up to 7σ value. For the minimum size 7-stage RO at 0.65 V ($\times$), the impact grows exponentially when σ is increased. It is found that RTN becomes comparable to process variation around 7σ value. When the operating voltage is slightly increased to 0.75 V ($\triangle, \circ$), the RTN impact decreases rapidly. Finally, when the transistor size is increased from the minimum to the standard size at 0.75 V, RTN has small (and almost constant) impact on process variation ($\circ$).

4. Conclusions

The impact of RTN on process variation with respect to CMOS combinational circuit is estimated by experimental data. Measurement data suggests that there is no or weak correlation between RTN variation and process variation. It is found that the impact of RTN can be drastically increased when supply voltage and gate area become low and small.

Acknowledgement

This work was supported in part by CREST, JST.

References

[1] N. Tega, *et al.*, IRPS2011, p.630.
[2] T. Matsumoto, *et al.*, IEDM2012, p.581.
[3] T. Matsumoto, *et al.*, CICC2014, Session 14-4.

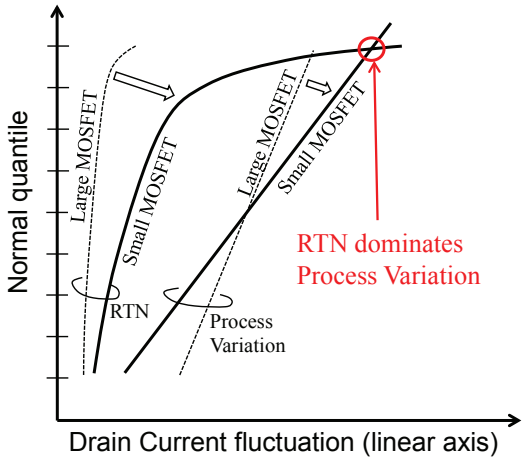

Figure 1: Conceptual figure of RTN vs Process Variation as for statistical distribution.

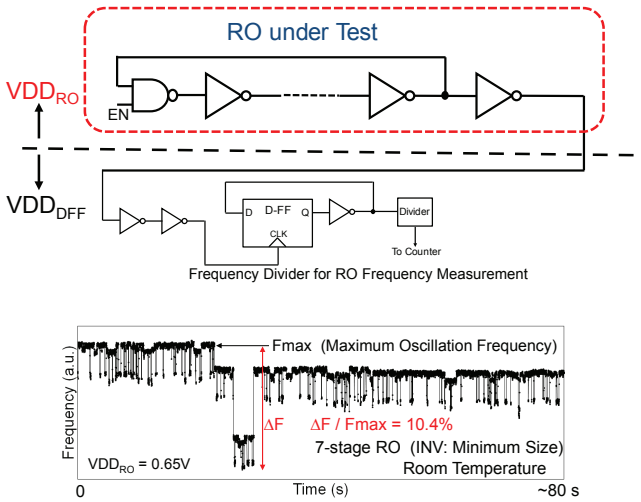

Figure 2: Test structure for RTN measurement. RO frequency fluctuation by RTN in one RO is also shown.

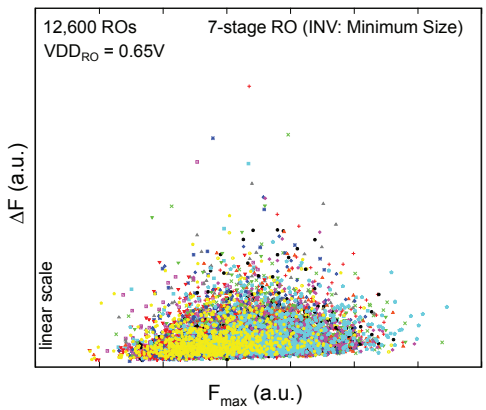

Figure 3: ΔF versus $F_{\max}$ plot over 12,600 ROs (vertical axis: log-scale).

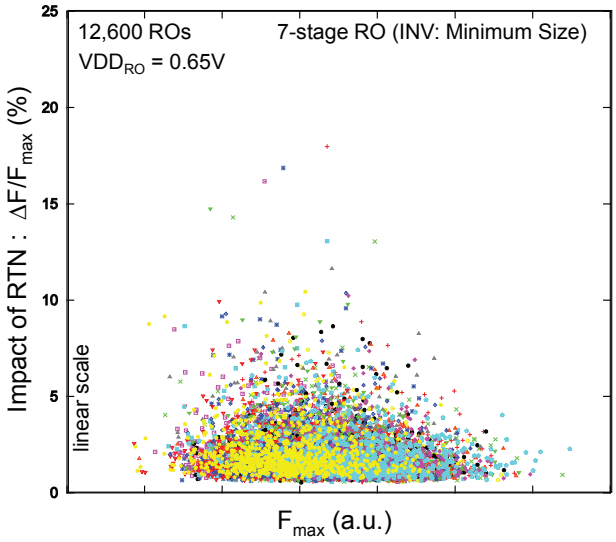

Figure 4: $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs.

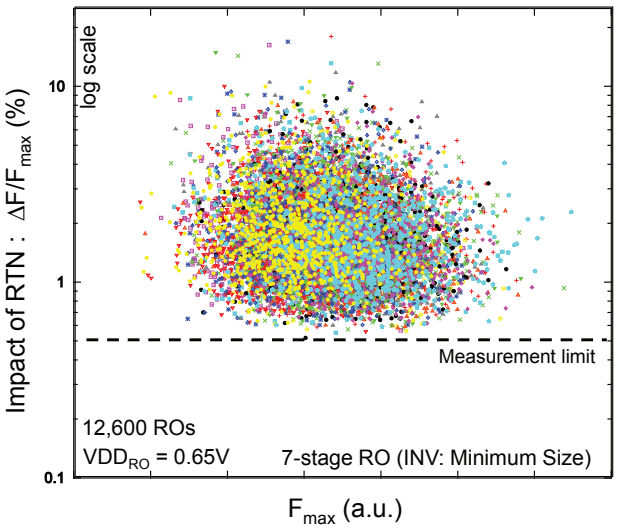

Figure 5: $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs (vertical axis: log-scale).

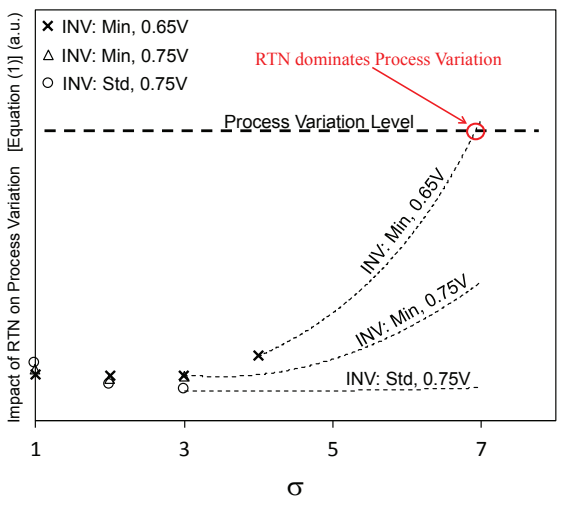

Figure 6: The impact of RTN on process variation.