Variability Characterization Using an RO-array Test Structure and Its Impact on Design

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***Abstract*—Real silicon variability characterization and modeling are important topics for statistical timing analysis. In this paper, we describe our RO-array test structures in 65nm process and measurement result of WID and D2D variations. We decompose and characterize WID variability into deterministic, systematic, and random components. We also discuss how these components affect circuit timing analysis.**

Keywords: Delay variability, Test structure, RO-array, WID variation, SSTA

I. Introduction

As technologies scaled down to deep sub-micrometer region, process variation becomes critical and significantly impacts on circuit performance. In the present and future process, the main causes of process variation such as RDF (Random Dopant Fluctuation), LER (Line Edge Roughness) are increasing, and these variations are observed as a random component [1]. Because these sources of variations are random, a probabilistic methodology is more accurate than a deterministic methodology. For accurate estimation of circuit path delay, many researchers pay attention to SSTA (Statistical Static Timing Analysis) as a timing analysis tool.

There are several techniques for SSTA to improve its accuracy [3][2], however it is not enough to guarantee SSTA accuracy because of the overall SSTA accuracy is fundamentally limited by variation models. Therefore, constructing accurate variation models are key challenge for SSTA[4][5].

In this paper, we describe our on-going effort for silicon variability characterization. Our objective is to develop a systematic method that can be applied for various fabrication process to extract accurate variability information required by statistical design methodologies. For this purpose, we have developed a design procedure for RO (Ring Oscillator)-array test structures and an analysis method for characterizing WID (Within Die) and D2D (Die to Die) variability. According to this design procedure, we designed and fabricated three types of test structures in 65nm process. We have decomposed the measured WID variability into three different components: deterministic, systematic, and random components. Random component is largest in all three processes at a single-gate level. Deterministic component, which is 15% of random component, exhibits little dependency on circuit structures and logic depth. Its therefore dominant for a circuit that has longer logic depth, and hence it should be properly factored in a timing margin. Additionally, inadequate extraction of deterministic component from WID variability affects the quality of random component. For this reason, extracting adequate deterministic component is necessary for constructing accurate variability model.

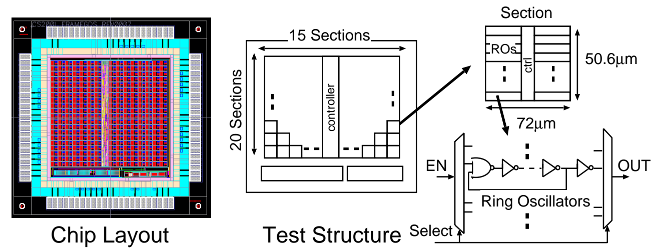

Fig. 1. 65nm RO-array test structure floor plan (c).

The remainder of this paper is organized as follows: Section II describes our design procedure for RO-array test structure which is applied for 65nm process. Section III first describes measurement result of WID and D2D variability, and decompose WID variability into three components. Then we discuss these impacts on circuit design. Section IV summarized this paper.

II. RO-test structure for variability characterization

To obtain real silicon variability information suitable for statistical timing analysis, we collect gate-level delay variability as a frequency variability of ROs. Fig. 1 shows the structure and layout of 65nm test structures [test structure (c)]. Other structures has one of the same structure and layout. In this design, we made 56 different types/stages of ROs and integrated into one "Section". The "Section" is arranged into sets of 7-by-20 and 8-by-20 arrays, therefore total 300 of each type of ROs are placed regularly. We can measure the WID spatial distribution of oscillation frequencies with an 79.2/64.8 μm resolution in the horizontal/vertical direction. In this test structure, only one RO is enabled to oscillate and measured its oscillation frequency. Therefore, this test structure provides accurate measurement result. In order to design effectively, we establish a design procedure to design similar test structures.

In this design procedure, we use manual design only for RO itself, and use automated synthesis and place & route for control logic from RTL netlist. Each "Section" has an identical layout including power and ground nets to reduce a layout dependence factor, and for design efficiency.

III. Variation analysis

A. WID vs D2D variability

In "test structure (a)", we have 384 identical ROs for each logic cell. Similarly, we have 270 ROs in "test structure (b)", and 300 ROs in "test structure (c)". These three test structures were fabricated in the same 65nm process, but in different lots.

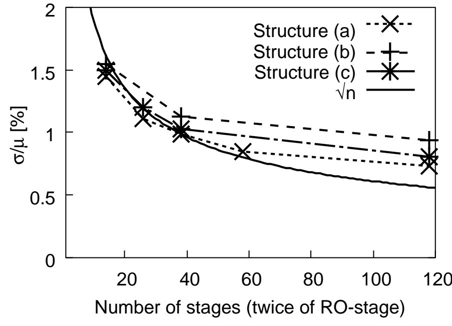

Fig. 2. WID variability at each circuit stages (twice of RO-stages). WID variability does not decrease as the circuit stage increase.

TABLE I
WID (AVERAGE) VS. D2D σ/μ [%]

	65nm (a)		65nm (b)		65nm (c)	
RO	WID	D2D	WID	D2D	WID	D2D
INV7	1.45	1.59	1.55	1.28	1.50	1.23
INV13	1.11	1.64	-	-	1.20	1.22
INV19	0.99	1.64	1.13	1.22	1.03	1.45
INV29	0.85	1.67	-	-	-	-
INV59	0.73	1.57	0.94	1.19	0.81	1.37

We have 20 chips for test structures (a) and (b), and 30 chips for (c). We have evaluated WID and D2D variability from ROs which are composed of 7, 13, 19, 29, 59-stage standard inverters.

Table I lists standard deviation of WID and D2D frequency variability of each RO. Listed value of WID variability is averaged value of each chip. The D2D variability in "test structure (a)" is around 1.6%, "structure (b)" is 1.2%, "structure (c)" is 1.3%, and it is almost constant in different stage ROs in the same test structures. The WID variability in the three test structures is around 1.5% in 7-stage RO.

As the number of stages increase, the WID variability decrease. However, the variability of longest stage RO such as 59-stage RO still measured as around 0.8%.

Fig. 2 shows the sigma of WID variation at each stages (twice of RO-stages). Fig. 2 shows WID variation does not decrease by $\sqrt{n}$ number of stages. This means WID variation is correlated each other, and we decompose WID variation into several components which will be explained in the next section.

B. WID variation decomposition and analysis

Measured WID variability includes some correlated component. With careful observation, we found that raw data has spatially correlated component. Therefore, we have decomposed WID variability into three different components: deterministic, systematic, and random components. The deterministic component represents location specific variability on a chip. The systematic component represents a gradual variation over a chip. The random component represent intrinsic random component on a chip. WID spatial distribution of 19-stage ROs in "test structure (b)", and these components are figured out in Fig.3. This variation decomposition process is described as below.

a) Deterministic component: This component has the same proportion of the total amount of variation at the same

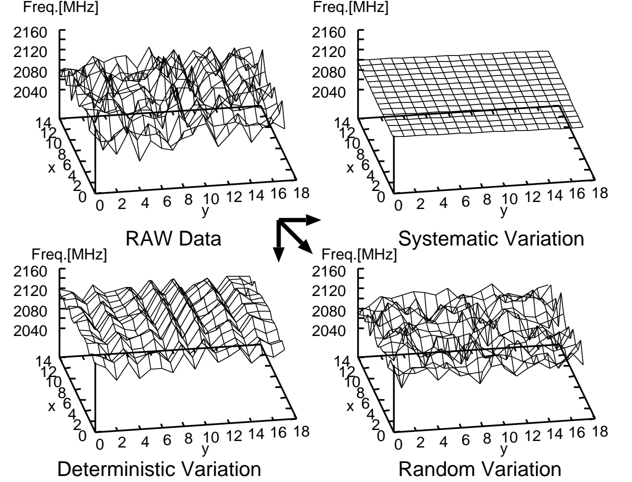

Fig. 3. WID variation decomposition (INV19 at structure (b)). Measured oscillation frequency (RAW) is decomposed into three component: deterministic, systematic and random component.

location on each chip. The upper left figure in Fig.3 shows an example of the spatial distribution of measured oscillation frequencies over a chip. We have measured 20 chips, and obtain chip-level oscillation frequency map for each chip. Also we obtain an average of frequencies from each chip, and total average frequency of all chips. Normalizing each chip-level oscillation frequency map with its chip-level average and total average, we make normalized oscillation frequency map averaged at each location on a chip. Then, we define this averaged oscillation frequency map as a location specific variation component "deterministic component", as shown in the bottom left figure in Fig.3. Model equation of deterministic component $d_{det}(x, y)$ is listd below.

$$d_{det}(x, y) = \sum^{i} d_i(x, y) \times \frac{\mu_{allchip}}{\mu_i}, \quad (1)$$

where the index i is chip number, $d_i(x, y)$ is oscillation frequency map of each chip, $\mu_{allchip}$ is the average frequency of all chips, and μ_i is average frequency of each chip. The main cause of this component may layout-dependent OPC residuals, mobility or IR-Drop variation.

b) Systematic component: This component represents a gradual variation over a chip. In this paper, "systematic component" is approximated as a linear function of circuit location of the residual component, as shown in the upper right figure in Fig.3. Model equation of systematic component $d_{sys,i}$ is listed below.

$$d_{sys,i}(x, y) = a_i x + b_i y + c_i, \quad (2)$$

where a_i, b_i are x-gradient and y-gradient, and c_i is z-intercept of systematic component. The main cause of this component may include defocus variation on lithography process, lens aberration, etc.

c) Random component: This component does not have any correlation with the location on the chip. This component originate from variations of V_{th} and L due to RDF and LER, so this component expects to follow a Gaussian distribution. This "random component" is given as the total residual component

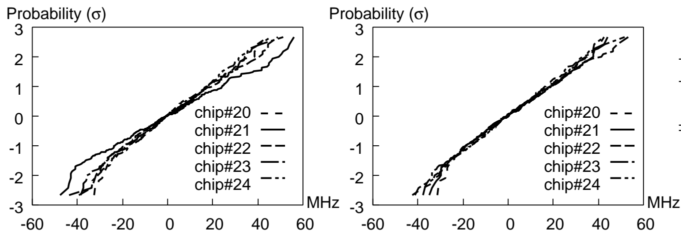

Fig. 4. CDF of INV19 chip#20-24 random component at structure (b). Left figure shows random component in chip#21 does not follows a Gaussian distribution. Right figure shows all random component follows a Gaussian distribution.

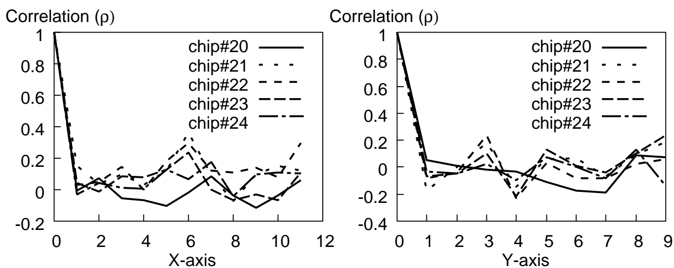

Fig. 5. Spatial autocorrelation coefficient of INV19 chip#20-24 random component at structure (b). The point x=6 in left figure, chip#21-23 still includes very weak correlation component in random component.

which eliminating deterministic and systematic component from raw data as shown in the bottom right part of Fig. 3. There are several strategies to extract the random component from raw data. In this case, we use a ratio of raw data and the deterministic component. Therefore, we adjust the deterministic component for each raw data using their ratio of averaged oscillation frequency, then subtract the adjusted deterministic component and the systematic component from a raw data. This residual represents the random component. Model equation of random component $d_{rand,i}$ is listed below.

$$d_{rand,i}(x,y) = d_i - d_{det} \times \frac{\mu_i}{\mu_{allchip}} - d_{sys,i}. \quad (3)$$

Note that extracting the deterministic component affects the result of the random component, therefore accurate extraction is needed. Experimental results are shown in Fig. 4. The left side of Fig. 4, shows CDF of random component which does not use a ratio of raw data and the deterministic component, which just subtracts the deterministic component from raw data. It is easy to understand CDF of chip#21 does not follow a Gaussian distribution. On the other hands, if we use a ratio of raw data and deterministic component, CDFs follow a Gaussian distribution as described in the right side of Fig. 4. However, on the left Fig.5, spatial autocorrelation coefficient of chip#21-23 shows very weak correlation in the random component. It shows that the random components still includes small residual of correlated component. If deterministic component is not correctly extracted from raw data, random component includes some resident of deterministic component. Therefore, accurate extraction of deterministic component is one of the key of accurate timing analysis.

Table II shows correlation coefficient of each raw data, and raw data without deterministic component. It is easy

TABLE II
WID correlation coefficient (Min - Max).

RO	65nm (a) RAW	65nm (a) RAW w/o Det.	65nm (b) RAW	65nm (b) RAW w/o Det.	65nm (c) RAW	65nm (c) RAW w/o Det.
INV7	0.02 - 0.22	0.00 - 0.2	0.14 - 0.4	0.01 - 0.14	0.11 - 0.33	0.00 - 0.15
INV13	0.03 - 0.33	0.03 - 0.25	-	-	0.26 - 0.46	0.00 - 0.15
INV19	0.07 - 0.39	0.09 - 0.31	0.34 - 0.61	0.01 - 0.24	0.28 - 0.94	0.01 - 0.18
INV29	0.10 - 0.43	0.02 - 0.29	-	-	-	-
INV59	0.15 - 0.61	0.29 - 0.45	0.46 - 0.76	0.01 - 0.38	0.56 - 0.73	0.00 - 0.22

TABLE III
WID variability decomposition σ/μ.

RO	65nm (a) Det.	65nm (a) Sys.	65nm (a) Rand.	65nm (b) Det.	65nm (b) Sys.	65nm (b) Rand.	65nm (c) Det.	65nm (c) Sys.	65nm (c) Rand.
INV7	0.59	0.15	1.32	0.82	0.15	1.30	0.74	0.14	1.30
INV13	0.52	0.14	0.96	-	-	-	0.71	0.12	0.95
INV19	0.52	0.12	0.83	0.76	0.14	0.81	0.66	0.13	0.77
INV29	0.49	0.11	0.69	-	-	-	-	-	-
INV59	0.48	0.12	0.53	0.74	0.14	0.56	0.66	0.11	0.45
INV			4			4			4

to understand each raw data has some correlation between each chip, especially long-stage ROs. On the other hand, after deterministic component is extracted from raw data, the correlation coefficient becomes small. This result shows WID variation includes some location specific component, and it affect the quality of random component.

Table III lists the decomposition result of three test structures. Fig.6 shows the sigma of three WID components. In all test structures, systematic component is very small and it has no dependence to stage-length. One reason might be expected that these test structures are small die, then inclined slope does not affect to the circuit performance. Deterministic component is smaller than random component. However, deterministic component has little stage-length dependence. In circuits with longer stage-length, deterministic component becomes comparable to random component. Therefore, deterministic component should be considered as a timing margin. From Table III, the amount of deterministic component is not so much different among test structures. It shows that a designer have to set timing margin carefully to guarantee the circuit. On the other hand, random variability decrease as the circuit stage-length increases due to averaging effect of random component. Using an equation to estimate the random variation in a single-stage[5], random component is extracted as 4% (σ/μ) in these

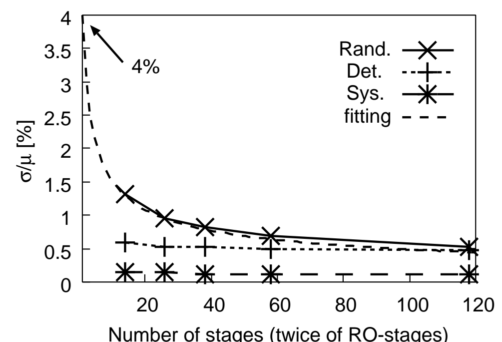

Fig. 6. Circuit stage dependence of D2D and WID three components (test structure (a)). Only random component depends on circuit stages, and is assumed as 4% at single stage.

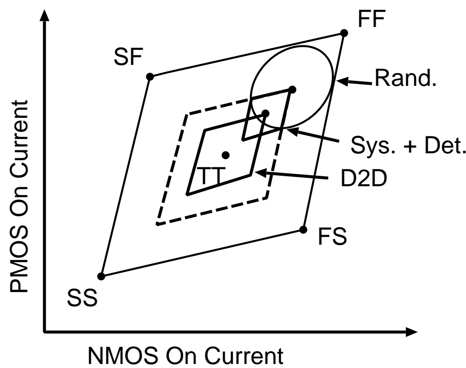

Fig. 7. Statistical design corner model. D2D, Systematic. and deterministic components compose a corners. Random components composes a Gaussian distribution around the corner

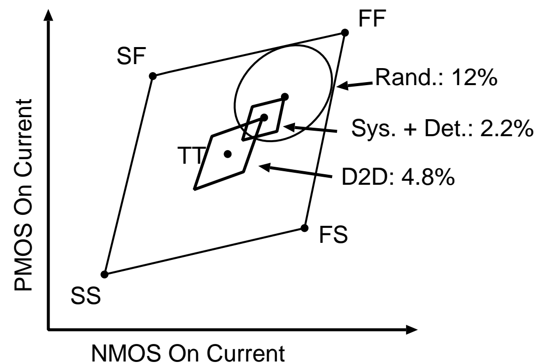

Fig. 8. Statistical Design Corner Model of Test Structure (a).

three test structures.

C. Variation characteristics and it impact on design

In this section, we want to discuss how WID variability affects to circuit design. As mentioned previously, only random component depends on circuit stage-length. Using this characteristics, we want to construct statistical path delay corner model under WID and D2D variability. The random component ideally follows a Gaussian distribution. D2D, systematic, and deterministic components may follows some kind of distribution. In this case, we set these components as a deterministic value. Using these characteristics, statistical design corner model is described as Fig. 7. In Fig. 7, only random component is identical and follows a Gaussian distributiion. However, D2D, systematic and deterministic components is some correlated distibutioin. In the corner model, systematic and deterministic components should be treated as a small corner around D2D variation corner. Therefore, systematic and deterministic component expands an area of design corners in long-stage circuit compared to ideal random variability. Statistical timing analysis with these components is required to guarantee the accuracy.

And then, we try to apply the real silicon variability to this statistical design corner model. From Tables I and III, we got real variability of D2D, deterministic, systematic, and random components. Usually design corner is described in $\pm 3\ \sigma$, therefore the values in the tables are tripled. Using the variability information from test structure (a), the statistical design corner model is shown in Fig. 8. In Fig. 8, D2D component, deterministic and systematic component, and random component are estimated as 4.8%, 2.2% and 12% in a single stage. This result shows the random component is dominant in this 65nm process. However, designer cannot ignore deterministic component in long-stage circuit path delay.

IV. Conclusion

In this paper, we explain our variability characterization for statistical timing analysis. We construct RO-array based test structures to measure real silicon variability, and measured D2D and WID variability in three test structures in 65nm process. We decompose WID variability into three different components: deterministic, systematic and random component. Random component is 4% in one stage in 65nm process, and its decrease as the total stage length increase. Systematic components is 0.11-0.15% in each stage. Deterministic components is 0.48-0.82 % in each stage, and it has small dependence on the stage length. In a large stage circuit, deterministic component is comparable to random component in total variability. Deterministic components should be considered in a statistical path delay analysis.

Acknowledgment

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