Zero-standby-power Nonvolatile Standard Cell Memory Using FiCC for IoT Processors with Intermittent Operations

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***Abstract*—A standard cell memory (SCM) is a memory constructed with standard cells and implemented by logic synthesis and automatic placement and routing, which enables stable operation in the low voltage region compared to an SRAM. In this paper, we show the measurement results of a nonvolatile SCM (NV-SCM) using a Fishbone-in-Cage Capacitor (FiCC), which is suitable for IoT processors with intermittent operations. The NV-SCM was fabricated in a 180 nm standard CMOS process technology. The area overhead from the nonvolatility of bit cells is 74%. We confirmed full functionality of the NV-SCM. In the normal read/write and the data restore operation, the NV-SCM can operate up to 21 MHz. The data retention time was 95 minutes when the write time to the nonvolatile memory was 0.3 seconds and the reading voltage was set to 1.4 V. The simulation results show that the proposed NV-SCM can reduce the energy consumption by 51.19% compared to a conventional volatile SCM when hybernation/normal operation time ratio is 500.**

***Index Terms*—SCM (Standard Cell Memory), Nonvolatile memory, Nonvolatile processor, IoT (Internet of Things), FiCC (Fishbone-in-Cage Capacitor)**

I. Introduction

In recent years, the Internet of Things (IoT), 5G, and other information and communication technologies have made significant progress [1], [2]. Mobile devices such as laptops and smartphones require lower power consumption and zero-standby-power of microprocessors and other components in order to extend their battery life [3].

One of the most effective ways to reduce the energy consumption of integrated circuits is to scale the power supply voltage. In reference [4], it was shown that scaling the supply voltage to near the transistor threshold voltage improved the energy efficiency of the processor by up to 4.7 times. However, in such a low voltage region, the performance variation of integrated circuits due to process variation becomes significant, and the malfunction of the integrated circuits becomes a problem [5], [6]. In integrated circuits, on chip memories, such as 6T SRAM, are vulnerable to process variations [7], [8], [9]. 6T SRAM is hard to operate in the low voltage region due to vulnerability to unbalance threshold voltage variations within a bit cell. A standard cell memory (SCM) has been proposed as an alternative to SRAM [10]. D-latches or D flip-flops are used in the bit cells, and the peripheral circuits are implemented using random logic. The circuit is implemented using only CMOS digital circuits, which enables stable operation in the ultra low voltage region. In reference [11], it is shown that 4-kbit SCM operates normally at a supply voltage of 350 mV.

One of the most effective ways to achieve zero-standby-power, the nonvolatile power gating (NV-PG) technique has been widely adopted to cut off static leakage power [12], [13]. NV-PG architecture using nonvolatile bistable circuits such as a nonvolatile SRAM (NV-SRAM) and a nonvolatile flip-flop (NV-FF). This architecture has two modes: normal operation mode and shutdown mode. In the normal operation mode, nonvolatile data retention is not used. Thus, the NV-SRAM and NV-FF circuits execute only the ordinary SRAM/FF operations in the normal operation mode. On the shutdown operation mode, shutdown of the circuit domains or systems with nonvolatile data retention is executed. In reference [14], a nonvolatile SCM (NV-SCM) is proposed by applying an MTJ (Magnetic Tunnel Junction) element to the conventional volatile SCM, but it cannot be fabricated in a conventional standard CMOS process technology. It is compatible with a CMOS process but additional masks and semiconductor manufacturing equipment are required.

In this paper, we describe the layout design and measurement of an NV-SCM [15] with a nonvolatile memory using FiCC (Fishbone-in-Cage Capacitor) [16], a sort of metal fringe capacitor. The NV-SCM can be fabricated in conventional CMOS process without any additional masks.

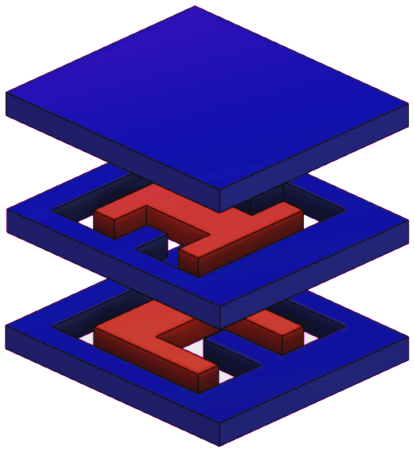

Fig. 1. 3D structure of FiCC

II. Nonvolatile Memory Using FiCC

A. FiCC

A metal fringe capacitor (MFC) [17] is a capacitor that consists only of metal wire segments and utilizes the capacitance between them. Among capacitors which can be configured on an ASIC (Application Specific Integrated Circuit), MFCs have the advantages of (1) needing no additional masks in a standard CMOS process and (2) having ideal linear characteristics. Thanks to the process technology scaling, smaller wire width and smaller distance between wires are allowed, which increases capacitance per area [18], [19]. However, since MFCs use fringe capacitance between metal wire segments, they are influenced by a crosstalk capacitance with neighboring wires and capacitors, and layout designers must consider them. In a previous study, a shielding metal wall was introduced for each capacitor to reduce the crosstalk capacitance at the cost of area overhead [20].

The FiCC (Fishbone-in-Cage Capacitor) [21] was proposed to address those issues. The FiCC is an MFC that consists of outer electrodes and inner electrodes. The 3D structure of the FiCC is shown in Fig. 1. The electrodes in blue and red are the outer-side and inner-side electrodes, respectively, and the electrodes of the same side are connected vertically through vias. By connecting a noise-sensitive net to the inner electrode and a low impedance net with a stable potential such as GND or VDD to the outer electrode, the former is shielded like a Faraday cage. This structure enables us to suppress the crosstalk capacitance between the inner terminal and other neighbor wires or capacitors to 1/10.

B. Nonvolatile Memory Using FiCC

Nonvolatile memory using FiCC is a CMOS-compatible memory element composed of a FiCC and an NMOS transistor, forming a circuit equivalent to the Floating Gate (FG) structure of a flash memory element. A nonvolatile memory using FiCC is shown in Fig. 2. The node that consists of the transistor's gate terminal and the FiCC's inner electrode is isolated from the outer by an insulator and acts as a floating gate. The write and erase operations of the nonvolatile memory are shown in Figs. 3 and 4, respectively. The write operation is performed by applying 5.0 V to the Control Gate (CG) to cause tunneling and trap electrons in the FG. The erase operation is performed by pulling electrons out of the FG by tunneling. By applying a write voltage of 5.0 V for 5 seconds to the CG of a nonvolatile memory using FiCC, the threshold voltage can be increased to 3.3 V, and the threshold voltage shift can be observed even after one day [16]. It is also shown that the memory characteristics do not change significantly after about 1,200 write and erase cycling. Using tunneling for write and erase operations saves energy consumption significantly compared to the MTJ memory.

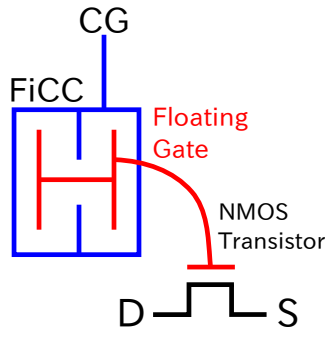

Fig. 2. Nonvolatile memory using FiCC

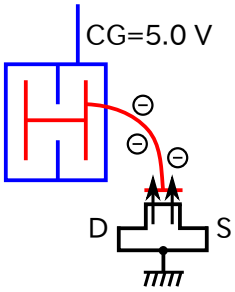

Fig. 3. Write operation

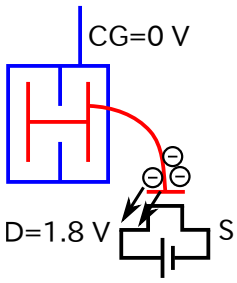

Fig. 4. Erase operation

III. D-latch for NV-SCM

The structure of the D-latch for the NV-SCM (1-bit NV-SCM) is shown in Fig. 5. The 1-bit NV-SCM consists of the conventional volatile D-latch and the nonvolatile part in red. The nonvolatile part consists of a nonvolatile memory using FiCC and three NMOS transistors. Because of the structure of the nonvolatile part, the nonvolatile memory using FiCC can be substituted for other nonvolatile memories.

The 1-bit NV-SCM has four operation modes: latch, store data to the nonvolatile part, restore data from the nonvolatile part to the volatile latch, and data erase operation. The applied voltages to CK, DG_W, DG_R, CG, SG, and SL terminals, excluding the data restore operation, are shown in TABLE I. During the latch operation, DG_W, DG_R, CG, SG, and SL are all set to 0 V. During the data store operation, DG_W=1.8 V, CG=5.0 V, CK=DG_R=SG=SL=0 V, and data is stored

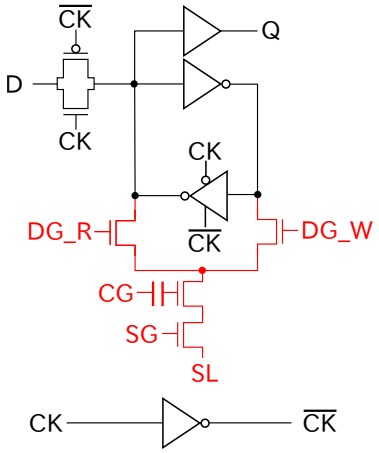

Fig. 5. 1-bit NV-SCM

TABLE I
OPERATION MODE OF NV-SCM

	CK	DG_W	DG_R	CG	SG	SL
Latch	-	0 V	0 V	0 V	0 V	0 V
Store	0 V	1.8 V	0 V	5.0 V	0 V	0 V
Erase	-	0 V	0 V	0 V	1.8 V	1.8 V

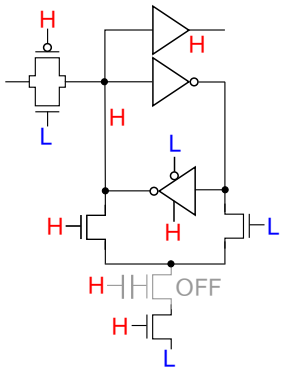

Fig. 6. Restore operation (programmed)

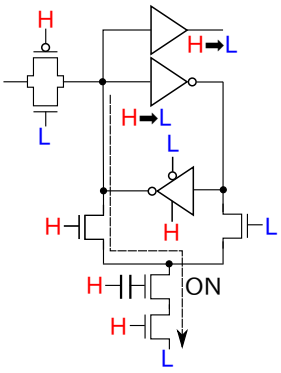

Fig. 7. Restore operation (nonprogrammed)

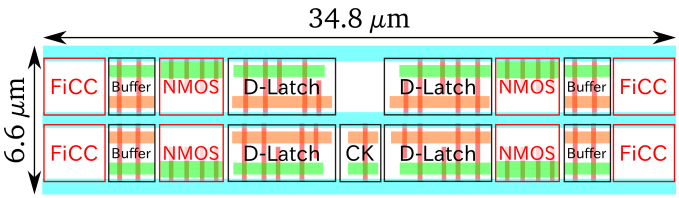

Fig. 8. Layout of the D-latch for the 4-bit NV-SCM

to the nonvolatile memory using the FiCC. The amount of increase in the threshold voltage of the nonvolatile memory cell (NMOS transistor with the FiCC) by the data store operation is determined by the holding value of the D-latch. During the data erase operation, data is erased from the nonvolatile memory using the FiCC with DG_W=DG_R=CG=0 V, SG=SL=1.8 V. In the data restore operation, the power is first turned on to the D-latch and then the D-latch stores 1 (high), followed by DG_R=CG=SG=1.8 V, CK=DG_W=SL=0 V. Thus, the time required for the data restore operation is only a few clock cycles. Figs. 6 and 7 show the behavior of the latch during the data restore operation when the threshold voltage of the nonvolatile memory cell is higher or lower than 1.8 V, respectively. When the threshold voltage of the nonvolatile memory cell is higher than 1.8 V, the NMOS transistor does not turn on even at CG=1.8 V and the latch retention value remains high. When the threshold voltage is lower than 1.8 V, the NMOS transistor turns on, the latch retention value changes from high to low. Thus, depending on the threshold voltage of the nonvolatile memory cell, the high or low data is restored to the latch.

IV. Layout Design and Measurement of NV-SCM

A. Layout Design of NV-SCM

We designed the layout of 4-bit and 16-word-8-bit NV-SCM using the 180 nm CMOS process. The layout of the D-latch for the 4-bit NV-SCM in Fig. 8 consists of four D-latches for NV-SCM described in section III. In the layout design of NV-SCM by logic synthesis and automatic placement and routing, the layout area of NV-SCM can be reduced by using the D-latch including 4-bit NV-SCM as bit cells. Since the clock signal is common, there is only one inverter for the clock in the whole cell. DG_W, DG_R, CG, SG, and SL are short-circuited in the cell. The layout design of the D-latch for the 4-bit NV-SCM resulted in a size of 229.68 μm^2 (34.8 μm $\times$ 6.6 μm), with an area overhead of 74% due to the nonvolatility of the bit cell. The 16-word-8-bit NV-SCM contains 16$\times$2 4-bit NV-SCMs. The layout size of the 16-word-8-bit NV-SCM is 0.0314 mm^2 (99.0 μm $\times$ 317.4 μm) as shown in Fig. 9. We also designed the layout of 16-word-8-bit conventional volatile SCM to compare its performance with NV-SCM. The layout size of the 16-word-8-bit SCM is 0.0232 mm^2 (85.8 μm $\times$ 270.0 μm).

B. Measurement of NV-SCM

We confirmed that the 4-bit NV-SCM (latch, store, restore, and erase operations) were fully functional. 4-bit NV-SCM can work up to 80 MHz in latch and restore operation when the supply voltage is 1.8 V. The relationship between the store (write) time and the data retention time of the nonvolatile memory is shown in Fig. 10. When the voltage applied to the CG during the data restore operation is 1.8 V, the data retention time saturates at around 0.3 seconds of the write time, and the data retention time is about 24 minutes. Based on this result, we changed the voltage applied to the CG during the restore operation to 1.4 V. In the case of 1.4 V, the data retention time also saturated at around 0.3 seconds of the write time, but the data retention time was extended to 95 minutes. This suggests that changing the voltage applied to the CG during the restore operation can shorten the time required to store (write) data to the nonvolatile memory using FiCC and extend its lifetime by suppressing the damage on the gate oxide of the NMOS transistor connected to the FiCC.

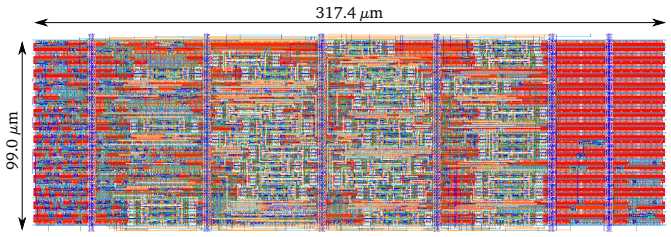

Fig. 9. Layout of 16-word-8-bit NV-SCM

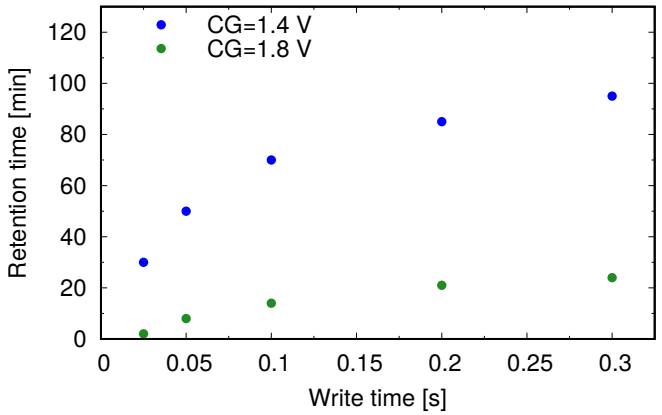

Fig. 10. Retention time of nonvolatile memory using FiCC

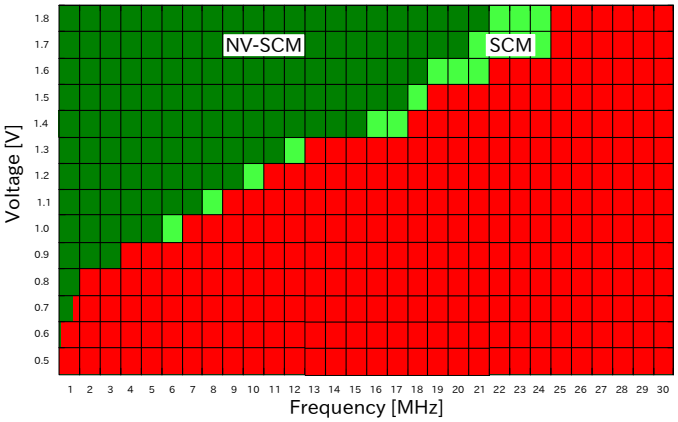

Fig. 11. Shmoo plot of the 16-word-8-bit SCM and NV-SCM

TABLE II
POWER CONSUMPTION OF 256-WORD-32-BIT SCM AND NV-SCM

	Normal operation	Standby operation
SCM	0.8060 mW	1.713 μW
NV-SCM	0.8115 mW	0

We confirmed that the 16-word-8-bit NV-SCM (latch, store, restore, and erase operations) were fully functional. The shmoo plot of the 16-word-8-bit SCM and NV-SCM is shown in Fig. 11. The areas shown in red and green indicate fail and pass, respectively. The SCM and NV-SCM can operate up to 24 MHz and 21 MHz, respectively when the supply voltage is 1.8 V. This result indicates that there is almost no effect on the operating speed due to the nonvolatile part in the NV-SCM. We measured the relationship between the store (write) time and the data retention time of the nonvolatile memory. The voltage applied to the CG during the data restore operation is 1.4 V. Compared with the 4-bit NV-SCM, the data retention time is different bit by bit. The main reason is that the voltage applied to the CG during the store and restore operations varies due to differences in the resistance and capacitance of wires connecting the CG.

V. COMPARISON OF ENERGY CONSUMPTION BETWEEN SCM AND NV-SCM

The relationship between the energy consumption of SCM and NV-SCM is shown in Fig. 12. Let $E_{\rm leak}$ denote the difference in energy consumption between SCM and NV-SCM during normal read and write operations. Since the NV-SCM can turn off the power in the standby operation, the energy consumption can be regarded as zero. Therefore, the NV-SCM can reduce the energy consumption of the SCM in the standby operation. Let $E_{\rm sb}$ be the energy consumption that the NV-SCM can reduce. Unlike the SCM, the NV-SCM completely turns off the power when it is in the standby operation. It consumes energy when it starts to operate again. Therefore, a standby time (BET : Break Even Time) is required to achieve $E_{\rm leak}$+$E_{\rm store}$+$E_{\rm restore} \leqq E_{\rm sb}$, where $E_{\rm store}$ and $E_{\rm restore}$ are the energy consumed during the data store and restore operations respectively. They can be regarded as zero since the time of store and restore operations are very short compared to the time of the normal read, write and standby operations.

In order to compare the energy consumption of SCM and NV-SCM, we performed simulations using one of fast SPICE simulators FineSim from Synopsys. The memory size is 256-word-32-bit, at 1.8 V, 27 °C, and 10 MHz. The power consumption of the 256-word-32-bit SCM and the NV-SCM are shown in TABLE II. In the normal operation, only one-word (32-bit) operates simultaneously, and the remaining 255-words (8160-bit) are in the standby operation. We derive the BET and the reduced energy. The difference in power consumption between the NV-SCM and the SCM during the normal operation is 5.5 μW. The power off time required per second of the normal operation time is 5.5 μJ/1.713 μW=3.211 s. With the normal operation time $t_{\rm op}$ as a variable, the BET is as shown in (1). The relationship between the ratio of standby/normal operation time and the reduced energy is shown in Fig. 13. At $t_{\rm sb}/t_{\rm op}$ = 500, the NV-SCM can reduce the energy consumption by 51.19% compared to the SCM.

$$BET = 3.211 \times t_{\rm op}. \quad (1)$$

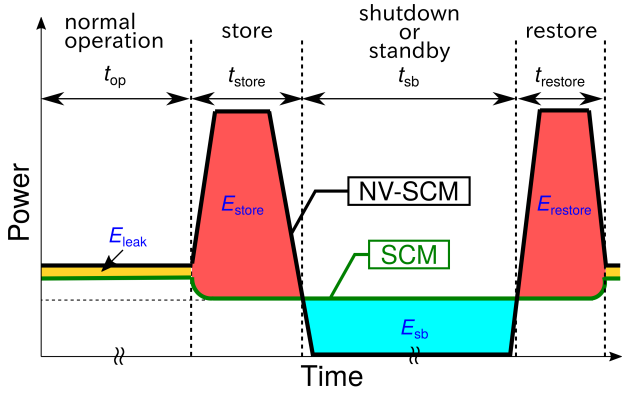

Fig. 12. Energy consumption diagram of SCM and NV-SCM

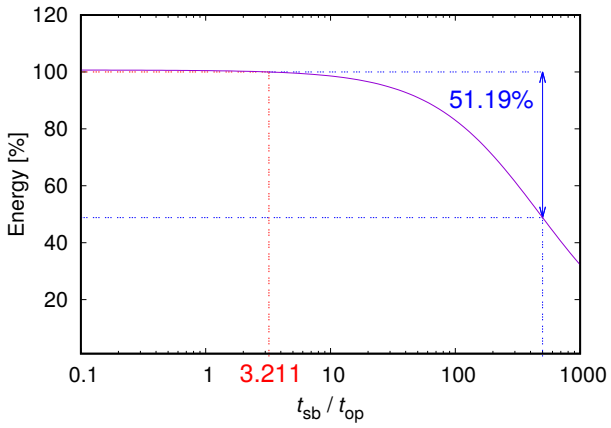

Fig. 13. Relationship between standby/normal operation time ratio and energy reduction

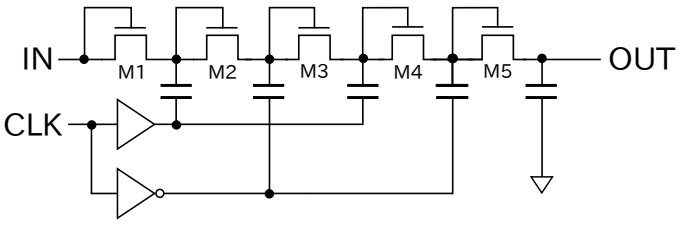

Fig. 14. 4-stage Dickson charge pump

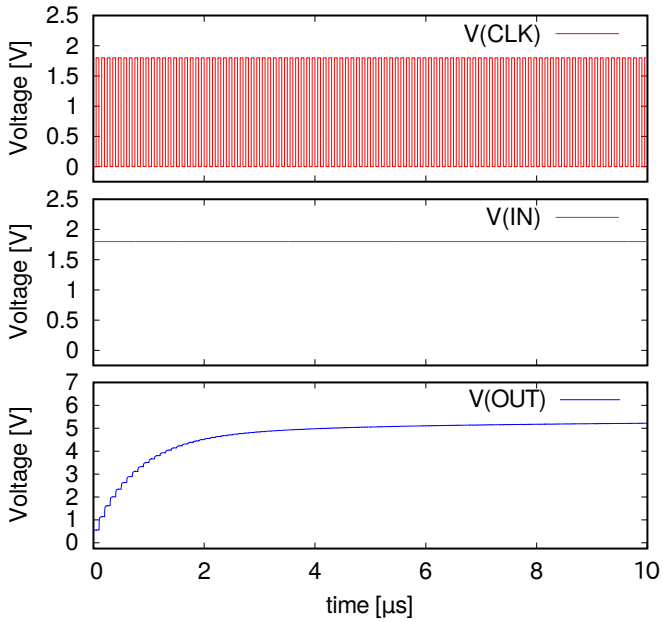

Fig. 15. Simulation results of 4-stage Dickson charge pump

VI. Supply Voltage Switching Circuit for CG Using Charge Pump

A. Dickson Charge Pump

In the NV-SCM, 5.0 V must be applied to the CG during the data store operation. However, since the power supply voltage used for other circuits is 1.8 V, a charge pump boosts the voltage from 1.8 V to 5.0 V.

The 4-stage Dickson charge pump [22] is shown in Fig. 14 composed of a smaller number of elements per stage than other charge pumps [23], [24]. This means that the layout area of the charge pump can be minimized. Through the NMOS switches (M1 to M5) whose drains and gates are diode-connected, charge is pushed out in only one direction by the complementary clock CLK whose amplitude is the supply voltage $V_{\rm dd}$. The charge is lifted by the operation of the clock signal and flows into the capacitor through the diode-connected NMOS transistor to boost each node. However, due to the voltage drop equal to the threshold voltage at each charge transfer NMOS switch, the output voltage of the 4-stage Dickson charge pump is expressed as $V_{\rm out} = 5\,(V_{\rm dd} - V_{\rm th})$.

The supply and input voltages were set to 1.8 V and the clock frequency was set to 10 MHz. The simulation results are shown in Fig. 15. It can be seen that the output voltage of the charge pump is boosted to around 5.0 V. The output drive current $I_{\rm out}$ can be calculated using (2) [25]. $C_{\rm Load}$ is the load capacitance, $V_{\rm out}$ is the output voltage of the charge pump and $T_{\rm ramp-up}$ is the time required by the charge pump to reach the output voltage. We derive $I_{\rm out}$ using the values from the simulation ($C_{\rm Load}$ = 100 fF, $V_{\rm out}$ = 5.0 V, $T_{\rm ramp-up}$ = 5 μs). From the above, we obtain I_{out} = 0.1 μA, which is over a few nA required to the writing operation to the nonvolatile memory using FiCC [16].

$$I_{\rm out} = C_{\rm Load} \times \frac{V_{\rm out}}{T_{\rm ramp-up}}. \tag{2}$$

B. Supply Voltage Switching Circuit for CG

In the NV-SCM, it is necessary to switch the voltage applied to CG from 0 V for the latch and erase operation, to 5.0 V for the store operation, and to 1.8 V for the restore operation. The supply voltage switching circuit for CG using charge pump is shown in Fig. 16. When supplying 0 V to CG, 1.8 V is applied to OUT_ZERO. When supplying 5.0 V to CG, 1.8 V is applied to IN_CP and CK_CP. When supplying 1.8 V to CG, 1.8 V is applied to IN_HIGH.

The supply voltage and input voltage were set to 1.8 V and the clock frequency was set to 10 MHz. The simulation

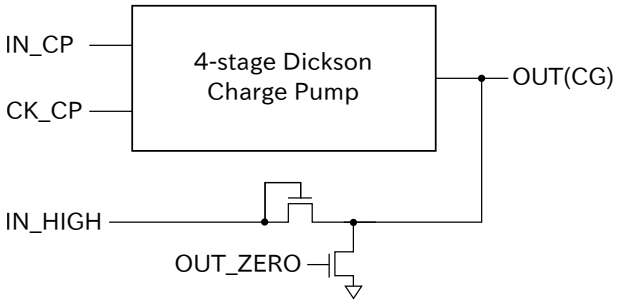

Fig. 16. Supply voltage switching circuit for CG

results show that the circuit structure shown in Fig. 16 can supply 5.0 V to CG. But in case of supplying 1.8 V to CG, actually the voltage supplied to CG is about 1.4 V due to the voltage drop in the diode-connected NMOS transistor. However, we confirmed that the data retention time of the nonvolatile memory using FiCC is extended by setting the voltage applied to CG to 1.4 V during the data restore operation in the measurement of NV-SCM as described in section Ⅳ.B.

VII. Conclusion

In this paper, we show the measurement results of an NV-SCM using FiCC suitable for IoT processors with intermittent operations. We designed the layout of the NV-SCM using the 180 nm CMOS process. The area overhead due to the nonvolatility of bit cells is 74%. Through measurements, we confirmed full functionality of the NV-SCM. In the normal read/write and the restore operation, the NV-SCM can operate up to 21 MHz. The data retention time was around 95 minutes when the write time to the nonvolatile memory is 0.3 sec. and the voltage applied to the CG is 1.4 V during the restore operation. The proposed NV-SCM can reduce the energy consumption by 51.19% compared to a conventional volatile SCM when hybernation/normal operation time ratio is 500 as shown in the simulation.

Acknowledgment

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References

[1] K. Shafique, B. A. Khawaja, F. Sabir, S. Qazi, and M. Mustaqim, "Internet of things (IoT) for next-generation smart systems: A review of current challenges, future trends and prospects for emerging 5G-IoT scenarios," *IEEE Access*, vol. 8, pp. 23 022–23 040, 2020.

[2] L. Chettri and R. Bera, "A Comprehensive Survey on Internet of Things (IoT) Toward 5G Wireless Systems," *IEEE Internet of Things Journal*, vol. 7, no. 1, pp. 16–32, 2020.

[3] K. Ishibashi, "Latest Developments on Low Voltage and Low Power LSI Technology," *IEICE Transactions on Electronics*, vol. 97, no. 1, pp. 9–16, 2014 (In Japanese).

[4] S. Jain, S. Khare, S. Yada, V. Ambili, P. Salihundam, S. Ramani, S. Muthukumar, M. Srinivasan, A. Kumar, S. K. Gb *et al.*, "A 280 mV-to-1.2 V wide-operating-range IA-32 processor in 32 nm CMOS," in *2012 IEEE International Solid-State Circuits Conference*. , IEEE, 2012, pp. 66–68,.

[5] N. Mehta and B. Amrutur, "Dynamic supply and threshold voltage scaling for CMOS digital circuits using in-situ power monitor," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 20, no. 5, pp. 892–901, 2011.

[6] S. Saxena, C. Hess, H. Karbasi, A. Rossoni, S. Tonello, P. McNamara, S. Lucherini, S. Minehane, C. Dolainsky, and M. Quarantelli, "Variation in transistor performance and leakage in nanometer-scale technologies," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 131–144, 2007.

[7] J. Chen, L. T. Clark, and T.-H. Chen, "An ultra-low-power memory with a subthreshold power supply voltage," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 10, pp. 2344–2353, 2006.

[8] G. Chen, D. Sylvester, D. Blaauw, and T. Mudge, "Yield-driven near-threshold SRAM design," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 18, no. 11, pp. 1590–1598, 2009.

[9] M. Qazi, M. Sinangil, and A. Chandrakasan, "Challenges and directions for low-voltage SRAM," *IEEE design & test of computers*, vol. 28, no. 1, pp. 32–43, 2010.

[10] P. Meinerzhagen, C. Roth, and A. Burg, "Towards generic low-power area-efficient standard cell based memory architectures," in *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*. , IEEE, 2010, pp. 129–132,.

[11] O. Andersson, B. Mohammadi, P. Meinerzhagen, A. Burg, and J. N. Rodrigues, "Dual-VT 4kb sub-VT memories with $<$1 pW/bit leakage in 65 nm CMOS," in *2013 Proceedings of the ESSCIRC (ESSCIRC)*. , IEEE, 2013, pp. 197–200,.

[12] S. Sugahara *et al.*, "Nonvolatile Static Random Access Memory (NV-SRAM) Using Magnetic Tunnel Junctions with Current-Induced Magnetization Switching Architecture," *JJAP*, 2008.

[13] Y. Shuto, S. Yamamoto, and S. Sugahara, "Comparative study of power-gating architectures for nonvolatile FinFET-SRAM using spintronics-based retention technology," in *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2015, pp. 866–871.

[14] J. Akaike, M. Kudo, and K. Usami, "Design and Evaluation of MTJ-based Standard Cell Memory," *IEICE Technical Report; IEICE Tech. Rep.*, vol. 116, no. 94, pp. 103–108, 2016.

[15] Y. Abe, K. Kobayashi, J. Shiomi, and H. Ochi, "Nonvolatile Standard Cell Memory Using FiCC for IoT Processors with Intermittent Operations," *Design Automation Symposium*, pp. 3–8, 2021 (In Japanese).

[16] I. Tanaka, N. Miyagawa, T. Kimura, T. Imagawa, and H. Ochi, "Thereshold-voltage Measurement of CMOS-compatible Non-volatile Memory Element using FiCC and Consideration on its Read-out Method," *Design Automation Symposium*, pp. 9–14, 2019 (In Japanese).

[17] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 384–393, 2002.

[18] A. Matsuzawa, "Analog and RF circuits design and future devices interaction," in *2012 International Electron Devices Meeting*. , IEEE, 2012, pp. 14.3.1–14.3.4,.

[19] Q. S. Lim, A. V. Kordesch, and R. A. Keating, "Performance comparison of MIM capacitors and metal finger capacitors for analog and RF applications," in *2004 RF and Microwave Conference (IEEE Cat. No. 04EX924)*. , IEEE, 2004, pp. 85–89,.

[20] D. Sandstrom, M. Varonen, M. Karkkainen, and K. A. Halonen, "W-band CMOS amplifiers achieving $+$10 dBm saturated output power and 7.5 dB NF," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3403–3409, 2009.

[21] N. Miyagawa, T. Kimura, and H. Ochi, "FiCC: Crosstalk Noise Hardened Metal Fringe Capacitor for High Integration," *IEICE Technical Report; IEICE Tech. Rep.*, vol. 116, no. 478, pp. 43–47, 2017 (In Japanese).

[22] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of solid-state circuits*, vol. 11, no. 3, pp. 374–378, 1976.

[23] N. Yan and H. Min, "A high efficiency all-PMOS charge pump for low-voltage operations," in *2005 IEEE Asian Solid-State Circuits Conference*. IEEE, 2005, pp. 361–364.

[24] H. Peng, N. Tang, Y. Yang, and D. Heo, "CMOS startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1618–1628, 2014.

[25] L. F. Rahman, M. Marufuzzaman, L. Alam, and M. B. Mokhtar, "Design Topologies of a CMOS Charge Pump Circuit for Low Power Applications," *Electronics*, vol. 10, no. 6, p. 676, 2021.