Nonvolatile SRAM Using Fishbone-in-Cage Capacitor in a 180 nm Standard CMOS Process for Zero-standby and Instant-powerup Embedded Memory on IoT.

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Abstract

In this paper, we propose a nonvolatile SRAM (NVSRAM) using the Fishbone-in-Cage Capacitor (FiCC) fabricated in a 0.18μm CMOS process technology. The FiCC can be implemented with metal wires as same as a metal-insulator-metal (MIM) capacitor that can be fabricated with a standard CMOS process technology. Three transistors and an FiCC are added to a conventional 6-transistor SRAM for non-volatile operations with 42% area overheads. Assuming 5 minutes active time per hour, the proposed NVSRAM can reduce 61.8% of power consumption compared with a standard SRAM. The fabricated NVSRAM can operate correctly as an SRAM at 100 MHz and perform nonvolatile store and restore operations by using the FiCC.

Key words: SRAM, Nonvolatile memory, FiCC memory, Nonvolatile SRAM, IoT, Zero standby power, FN tunneling

1 Introduction

Internet of Things (IoT) are currently spread out in many fields. Some applications for an IoT request intermittent operations. Between intermittent operation periods, an IoT just consumes battery by leakage power. The hibernation mode makes it possible to achieve zero-standby power but an off-chip nonvolatile memory must be used for ASICs fabricated in a standard CMOS process. Store and restore operations between an ASIC and an off-chip nonvolatile memory consume power. Thus it is not adequate to short standby time. On-chip nonvolatile memories are highly-demanded for IoTs working at short intermittent period[1]. In this paper, we propose a nonvolatile SRAM (NVSRAM) using the Fishbone-in-Cage Capacitor (FiCC)[2][3]. Many embedded nonvolatile memories were proposed such as SONOS flash memory and MTJ that cannot be fabricated in a standard CMOS process[4][5]. They are compatible with a CMOS process but additional masks and semiconductor manufacturing equipments are required. On the other hands, the FiCC can be implemented as same as a metal-insulator-metal (MIM) capacitor without any additional mask.

2 Nonvolatile SRAM Cell Using an FiCC

A 3D structure of the FiCC is shown in Fig. 1. It consists of outer and inner electrodes. The outer net shields the inner net as a floating gate. An operating principle of the FiCC is shown in Fig. 2. During the write (store) operation, a high voltage around 5 V is applied to CG, then electrons go up to the inner terminal by FN tunneling. During the erase operation, CG is pulled down to ground and a standard voltage around 1.8 V is applied to the source terminal. Then electrons are also removed by the FN tunneling. Fig. 3 shows the retention time of the FiCC. FiCC can hold enough charge over one hour after a 200 ms store operation. The erase operation takes one second.

We designed and fabricated a 64 bit nonvolatile SRAM macro with the FiCC in a 180 nm CMOS process. Figures 4-7 show the schematic and the layout of the NVSRAM. The area of the NVSRAM is 42% larger than that of the standard SRAM. The shape of FiCC is optimized to reduce the area overhead. The FiCC is implemented by two metal layers above the M3 layer that can be stacked over the SRAM cell.

There is no area overhead from the FiCC whose area is within the area of the 9T SRAM cell. This structure can be applied to an NVSRAM using other non-volatile memories, and can reduce area overhead by stacking nonvolatile memory cells.

The reliability of the FiCC was measured by repeating the store and erase operations. Fig. 8 shows the threshold voltage after repeating the cycle consisting of a 5-second store operation and a 100-second erase operation. After 1,200 cycles, the threshold voltage stays almost constant[3]. We consider the 1,200 cycles of the 5-second store operation are as stressful as 30,000 cycles of the 200 ms store operation.

The FiCC is attached to the gate terminal CG on the middle of the three additional NMOS transistor as shown in Fig 4. The 12T nonvolatile SRAM cell using SONOS in [4],while the proposed structure has 9 transistors. The split power supplies (VDDB and VDDT) enable the restore operation by using only the 3 additional transistors. Table 1 shows voltage maps of the additional signals of the NVSRAM on read and write operation as a standard SRAM and store, erase and restore operations as a nonvolatile memory. On the restore operation, VDDB goes up before VDDT as shown in Fig. 9. Then the node NB always becomes high. After that, CG, DG and SG are enabled. When the FiCC is programmed, the threshold voltage of the middle transistor becomes higher than standard supply voltage. Therefore NB is pulled down only in the nonprogrammed SRAM cells. At the store operation, the FiCC in the SRAM whose NB is low is programmed. At the restore operation the restored value of the programmed SRAM cell stays high. It means that the opposite data are always restored. This disadvantage can be recovered by adding a nonvolatile SRAM cell that holds the polarity of stored data in a SRAM macro. The input and output data of the SRAM macro can be inverted by XOR gates when its stored data are reversed.

3 Power Consumption

Power consumption at 100 MHz during the read and write operations and standby are estimated by using circuit-level simulations. Supply voltage is 1.8 V and ambient temperature is 27°C. Simulation results are shown in Table 2. Assuming that read and write operations are equally executed for 512 bit out of 1 Mbit at 100 MHz, power consumption of the NVSRAM and the standard SRAM becomes 271 μW and 259 μW respectively.

Break Even Time (BET) is used to estimate the effectiveness of power down by the FiCC, that means the time when power consumption of SRAM and NVSRAM becomes equal [6]. Relationship between the power consumption of SRAM and NVSRAM is shown in Fig. 10. NVSRAM consumes slightly more power than SRAM during read and write operations, but consumes no power while power is off. Longer standby time means less power consumption. BET (t_{BET}) is expressed by Eq. (1) using t_{op} (active time), ΔP_{op} (the difference of power consumption between NVSRAM and SRAM), and P_{sb} (power consumption of SRAM during standby time)

$$t_{\mathrm{BET}} = t_{\mathrm{op}} \times \Delta P_{\mathrm{op}} / P_{\mathrm{sb}} = 0.293 t_{\mathrm{op}} (@100\mathrm{MHz}) \quad (1)$$

In Fig. 11, E_{save} (energy consumption of SRAM during store operation) and E_{res} (energy consumption of SRAM during restore operation) are regarded as zero because t_{st} and t_{res} are much shorter than t_{op} and t_{sb}. Fig. 11 shows power reduction according to the ratio of t_{op} and t_{sb}. NVSRAM can reduce power consumption when standby time is longer than 29.3% of active time. When active time is 5 minutes standby time must be longer than 90 seconds.

4 Conclusion

We propose the NVSRAM by using the FiCC that can be fabricated by a standard CMOS process without any additional mask. The proposed NVSRAM can be applied to an IoT that operates intermittently enbling zero standby power. The area overhead of the NVSRAM is 42% in the 180 nm process. The fabricated 64 bit SRAM macro works at 100 MHz and 200 ms store operation to FiCC enables retention time over an hour. Assuming 5 minutes active per hour, the NVSARM can reduce power consumption by 61.8%.

References

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Table 1: Voltage map of additional control signals

operation	DG	CG	SG	SL
read and write	0 V	0 V	0 V	0 V
FiCC store	1.8 V	5 V	0 V	0 V
FiCC erase	0 V	0 V	1.8 V	1.8 V
FiCC restore	1.8 V	1.8 V	1.8 V	0 V

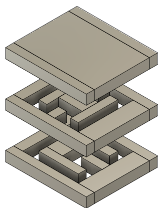

Figure 1: 3D Structure of FiCC[3]

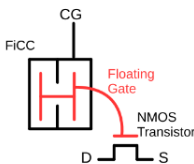

Figure 2: Nonvolatile memory using FiCC[3]

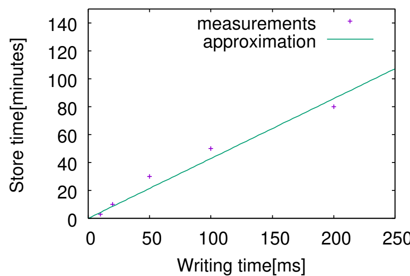

Figure 3: FiCC retention time

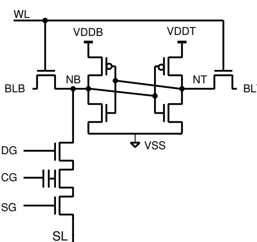

Figure 4: NVSRAM schematic

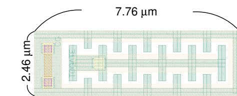

Figure 5: FiCC layout

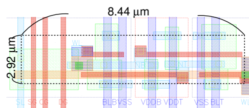

Figure 6: NVSRAM 1bit layout

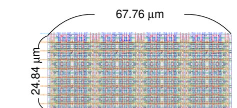

Figure 7: NVSRAM macro (8x8) layout

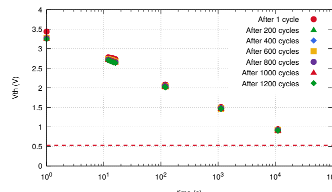

Figure 8: Threshold voltage reduction after repeating the cycle of store and erase operations[3]

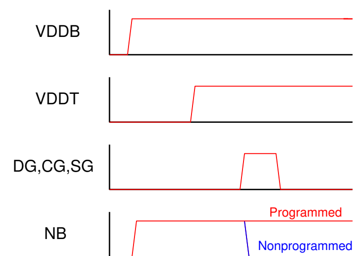

Figure 9: Timing chart of restore operation

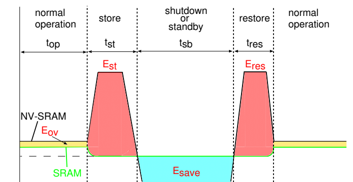

Figure 10: Power consumption diagram of SRAM and NVSRAM

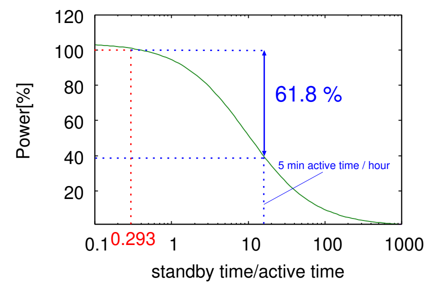

Figure 11: Power Reduction according to standby time.

Table 2: Power Consumption (read-/write at 100 MHz)

	read/write[μW]	standby[μW]
SRAM	259	41.0
NVSRAM	271	0