A Flip-Flop with High Soft-error Tolerance and Small Power and Delay Overheads

Kodai Yamada, Haruki Maruoka, Jun Furuta and Kazutoshi Kobayashi
Kyoto Institute of Technology, Kyoto, Japan
Phone, Fax +81-75-724-7410, E-mail kyamada@vlsi.es.kit.ac.jp

I. Introduction

According to process scaling, soft errors become a significant issue to threaten the reliability of a semiconductor chip since a stored value in strage elements such as flip-flops or SRAMs is flipped. To improve the tolerance of FFs against soft errors, several redundant FFs such as Triple Modular Redundancy (TMR) [1] have been proposed for effective countermeasures. However, they have longer delay time and larger area, power consumption than conventional FFs. Fully Depleted Silicon on Insulator processes (FDSOI) have higher tolerance for soft errors than a conventional bulk process without any performance overhead, because BOX layers prevent charge from being collected from substrate [2]. In this paper, we propose a flip-flop with high soft-error tolerance and small power and delay overheads in a 65 nm FDSOI process.

II. Radiation-Hardened Flip-Flops

Fig. 1 shows a conventional DFF called the Transmission Gate Flip-Flop (TGFF). It has no tolerance against soft errors. Fig. 2 depicts the Adaptive Coupling FF (ACFF) [3]. It has lower power consumption than the TGFF, because it has no local clock buffer. The ACFF has AC elements, in which PMOS and NMOS transistors are connected in parallel to overwrite a stored value of Master Latch (ML) easily. But they prolong delay time, while they suppress a Single Event Transient (SET) pulse [4]. NMOS pass transistors suppress a SET pulse from NMOS transistors, while PMOS pass transistors suppress a SET from PMOS transistors. However, to prevent the ACFF from upsetting, Slave latch (SL) must be strong against soft errors.

A. Conventional Radiation Hardened Flip-Flop

Fig. 3 shows the stacked FF [5]. It has the inverters composed of two NMOS and PMOS transistors. Unless both of NMOS transistors upset at the same time, it does not flip. However, it has bigger area and delay time overheads than the TGFF.

B. Proposed Radiation-Hardened Flip-Flop

In Fig. 4, the proposed FF named Pulse Blocking Low Dynamic Power FF (PBLDP FF) is shown. It is proposed based on the ACFF with high soft-error tolerance and short delay time and small area overheads. NMOS transistors are weaker against soft errors than PMOS transistors due to the difference of mobility[6]. ML of the PBLDP FF has only PMOS pass transistors to suppress soft errors from NMOS transistors. The PMOS pass transistors have a shorter delay time overhead than AC elements because they are always ON-state. SL is composed of stacked inverters. They do not influence delay time because ML is directly connected to the output-inverter through the NMOS pass transistors.

III. Simulation Results and Discussions

A. Soft-error Tolerance of PBLDP FF

We evaluate soft-error tolerance of ML by device simulations. Fig. 5 depicts the schematic and the cross section on device simulations of ML. By setting the initial value of N0 to 0 V, a particle with Liner Energy Transfer (LET) of 60 MeV-cm^2/mg hits at the NMOS transistor, because particles with lower energy than 60 MeV-cm^2/mg is much less than those over 60 MeV-cm^2/mg in outer space [7]. The stored value of the latch is not upset, even though a particle has LET of 60 MeV-cm^2/mg which is 10x larger than the threshold LET of the conventional latch. In Fig. 6, voltage waveforms of N1 and N2 are shown. The amplitude of the SET pulse is reduced by 45%.

B. Circuit Performance

Table I indicates the simulation results of area, delay time, static power and dynamic power at 10% data activity. All values are normalized to those of the TGFF. The values in parentheses are normalized to those of the stacked FF. The delay time and the dynamic power of the PBLDP FF are 22% and 52% smaller than that of the stacked FF. They are also smaller than that of the ACFF. However, the area and static power of the PBLDP FF are 1.2x and 36x lager than that of Stacked FF. This is because N0 or N2 becomes over the threshold voltage when N1 or N3 is 0 V.

The static power of the PBLDP FF is reduced by 95%, when body bias of -1 V is applied on NMOS transistors. Since the threshold of NMOS transistors is increased, the short-circuit current through the inverter is decreased. On the other hand, the static power of the PBLDP FF is reduced by 75% by applying -0.1 V to the gate of PMOS pass-transistors because the terminal N0 or N2 is close to 0 V. We synthesize a 32-bit micro controller by using the PBLDP FF and the TGFF. Table II shows the syntheized results. The total area with the PBLDP FF is 6% bigger than that with the conventional area although the area of the PBLDP FF is 23% bigger.

IV. Conclusion

The proposed PBLDP FF with high soft-error tolerance has 52% lower dynamic power and 22% shorter delay time than the conventional radiation hardened FF.

References

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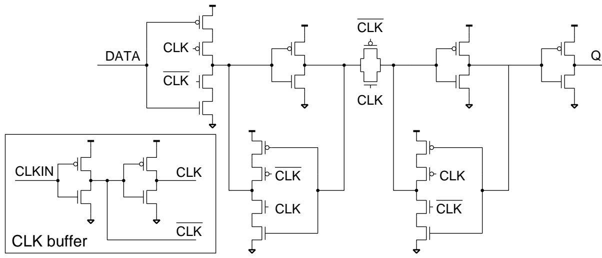


Fig. 1. Transmission-gate FF (TGFF).

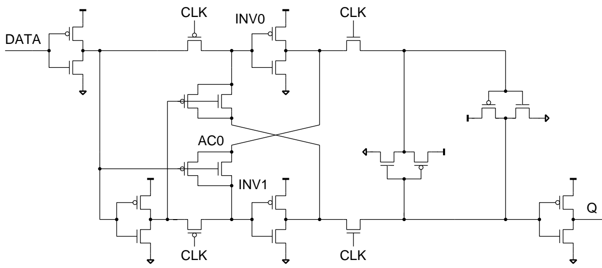


Fig. 2. Adaptive Coupling FF (ACFF).

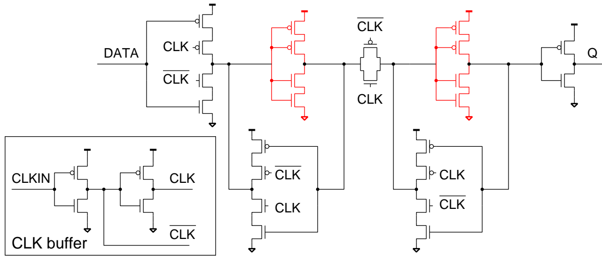


Fig. 3. Conventional stacked FF.

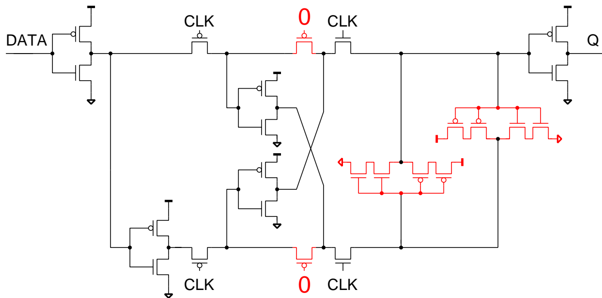
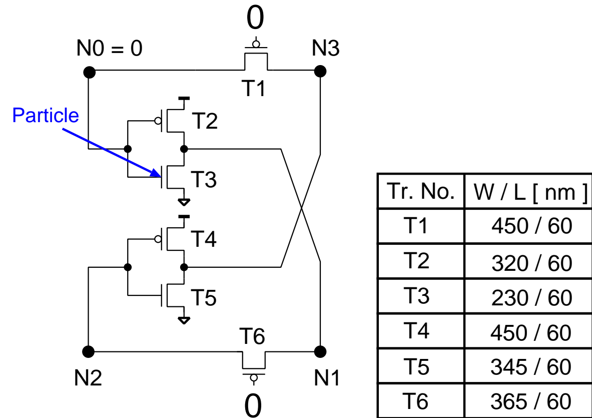
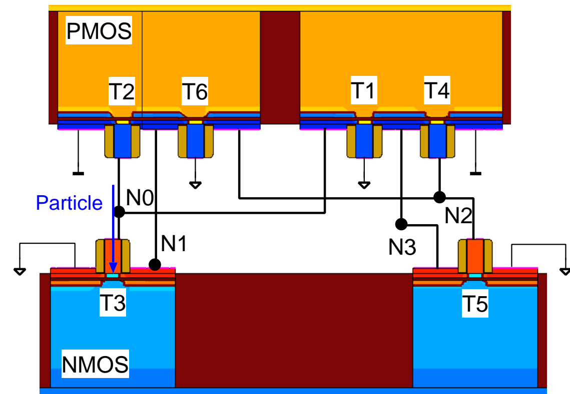


Fig. 4. Proposed PBLDP FF.



Tr. No.	W / L [nm]
T1	450 / 60
T2	320 / 60
T3	230 / 60
T4	450 / 60
T5	345 / 60
T6	365 / 60

(a) Schematic



(b) Cross section

Fig. 5. Schematic (a) and cross section (b) on device simulations of ML. By setting the initial value of N0 to 0 V, a heavy ion hits at the NMOS transistor at V_{DD} = 0.8 V. The transistor width and length are shown beside the schematic figure.

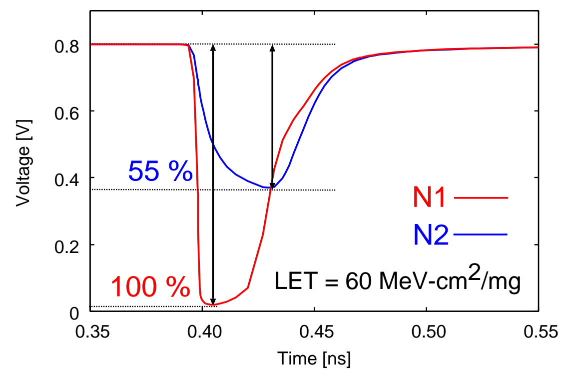


Fig. 6. SEU simulation results. N1 and N2 are influenced by a particle hit in Fig. 5. ML of PBLDP FF is not upset up to LET = 60 MeV-cm^2/mg .

TABLE I

SIMULATION RESULTS OF AREA, D-Q DELAY, POWER OF EACH FF. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKED FF.

FF	Area	D-Q delay	Dynamic Power	Static Power
TGFF	1	1	1	1
ACFF	1.00	1.44	0.47	2.35
Stacked FF	1.12	1.66	1.02	1.13
PBLDP FF	1.29 (1.15)	1.30 (0.78)	0.49 (0.48)	38.9 (36.2)

TABLE II

SYNTHESIZED AREA NORMALIZED BY THE RESULTS OF TGFF.

	TGFF	PBLDP FF
Connbinational	1	0.99
Noncombinational	1	1.23
Total	1	1.06