

# A Perpetuum Mobile 32bit CPU

with 13.4pJ/cycle, 0.14μA Sleep Current

using Reverse Body Bias Assisted 65nm SOTB CMOS Technology

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**Abstract** A 32-bit CPU which operates with the lowest energy of 13.4 pJ/cycle at 0.35V and 14MHz, operates at 0.22V to 1.2V and with 0.14μA sleep current is demonstrated. The low power performance is attained by Reverse-Body-Bias-Assisted 65nm SOTB CMOS (Silicon On Thin Buried oxide) technology. The CPU can operate more than 100 years with 610mAh Li battery. Keywords: MCU, CMOS, SOTB, and SOI

**Extended Abstract** Super low power CPU is necessary to make Perpetuum-Mobile computing into reality. This paper demonstrates 13.4pJ/cycle, 0.14μA sleep current CPU which operates at 14MHz at 0.35V, so that super low power operation and low sleep current are attained simultaneously.

The structure of the 65nm SOTB CMOS technology for core logic and SRAM along with Bulk technology for IO is shown in Fig. 1[1]. The original  $V_{th}$  for PMOS and NMOS in SOTB are low values of 0.20V and 0.19V, respectively. No pn junction exists between source and drain electrodes and wells, so that we can apply large RBB of up to -2.5V, which can drastically reduce leakage in sleep mode.

The power line architecture of the chip is illustrated in Fig. 2. IO circuits with 1st level shifters are formed by Bulk transistors. The 2nd level shifter, CPU logic and data memories are formed on SOTB transistors. For logic, VBB(voltage of RBB) of -0.5V is applied to minimize the energy/cycle value and  $V_{th}$  for p/n MOS transistors are increased to 0.26V and 0.25V, respectively. Larger body bias of SRAM (VBBM) of -1.0V is applied to reduce leakage of the high density 1.15Mbit SRAMs. The supply voltage of SRAM arrays(VDDM) is increased by 0.1V to VDD for high speed operations at low supply voltages. Memory IO circuits that consist of NAND gates are used in order to avoid speed degradation of macro interface at low VDD.

The CPU chips are fabricated by 65nm SOTB CMOS technology[1]. Photo micrographs CPU core and chip architecture are shown in Fig. 3. The CPU core consists of

in-order 5-stage pipeline, and 4 blocks of 32Kword X 9 data memory. Instructions are fed from an instruction memory out of the chip through the IO circuits. The CPU core, which consists of 50.1K gate logic and 1.15 Mbit 6T SRAM arrays and occupies 2.1 mm<sup>2</sup>. The CPU chips are also fabricated by 65nm Bulk-only CMOS using the same mask pattern to compare characteristics of CPUs for SOTB and Bulk technologies.

Fmax of 32bit CPU core was measured as shown in Fig. 4. A simple test program to check the CPU functions including ADD and the data memory read/write operations is carried out for the measurements. While instructions are supplied from ROM outside of the chip, data is stored in the data memory inside the chip. CPU on Bulk CMOS operates down to 0.5V however the Fmax is only 1MHz. CPU on SOTB CMOS with VBB of -0.5V can operate down to 0.22V and 1MHz. It operates 14MHz at 0.35V and 46MHz at 0.5V. The CPU on SOTB operates at lower supply voltage than Bulk by 0.28V, and operate faster by the factor of X46 at a supply voltage of 0.5V.

Energy per cycle of the 32bit CPU is shown in Fig. 5. The energy includes both energy for CPU logic and data RAM. When VBB(Logic RBB voltage) and VBBM(Memory RBB voltage) are suitably applied, the Emin can be drastically reduced and it reaches to 13.4pJ at VDD of 0.35V and VDDM(Supply voltage for memory) of 0.45V. Even when the CPU operates by Emin at 0.35V, it operates at high frequency of 14MHz, while CPU of ref[3] operates at Emin at only 73KHz. Therefore, the CPU on SOTB can achieve high performance with the smallest energy per cycle value.

Sleep current of the 32bit CPU when large VBB is applied is shown in Fig. 6. We can reduce the sleep current by more than three orders of magnitude when the VBB of -2.5V is applied. The effect to reduce the sleep current can be achieved even when temperature increases as shown in Fig.6. Therefore, we can prevent thermal runaway which is caused by positive feedback of leakage and temperature.

The operating and sleep current of CPU is normally trade off on MCUs as shown in Fig. 7. The CPU of this work can reduce both sleep current and operating current simultaneously, and it can reaches 38μA/MHz operating current and 0.14μA sleep current.

We have estimated average current and battery life when CPUs are used with 610 mA·h battery(equivalent to CR2032 Li coin battery), and capable energy harvesters as shown Table 1. When the CPU becomes sleep mode for 100s after it operates at 100ms periodically on SOTB, the estimated life of the battery becomes 134 years. This life is longer than that uses commercially available CPUs at any operation-sleep time ratio. The CPU operates at average current of 0.52μA, and it eternally continue to operate even with the ambient light energy harvesters that generates 10μA/cm<sup>2</sup> in door.

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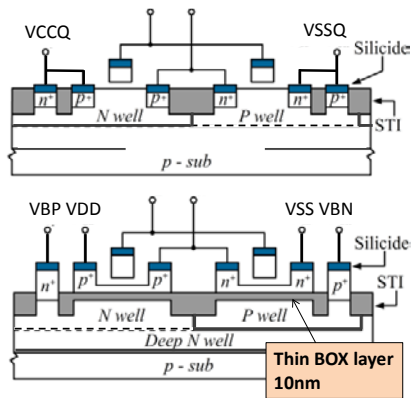


Fig.1. Structures of Bulk and SOTB MOSFET

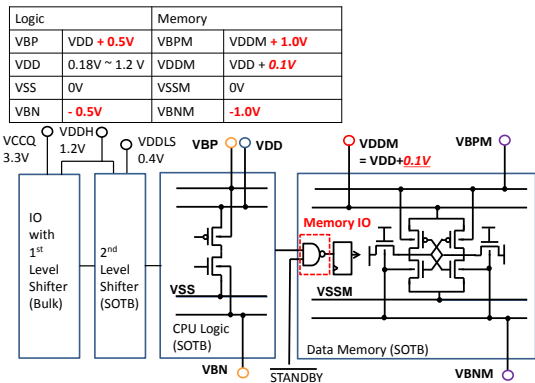


Fig. 2 Power line architecture

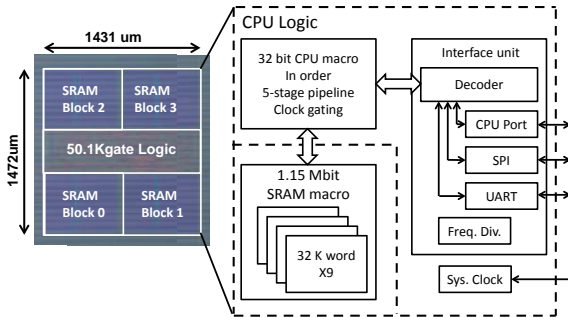


Fig. 3 32bit CPU Chip Micrograph and architecture

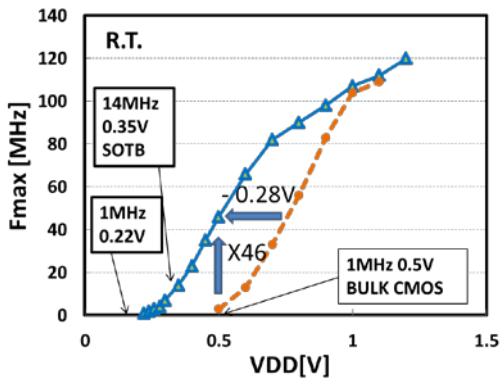


Fig.4 Maximum Operating Frequency of CPU

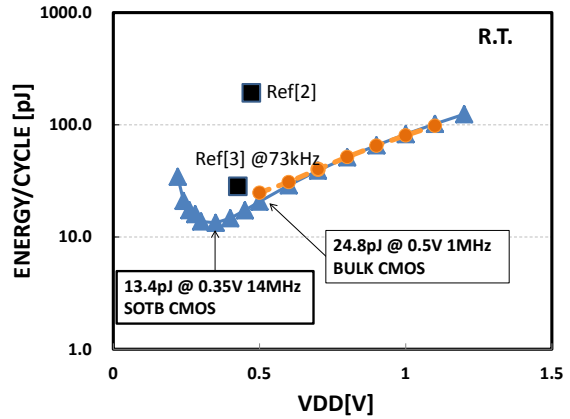


Fig 5 Energy/Cycle values of CPU

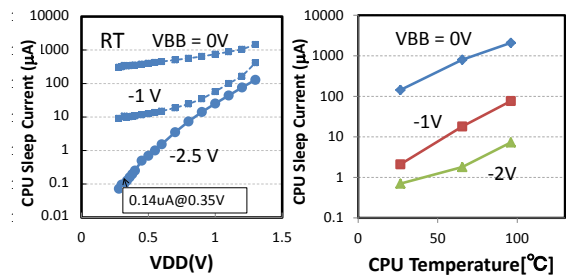


Fig. 6 Sleep current as functions of VDD and Temperature

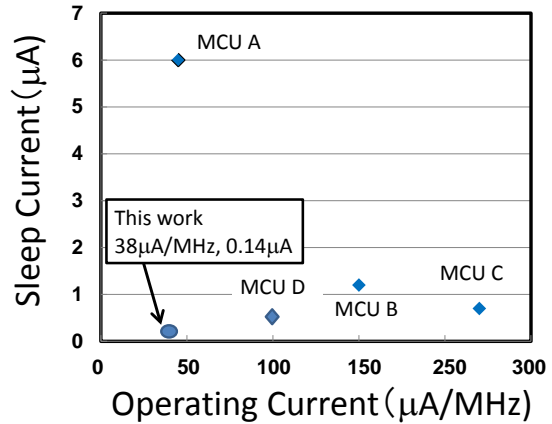


Fig. 7 Sleep Current as a function of operating current

Table 1 Average current and battery life, and capable harvest power

Operation time/ Sleep Time	Average Current (µA)	610 mAH Battery Life (Year)	Capable Harvest Power (cm-2)
100ms/100s	0.52	134	Ambient Light In door (10µW)
100ms/10s	3.94	17.6	Thermal Energy (30µW)
100ms/1s	38.1	1.8	Vibration (100µW)
Always in operation	380	0.18	Ambient light Out door (10000µW)