Capacitor-Based Three-Level Gate Driver for GaN HEMT Only with a Single Voltage Supply

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***Abstract*—This paper presents the capacitor based three-level gate driver for Gallium Nitride High Electron Mobility Transistor (GaN HEMT) using only a single voltage supply. The three-level gate driving method is effective to reduce reverse conduction loss of the GaN HEMTs and prevent false turn-on phenomenon in the half-bridge circuit. Conventional implementations require multiple voltage supplies resulting in large circuit area. The proposed gate driver has a capacitor which works as a voltage source to generate negative gate voltage by a single voltage supply. Measurement results of a half bridge circuit show that the proposed three-level gate driver prevents false turn-on and has less reverse conduction loss than a conventional two-level method. Thus, the proposed circuit improves the efficiency of the 48 V input and 12 V/ 4 A output SR-Buck converter by 1.6% compared to the conventional one.**

***Index Terms*—GaN-HEMT, Gate Driver, three-level driving, false turn-on, reverse conduction loss, SR-Buck converter.**

I. INTRODUCTION

Recentry, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) are a promising candidate to improve efficiency power density of power conversion circuits, because they have superior device characteristics such as high speed switching capability, high break down field and low on-resistance compared to conventional Silicon (Si) devices [1] [2] [3] [4]. Thanks to these superior characteristics, GaN HEMTs are suitable for a lot of applications such as electric vehicles and drones which must to be miniaturized and have higher efficiency. Moreover, the reverse recovery loss can be ignored because GaN HEMTs have no PN junction between drain and source terminals, resulting in improving efficiency of power conversion circuits such as a power factor correction (PFC) circuits and synchronous rectifier (SR) buck converters which have bridge-leg configuration [5].

However, owing to the low threshold voltage $V_{\rm th}$ and large switching noise caused by the fast switching, false turn-on is more likely to occur in bridge circuits by GaN HEMTs compared to Si devices [6] [7] [8]. It leads to undesirable operations such as circuit oscillation, higher power loss and overheating. Furthermore, in the worst case, GaN HEMTs can be damaged. It must be a limitation when GaN HEMTs are apply to power conversion circuits. To solve this problem, in conventional 2-level methods, negative voltage is supplied to the gate terminal of GaN HEMTs. However additional power supply for negative voltage is required, resulting in increasing the circuit area. In addition, lateral GaN HEMTs without body diodes, the reverse current flows through the channel of by the reverse conduction mechanism. As a result, the reverse conduction loss is increased when GaN HEMTs are driven by negative gate voltage during freewheeling operation [9].

The multiple level driving, in which negative voltage is applied just after turn-off to overcome false turn-on and 0 V or more voltage applied for reducing the reverse conduction loss during dead time, is an effective method for GaN HEMTs. A 3-level gate driving method for GaN HEMTs is proposed in [10]. The proposed circuit applies negative bias to improve dv/dt immunity when a GaN HEMT turns-off, and provides the middle-level voltage with the GaN HEMT to reduce reverse conduction loss during dead time before turn-on switching. The measurement results realize to improve efficiency of an isolated resonant converter. However, the proposed circuit has an additional power conversion circuit to generate the middle-level voltage, resulting in circuit area increase. As shown in Fig. 1, the driving method using a speed-up capacitor is recommended in [11] and [12]. However, it is suitable for GaN HEMTs which have PN junction diode $D_{\rm p}$ whose forward voltage $V_{\rm F}$ is around 3.5 V formed between gate and source terminals, but not for GaN HEMTs without $D_{\rm p}$ such as GS66504B and EPC2207 [13] [14], because the voltage $V_{\rm c}$ $(= V_{\rm DD} - V_{\rm F})$ is applied to the speed-up capacitor during on-state. In addition, the capacitor is directly connected to the gate of the GaN HEMT. Thus, the turn-on time is larger because it can not be completely discharged with the high frequency operation over 500 kHz [11].

In this paper, we propose a three-level gate driver using a capacitor for GaN HEMTs in bridge circuits. The capacitor works as a voltage source to supply negative gate voltage to the GaN HEMT without any additional voltage source. Measurement results show that the proposed gate driver has capability to prevent false turn-on, reduce reverse conduction loss and improve efficiency of SR buck converters.

This paper organized as follows. We explain the false turn-on and reverse conduction mechanism of GaN HEMTs in Section 2. Section 3 presents operation principle of the proposed 3-level gate driver. Section 4 shows measurement results and Section 5 concludes this work.

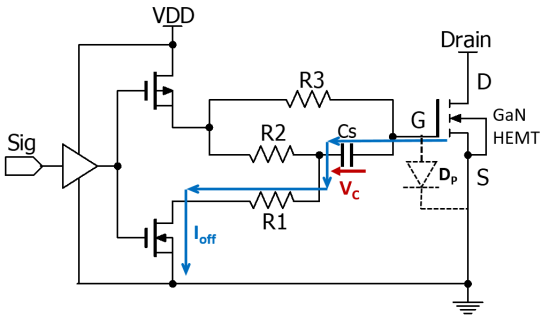

Fig. 1. Gate driver using a speed-up capacitor C_{s}.

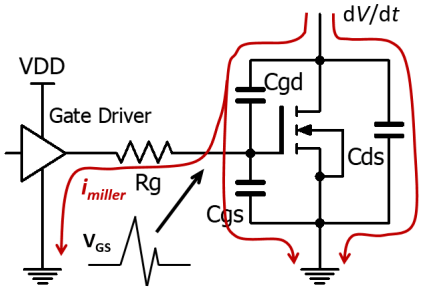

Fig. 2. Mechanism of false turn-on phenomenon at the low-side switch.

II. PROBLEMS OF GAN HEMTS

A. False turn-on phenomenon of GaN HEMTs

A half-bridge circuit is the major circuit configuration used in many power conversion circuits such as an SR buck converter and Totem Pole PFC circuit, etc. There is a specific problems which is false turn-on phenomenon causing power loss and power device failure.

To implement a half-bridge circuit by GaN HEMTs, false turn-on is caused by high positive dv/dt during off state of the low-side switch. Fig. 2 shows the mechanism of the false turn-on phenomenon at the low-side switch in the half-bridge circuit. When the high-side switch is turned on, high positive dv/dt from the drain to the source terminal of the switch is generated. Then, Miller current i_{miller} flows to the ground through the Miller capacitor C_{GD}, the gate resistor R_{G} and the gate driver. Then, LCR resonance turns on the low-side GaN HEMT if this ringing voltage exeeds the V_{th} [15]. For the GaN HEMTs, the threshold voltage is as low as 1.4 V typically, which is smaller than that of conventional devices such as Si and SiC (Silicon Carbide) devices. Therefore, it is a serious problems for GaN HEMTs due to its low V_{th}.

In conventional methods, a negative gate to source voltage V_{GS} is applied during off-state to increase the mergin of the LCR resonance amplitude and improve the dv/dt immunity of GaN HEMTs (2-level methods). However, an additional voltage supply is required to generate the negative voltage, resulting in increasing circuit area. In addition, in the case of GaN HEMTs which have reverse conduction characteristics, this conventional method increases the power loss during freewheeling operation.

Another simple method is to connect an RC snubber circuit consisting of a resistor and a capacitor between the gate and source terminals of a GaN HEMT. It is effective to suppress the resonance voltage, but switching speed is decreased due to the additional capacitor, resulting in increasing the switching loss [16].

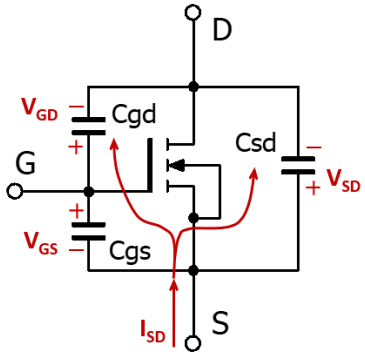

Fig. 3. Mechanism of reverse conduction and the equivalent model of GaN HEMT.

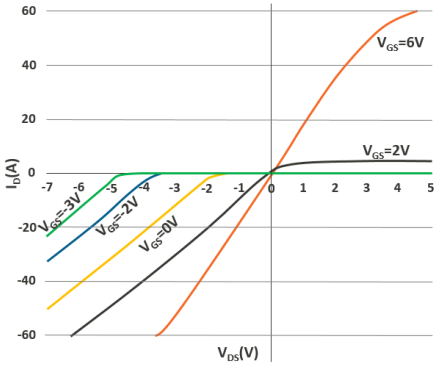

Fig. 4. V-I curve of GaN HEMT [13].

B. Reverse conduction mechanism of GaN HEMT

Another important problem of GaN HEMTs is the high reverse conduction loss. GaN HEMTs have reverse conduction characteristics because they have no body diode unlike Si and SiC MOSFETs.

Fig. 3 shows an equivalent model of a GaN HEMT and the mechanism of the reverse conduction. When V_{GS} is 0, a capacitor C_{gs} is not charged, which means the gate and source terminals are short-circuited and capacitors C_{sd} and C_{gd} are connected parallel. At this time, current flows from the source terminal to the GaN HEMT, the C_{gd} and C_{sd} are charged, the channel begins to build if the capacitor voltage V_{GD} reaches V_{th}. This is because the source and drain of the GaN HEMT are symmetrical at the gate. GaN HEMT is turned on if positive voltage above V_{th} is applied across the gate and drain terminals. The current from the source flows through

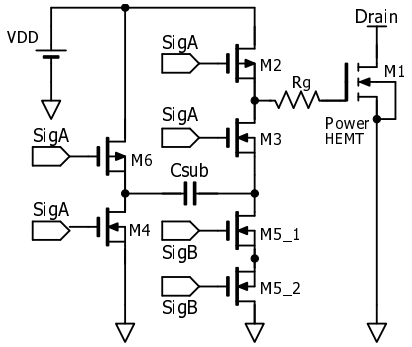

Fig. 5. Proposed three-level gate driver.

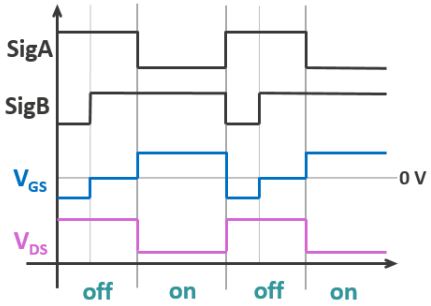

Fig. 6. Control waveforms of the proposed gate driver.

the channel, and the voltage drop across the source and drain V_{SD} is expressed as $V_{\mathrm{SD}} = V_{\mathrm{GD}} = V_{\mathrm{th}}$. This is the reverse conduction mechanism of GaN HEMTs.

When the negative gate voltage V_{GS} is appllied to the gate, C_{gd} is charged via C_{gs}. The voltage drop is increased the V_{GS} applied to C_{gs}. Therefore, when a negative voltage is applied, the voltage drop V_{SD} is expressed by the following equation.

$$V_{\mathrm{SD}} = V_{\mathrm{GD}} - V_{\mathrm{th}} \tag{1}$$

As a result, the IV characteristics of the GaN HEMT is as shown in Fig. 4 [13]. For example, the negative gate voltage -2.5 V is applied to the GaN HEMT, the voltage drop is higher than $V_{\mathrm{th}}-(-2.5\ \mathrm{V})$, which is larger than the V_{F} of the body diode of the Si devices. Therefore, in the case of GaN HEMTs, the conventional method using negative gate voltage to overcome the false turn-on phenomenon causes an increase in reverse conduction loss.

III. PROPOSED 3-LEVEL GATE DRIVER

Figure 5 shows the proposed capacitor-based three-level gate driver and Fig. 6 shows control waveforms of the proposed gate driver, respectively. It consists of Si MOSFETs and a capacitor C_{sub} and in order to perform the operation, the proposed gate driver is controlled by the two independent input signal sources (SigA, B). The capacitor works as a voltage source to supply negative gate voltage to the GaN HEMT during turn-off transient to prevent false turn-on. The operation principle of the proposed gate driver is shown in Fig. 7 and described as follows.

1) Current flows along the blue line to the gate terminal of the GaN HEMT, and the input capacitance C_{iss} is charged. Then the GaN HEMT is turned on. During on-state, current flows to the ground through the C_{sub}, and energy is stored in C_{sub}, also V_{C} is generated.

2) Current flows to the ground through the C_{sub}, the GaN HEMT turns off. Then, the C_{sub} operates as a voltage source, the GaN HEMT is driven by negative gate voltage $-V_{\mathrm{C}}$ to prevent false turn-on.

3) Current flows from the ground to the gate terminal before dead time. Then, the C_{iss} is charged, the V_{GS} settles to 0 V to reduce the reverse conduction loss.

The proposed gate driver can operate at three gate voltage levels (V_{DD}, negative gate voltage at turn-off transient and 0 V during off-state) without any additional voltage source, owing to C_{sub}. Therefore, it is possible to improve dv/dt immunity and reduce reverse conduction loss of the GaN HEMTs, with small circuit area. The Si MOSFET, M5_1 and M5_2, driven by SigB form a common-source-type bidirectional switch to flow current bidirectionally [17].

In the conventional method, the speed-up capacitor is used for the gate driver to apply the negative gate voltage. The speed-up capacitor is directly connected to the gate terminal, and GaN HEMT is turned off by negative voltage using the voltage applied to the capacitor during on-state. However, the turn-on time depends on switching frequency. If the off-state time is short ($< 5\ \mu$s), turn-on switching time is increased because the capacitor connected to the gate terminal can not be completly discharged during off-state. As a result, the switching loss is increased. In addition, to turn off switching with negative gate voltage, the voltage of the speed-up capacitor is required. It can only be used for some GaN HEMTs which have the diode characteristics between the gate and source terminals. On the other hand, in the proposed gate driver, off-state time does not affect turn-on switching whether it has completely discharged or not, because C_{sub} is not directly connected to the gate terminal. The proposed gate driver is suitable for power conversion circuit at high frequency. Moreover, since the voltage V_{C} which is approximately as large as V_{DD} is applied to the C_{sub}, it can also be used for GaN HEMTs without diode characteristics.

IV. MEASUREMENT RESULTS

In this section, measurement results show when the proposed gate driver is applicated to a resistor-load type measurement circuit, a half-bridge circuit, and an SR buck converter.

A. Resistor load type measurement circuit

The resistor-load type measurement circuit for the proposed gate driver is shown in Fig. 8. This circuit is used to measure switching frequency dependency of the switching characteristics of the proposed gate driver.

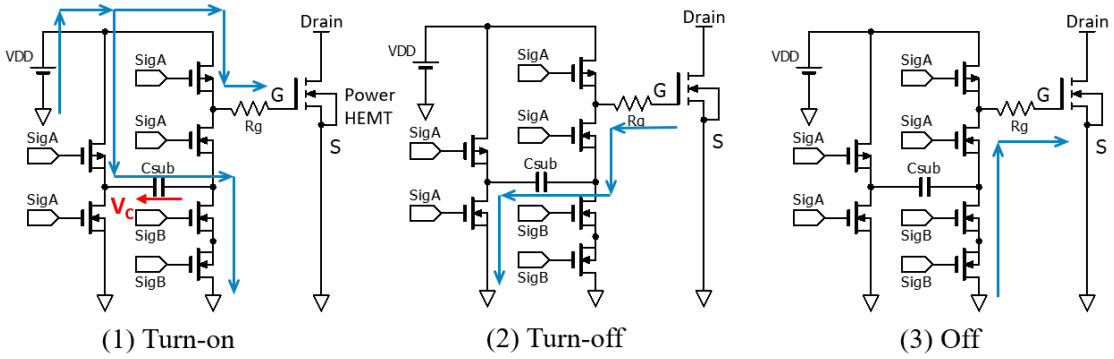

Fig. 7. Operation principle of the proposed gate driver.

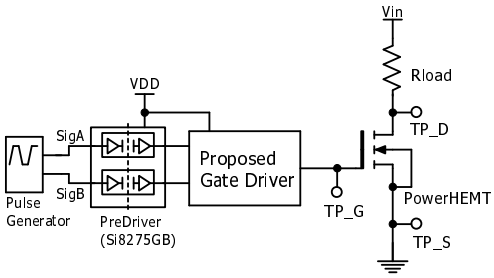

Fig. 8. Resistor load type measurement circuit.

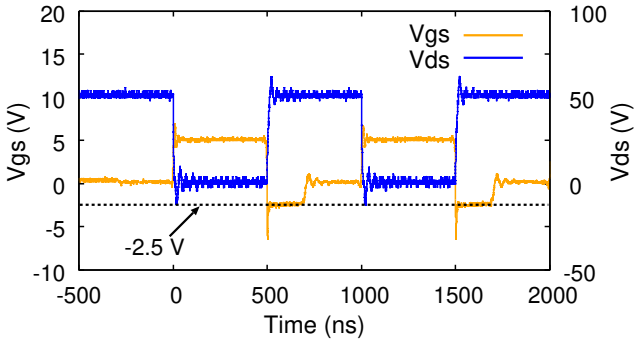

Fig. 9. 1 MHz switching waveforms of the proposed gate driver.

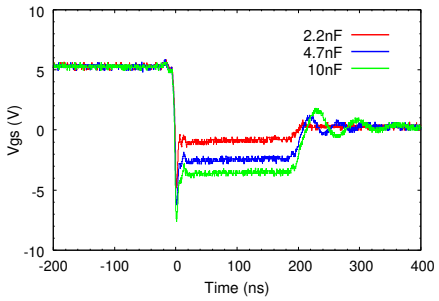

Fig. 10. The voltage V_{GS} during turn-off for different values of the C_{sub}.

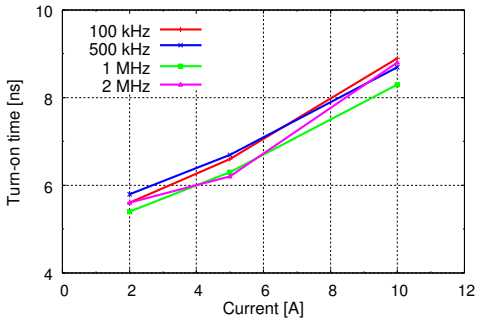

Fig. 11. Evaluation result of the turn-on switching time.

The capacitor C_{sub} is a 4.7 nF ceramic capacitor and a gate resistor R_{G} is 1 Ω for the proposed gate driver. The GaN HEMT used for measurement is GS66504B (GaN Systems). Contorol signals (SigA and B) are generated by an Analog Discovery2 (Digilent Inc.) and amplified by an isolated gate driver IC (Silicon Labs, Si8275GB) to drive the transistors consisted of the proposed gate driver. The oscilloscope used for the experiment was DPO 7054C of Tektronix. Voltage waveforms were obtained at the test points (TP_G, D, S). V_{in} determines off-state V_{DS}, and Rload determines on-state I_{D} during the measurement.

Fig. 9 shows continuous switching waveforms of the proposed gate driver at 50 V of V_{in}, 25 Ω of Rload and 1 MHz operation frequency. From the result, it is confirmed that it is driven by the negative voltage of −2.5 V at turn-off and after then stable at 0 V. Therefore, the measurement results prove the three-level gate voltage operation of the proposed gate driver without any additional voltage source.

Fig. 10 shows the capacitance of C_{sub} dependency of the switching characteristics at turn-off of the proposed gate driver. It can be confirmed that the negative voltage becomes larger as C_{sub} increases. It is possible to improve the dv/dt immunity by choosing an appropriate C_{sub} from the amplitude of gate voltage oscillation.

Fig. 11 shows the switching frequency and the drain currnt dependency of the turn-on switching time of the proposed gate driver. The turn-on time t_{on} is determined as the delay time when V_{GS} rises to 10% until V_{DS} drops to 10%. From

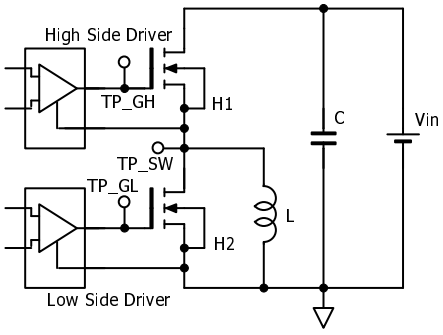

Fig. 12. Low side regeneration half-bridge circuit.

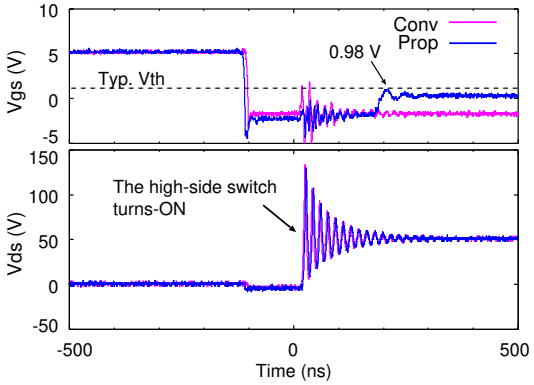

Fig. 13. Measurement results of the bridge-circuit at turn-off transient.

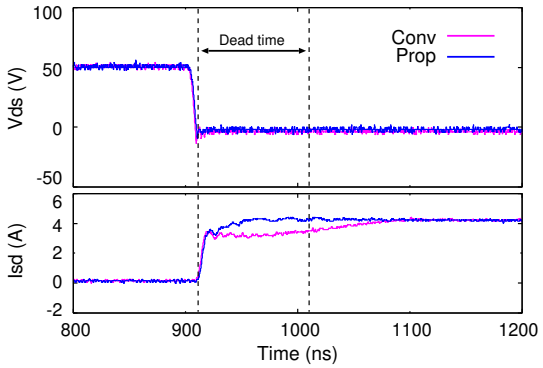

Fig. 14. Measurement results of the bridge-circuit during dead time.

the measurement results, the t_{on} is almost constant even if the switching frequency is increased. This is because C_{sub} is not directly connected to the gate terminal of the GaN HEMT and does not affect the turn-on switching. Therefore, the proposed gate driver can bring out the igh-speed switching characteristics of GaN HEMTs even when it operates at high frequency.

B. Half-bridge evaluation circuit

Figure 12 shows the low-side regeneration half-bridge circuit to evaluate false turn-on phenomenon and reverse conduction loss compared with the conventional 2-level driving

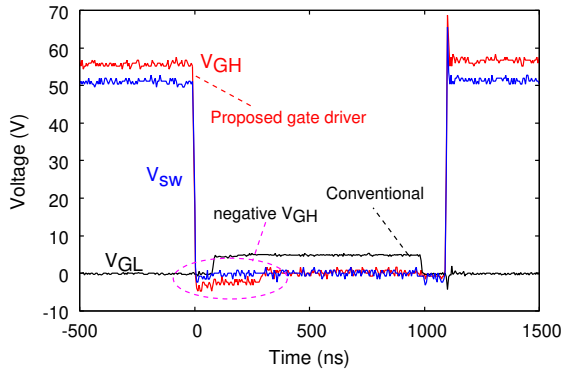

Fig. 15. Measurement waveforms of the bridge circuit when the proposed gate driver implemented high-side switch.

method [11]. The gate driver IC Si8275 is used for conventional 2-level gate driver (named Conventional) and the negative gate voltage is set to -2.5 V. The components consisting of the proposed gate driver and the equipment for the measurement are the same as the previous section A, respectively. The half-bridge circuit is composed of the GS66504B (Typ. $V_{\mathrm{th}} = 1.3$V) with dead time of 100 ns. A 100 μH inductor is used for the evaluation circuit.

Figures 13 and 14 show the measurement waveforms of the low-side regeneration circuit at the low side switch at 50 V of the input voltage V_{in}, 4 A of the input current at 500 kHz switching frequency, when the proposed gate driver is implemented to the low-side switch. From the Fig. 13, when the high-side switch turns on, ringing of V_{GS} is caused by the high positive dv/dt, but ringing voltage does not reach the threshould voltage 1.3 V of the GaN HEMT owing to the negative gate voltage. The voltage level, caused when the proposed gate driver returns from negative volatge to 0 V, does not also exceed the V_{th}. Evaluation results of the reverse conduction loss are, 8.7 W and 11.4 W on the proposed gate driver and the conventional 2-level method, respectively. During dead time, voltage drop V_{SD} of the conventional method is 3.8 V but that of the proposed gate driver is 2.3 V, reducing the reverse conduction loss by 23%. From these results, it is confirmed that the proposed gate driver has capability to prevent false turn-on phenomenon and reduce reverse conduction loss during freewheeling operation.

Fig. 15 shows measurement waveforms when the proposed gate driver is implemented as the high-side switch. From Fig. 15, it can be confirmed that the proposed gate driver can operate at three gate voltage levels even when the proposed gate driver is only used at the high side. Therefore, it is expected that the proposed gate driver improves efficiency of the power conversion circuit which has the freewheeling operation even at the high-side switch such as an LLC resonant converter and an inverter circuit.

C. 48 V to 12 V synchronous buck converter

Figure 16 shows a simplified schematic of the synchronous buck converter with gate drivers. Conversion efficiency is

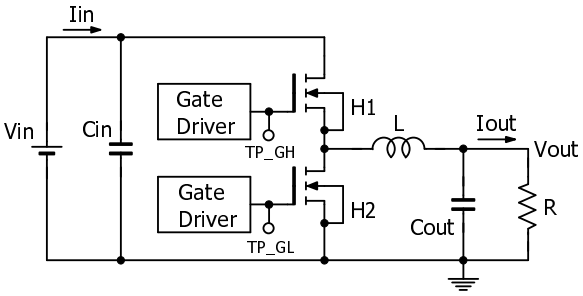

Fig. 16. Simplified synchronous buck converter schmatics.

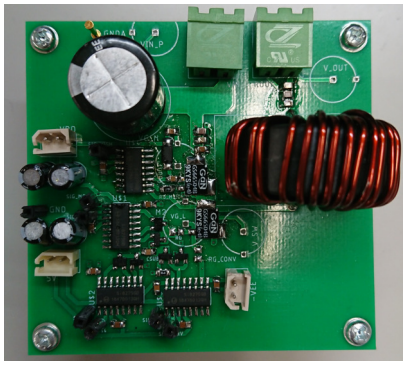

Fig. 17. Photo of the implemented SR buck converter on the board.

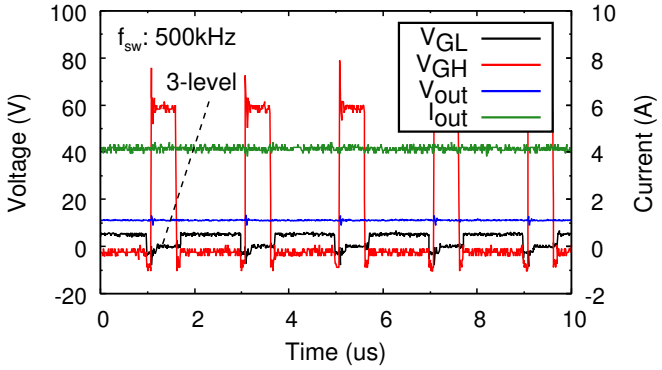

Fig. 18. Measurement waveforms of the 48 V - 12 V SR buck converter using the proposed gate driver for the low-side switch.

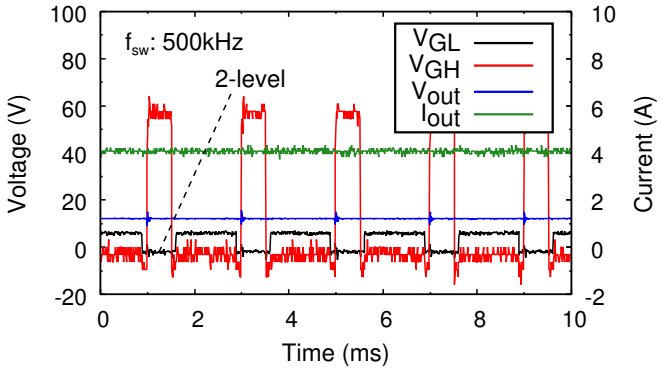

Fig. 19. Measurement waveforms of the 48 V - 12 V SR buck converter using the conventional gate driver for the low-side switch.

compared when the proposed gate driver and the conventional 2-level method are used for the low-side switch of the SR buck converter, respectively. The components used in the proposed gate driver and the SR buck converter are the same as those of the low-side regeneration half-bridge circuit of the previous section B. The specification is 48 V of input voltage $V_{\rm in}$, 12 V of output voltage $V_{\rm out}$ and 4 A of output current $I_{\rm out}$ (48 W). The photograph of the SR buck converter implemented on the print circuit board is shown in Fig. 17. The gate resistor can be replaced on the print-circuit board.

Figures 18 and 19 show the measurement waveforms when the proposed gate driver and the conventional method were used, respectively. The operating frequency is 500 kHz and the dead time is 100 ns. The evaluation results were 48 V of $V_{\rm in}$, 1.1 A of $I_{\rm in}$ and 52.8 W of the input power $P_{\rm in}$ for both of the proposed gate driver and the conventional method. On the other hand, when the conventional method was used, results were 12.1 V of $V_{\rm out}$, 4.1 A of $I_{\rm out}$ and 49.6 W of the output power $P_{\rm out}$, while the proposed gate driver was 12.0 V of $V_{\rm out}$, 4.2 A of $I_{\rm out}$ and 50.4 W of $P_{\rm out}$. Therefore, the proposed gate driver achieved 95.5% conversion efficiency, which is 1.6% higher than that of the conventional method. This is because the reverse conduction loss during dead time was reduced by the 3-level method.

Table I shows measurement results at 1 MHz switching time (dead time was set to 50 ns). The efficiency of the proposed gate driver was 4.6% higher than the that of the conventional method.

From the above results, the proposed gate driver is capable of the 3-level gate voltage operation with a single voltage supply, and achieved high efficiency in an SR buck converter composed of GaN HEMTs.

V. CONCLUSION

In this paper, we proposed the capacitor-based three-level gate driver for GaN HEMTs in half-bridge circuits in order to improve the dv/dt immunity and reduce the reverse conduction loss. The capacitor in the proposed gate driver works as a voltage source to supply negative gate voltage to the GaN HEMT during turn-off transient. The experimental results demonstrated that the proposed gate driver works at the 3-level gate levels operation without using an additional voltage

TABLE I
EVALUATION RESULTS OF THE SR BUCK CONVERTER (CONVENTIONAL 2-LEVEL METHOD VS. PROPOSED 3-LEVEL GATE DRIVER)

	Conventional		Proposed	
Frequency	500 kHz	1 MHz	500 kHz	1 MHz
Pin [W]	52.8	54.7	52.8	53.6
Pout [W]	49.6	47.1	50.4	48.6
Efficiency	93.9%	86.1%	95.5%	90.7%

supply. Compared to the conventional 2-level method, the proposed gate driver reduced reverse conduction loss by 23% in a half-bridge evaluation circuit. In the SR buck converter with 48 V input, 12 V/ 48 W output and 500 kHz switching frequency, the proposed gate driver improved efficiency by 1.6% over the 2-level method.

One of the great advantages of GaN HEMTs is monolithic integration with the gate driver on a chip [18]. This method can be suppressed parasitic inductance and faster switching operation. We plan to integrated the proposed gate driver with the power GaN HEMT monolithically, aiming for further high-speed switching and high efficiency.

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