Design of RCD Snubber Considering Wiring Inductance for MHz-Switching of SiC-MOSFET

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***Abstract*—The RCD (Resistor-Capacitor-Diode) snubber is usually designed without considering which wiring inductance seriously affects circuit behaviors, although the influence appears significantly at high-frequency operation. We investigate an optimal design of the RCD snubber for MHz-switching of SiC-MOSFETs considering location of parasitic wiring inductance. The mechanism of ringing induced by wiring inductance, and ringing suppression by the RCD snubber are also discussed. The wiring inductance near the gate and source terminals should be minimized. The wiring inductance near the gate and drain terminals must be considered to design an optimal RCD snubber.**

***Keywords*—SiC-MOSFET, Snubber, Wiring inductance, High-speed switching, Ringing**

I. Introduction

Recently, power converter circuits can be operated at MHz-level with appearing of wide gap semiconductor devices such as SiC (Silicon Carbide) and GaN (Gallium Nitride) devices as mentioned in [1], [2], [3]. A promising switching speed to drive SiC-MOSFET is 13.56 MHz [4], which is one of the ISM (Industory Science Medical) bands. High-frequency operation makes circuit systems compact with smaller passive components. However, ringing occurs at high-speed switching because voltage and current steeply fluctuate during switching. Ringing induces electromagnetic interference (EMI) noise and malfunction, which threatens reliability. Thus it is necessary to address ringing noise especially for MHz-switching [5]. The discharge-suppressing resistor-capacitor-diode snubber (hereinafter referred to as RCD snubber) is commonly used to suppress ringing at a MHz frequency operation [6]. The RC parameter of the RCD snubber is calculated by the common method as introduced in [7], [8].

However, the locations of the parasitic inductance are ignored in the calculation. In this paper, we present a guideline of the RCD snubber design considering the location of parasitic inductance for a high frequency operation. We evaluated influence of wiring inducatnce on MHz-switching with SiC-MOSFET, and ringing suppression by the RCD snubber considering location of wiring inductance.

Section II explains our motivation. Sect. III describes influence of wiring inductance on switching. The ringing suppression by the RCD snubber is discussed in Sect. IV. We propose an optimal design of the RCD snubber in Sect. V. Sect. VI concludes this paper.

II. Wiring Inductance

Power devices ideally have no ringing on switching as shown in Fig. 1 (a). Actually, peripheral parasitic inductance $L_{\rm p}$ induces ringing during switching as shown in Fig. 1 (b). The voltage over $L_{\rm P}$ is expressed by following Eq. (1).

$$V_{L_{\rm p}} = L_{\rm p} \times \frac{di}{dt} \tag{1}$$

As high frequency operation is accompanied with high di/dt, $V_{\rm r}$ has a fatal impact against power devices. Snubber circuits are commonly used to suppress the ringing. The RCD snubber circuit as shown in Fig. 2 is suitable for high frequency because of lower-power consumption. The principle is described as below. The snubber capacitor absorbs ringing through the snubber diode $D_{\rm snub}$ at turn OFF. The excessive noise is consumed by the snubber resistor during OFF. The snubber does not suppress ringing at turn ON because $D_{\rm snub}$ keeps current conducting only in one direction, and it saves energy efficiently.

The RC parameters of the RCD snubber, $C_{\rm snub}$, $R_{\rm snub}$ are calculated with Eqs. (2) $\sim$ (4) [9]. Definition of the symbols in the equations are shown in table I.

$$C_{\rm snub} = \frac{L_{\rm M} \times {I_{\rm OFF}}^2}{(V_{\rm DSp} - V_{\rm DD})^2} \tag{2}$$

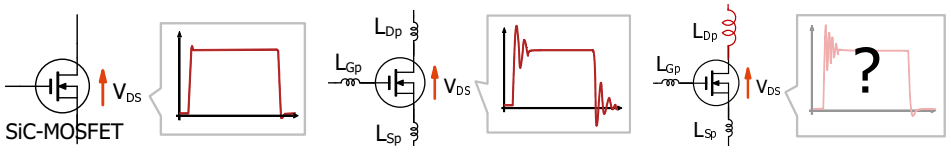
$$V_{\rm DSp} = V_{\rm DD} + V_{\rm F} + L_{\rm S} \cdot \frac{dI_{\rm D}}{dt} \tag{3}$$

$$R_{\rm snub} \leq \frac{1}{2.3 \cdot C_{\rm S} \cdot f_{\rm sw}} \tag{4}$$

Note that the total parasitic inductance in the circuit $L_{\rm M}$ is used in the calculation as can be seen in Eqs. (2), (4). It means that the peripheral parasitic inductance $L_{\rm Gp}$, $L_{\rm Dp}$,

TABLE I: Definition of the symbols in the equations.

Symbol	Explanation
$L_{\rm M}$	total inductance in the circuit
$I_{\rm OFF}$	Drain current at turn OFF
$V_{\rm DSp}$	peak surge voltage of $C_{\rm snub}$
$V_{\rm DD}$	voltage supply
$V_{\rm F}$	Forward voltage of Diode $D_{\rm snub}$
$L_{\rm S}$	inductance of the snubber circuit
$dI_{\rm D}/dt$	maximum drain current slope at turn OFF
$f_{\rm sw}$	switching frequency



(a) Ideal (b) Actuality (c) $L_{\mathrm{Dp}} > L_{\mathrm{Gp}}, L_{\mathrm{Sp}}$

Fig. 1: Effect of wiring inductance on switching.

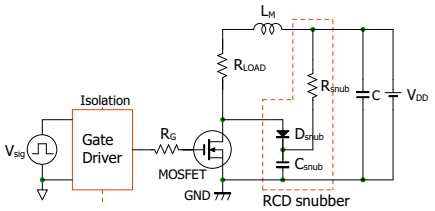


Fig. 2: An RCD snubber circuit.

L_{Sp} are not independently considered, while the ratio of parasitic inductance L_{Gp}, L_{Dp}, L_{Sp} varies depending on the circuit designs. We investigate how the location of parasitic inductance affects on the ringing suppression in order to address an optimal wiring design. Firstly, the dependence of the wiring inductance location is investigated in three cases; (i) L_{Gp} (ii) L_{Dp} (iii) L_{Sp} is dominant. Fig. 1 (c) shows the case (ii). Secondly, the ringing suppression effect by the RCD snubber is similarly investigated in three cases.

III. Influence of Wiring Inductance on SiC-MOSFET Switching

A. Measurement setup

We evaluate influence of wire inductance on switching. The switching characteristics are measured by the double pulse test (DPT), which is commonly used to evaluate switching characteristics of power devices such as MOSFETs and IGBTs [10], [11]. Figs. 3, 4 shows the DPT waveforms and circuit respectively. Turn ON, OFF characteristics are measured at the point shown in Fig. 3. The drain current I_{D} at turn ON is adjusted by the first ON pulse period (phase 1). I_{D} at turn OFF must be almost same with phase 2 because the energy consumed in the diode D during OFF (phase 3) is quite small compared to the magnetic energy stored in the inductor L during phase 1.

The DPT allows thermally-stable measurement because only a single-shot pulse is applied during measurement. In contrast, measurement with periodic pulses may cause fluctuation of switching characteristics due to self-heating of the power devices. In addition, parasitic inductance on the power line has small influence on measurement with the DPT.

The schematic of the measurement circuit is shown in Fig. 5, and an implemented print circuit board is shown in Fig. 6. Silicon Labs Si8234 is used for the gate driver. It isolates between the input signal controller circuit and the DPT circuit by RF (radio frequency) technology. The DPT input signal is generated by function generator KEYSIGHT 81160A. The gate resistor R_{G} of 1 Ω prevents from ringing. The device under test (DUT) is SCT2450KE SiC-MOSFET from Rohm

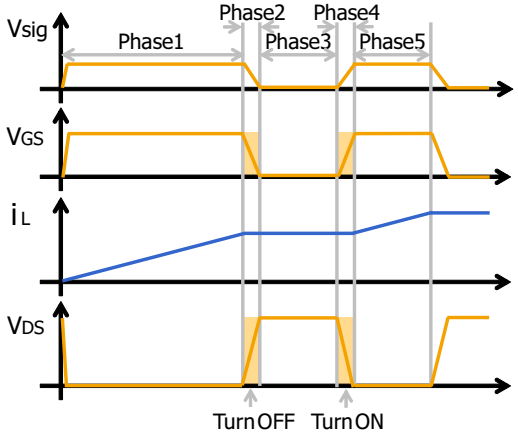


Fig. 3: DPT waveform.

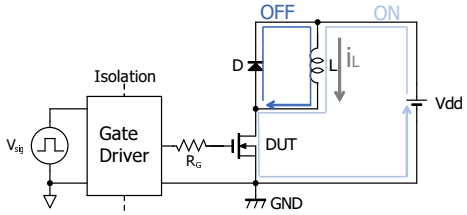


Fig. 4: DPT circuit.

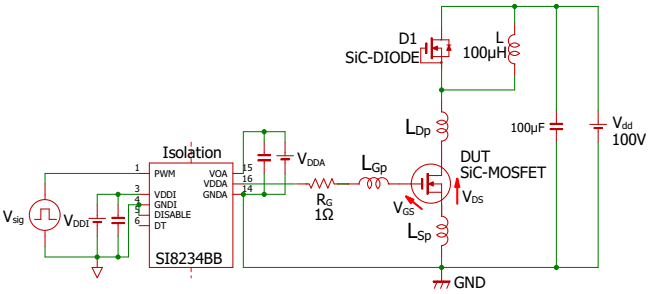


Fig. 5: DPT circuit to evaluate wiring inductance effects.

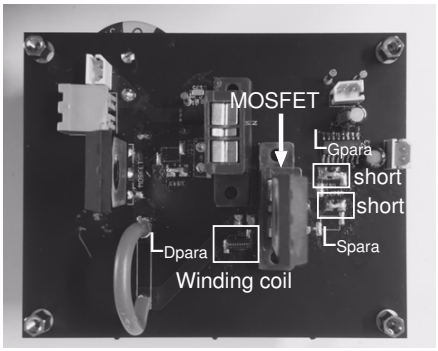


Fig. 6: Print circuit board for evaluation.

Co., Ltd. Its switching speed is fast and suitable for MHz-operation because of its small input capacitance C_{iss} of 463 pF [12].

The gate source voltage V_{GS} and drain source voltage V_{DS}, and drain current I_{D} are measured with the oscilloscope Tektronix DPO7054C. The switching characteristics are measured at the supply voltage V_{DD} = 100 V and I_{D} = 5 A.

The circuit is designed to be able to put a winding coil of 20 nH or 40 nH near the gate, drain and source terminals represented by L_{Gp}, L_{Dp}, L_{Sp}. The winding coils are regarded as wiring inductance. Inductance of 20 nH is equivalent to a copper-foil wire line which has a thickness h of 35 μm, a width w of 5 mm, and a length l of 50 mm. For reference, the maximum capacity of current per mm wire-width is approximately 1 A in root mean square value [13]. The wire inductance L_{P} is calculated by Eq. (5). L_{P} has unit of nH, when l, w, h have unit of mm [14].

$$L_{\mathrm{para}} = 0.2l\{\ln\left(\frac{2l}{w+h}\right) + 0.2235\left(\frac{w+h}{l}\right) + 0.5\} \quad (5)$$

Note that only one winding coil of L_{Gp}, L_{Dp}, or L_{Sp} is attached during measurement as shown in Fig. 6 in order to specify which wiring inductance is dominant.

B. Results and Discussions

Figure 7 shows switching waveforms at several L_{P} conditions. These characteristics are evaluated by switching time T_{ON}, T_{OFF}, rigning voltage V_{DSring} and energy loss E_{Loss} as defined in Fig. 8. E_{Loss} is defined as the energy loss of the DUT during a switching cycle T at 1 MHz. The evaluation results are shown in Fig. 9. The influence of each wiring inductance is described below.

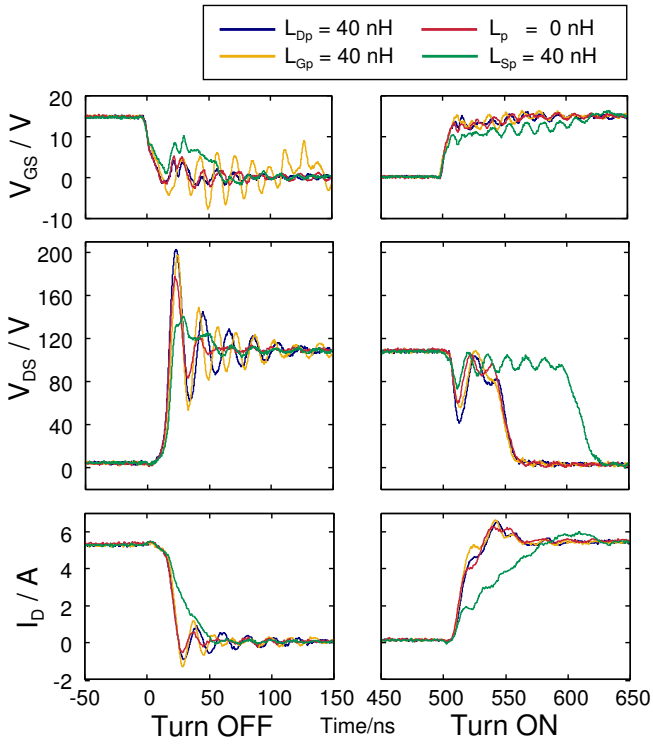


Fig. 7: Switching waveforms.

From Figs. 9 (c) and (d), the inductance near the gate and drain terminals L_{Gp}, L_{Dp} enlarge ringing V_{DSring}, while they give little influence on switching time T_{ON}, T_{OFF} and energy loss E_{Loss}.

V_{DSring} increases by 30.2% with 40 nH of L_{Gp} due to LC resonance between parasitic inductance and input capacitance C_{iss} of the MOSFET. Fig. 10 shows the gate-side impedance curves when L_{Gp} = 0, 20, 40 nH. The impedance consists of C_{iss}, parasitic inductance and capacitance in the gate side loop in series. C_{iss} of the DUT is 463 pF, and internal parasitic capacitance in the gate driver Si8234BB is 370 pF. Note that impedance also contains extra parasitic inductance of 16 nH which is composed of PCB wiring inductance, parasitic inductance of the MOSFET and gate-driver IC package and socket. High parasitic inductance bring resonance frequency fr close to 1 MHz of fundamental frequency and ringing tends

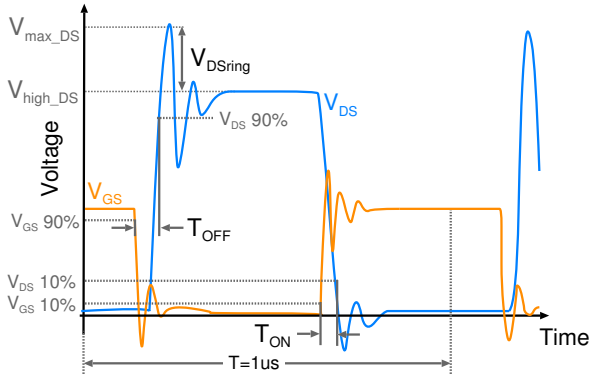
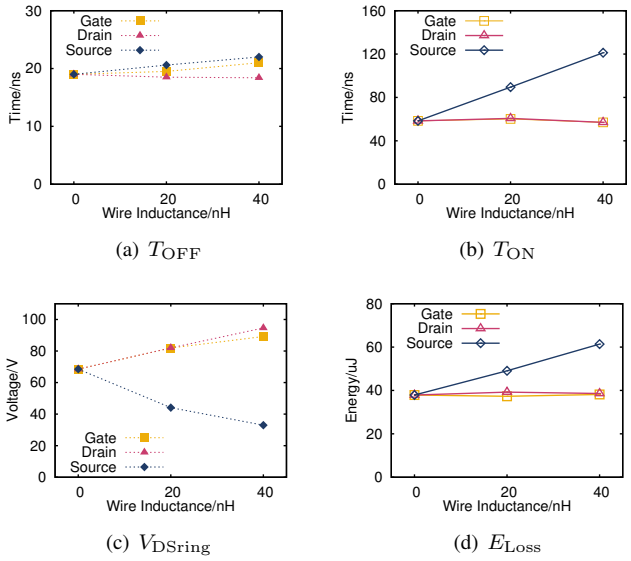


Fig. 8: Definitions for parameters.



(a) T_{OFF} (b) T_{ON}

(c) V_{DSring} (d) E_{Loss}

Fig. 9: Wiring inductance dependence of switching characteristics.

to be significant. For instance, Fig. 10 indicates fr is around 50 MHz at L_{Gp} = 40 nH while Fig. 7 shows ringing frequency of V_{GS} waveform is around 60 $\sim$ 70 MHz after turn OFF. From the results, the ringing on V_{GS} comes from the LC resonance and affects the V_{DS}.

V_{DSring} increases by 38.1% with 40 nH of L_{Dp} due to voltage fluctuation at L_{Dp}. Voltage drop across L_{Dp} occurs while I_{D}fall-slope changes at turn OFF following Eq. (1). As the voltage drop depends on L_{Dp}, large L_{Dp} would increase V_{DSring}.

In contrast, the inductance near the source terminal L_{Sp} enlarges switching time, and energy loss which is correlated with T_{ON}. T_{ON} increases by 108% and E_{Loss} correlatively increases by 62.0% with 40 nH of L_{Sp}. L_{Sp} keeps the source voltage V_{s} high against the ground during turn ON as shown in Fig. 11(b). It disturbs rising up of V_{GS} and slows down the rise of I_{D} as shown in Fig. 7. Thus T_{ON} increases more than twice with 40 nH of L_{Sp}. On the other hand V_{DSring} decreases by 51.8% with 40 nH of L_{Sp} owing to the decrease in transient speed of I_{D}. The decrease in the speed is caused in the same theory of turn ON period as shown in Fig. 11(a), and it leads V_{DSring} to small following Eq. 1.

Finally we explain the cause of depression at V_{DS} during turn ON as shown in Fig 7. Fig 12 shows the enlargement of the depression. Note that the level of depression depends on the parasitic inductance location, and is large in the order of L_{Dp} = 40 nH, L_{Gp} =40 nH, L_{P} = 0 nH and L_{Gp} = 40 nH. It

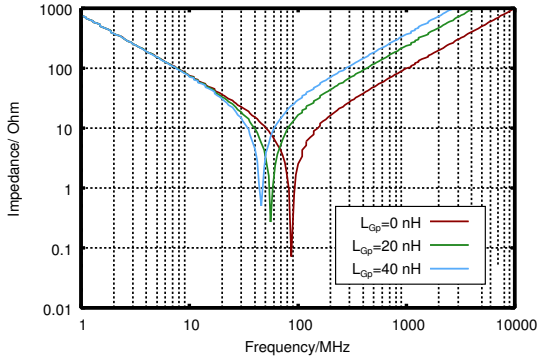
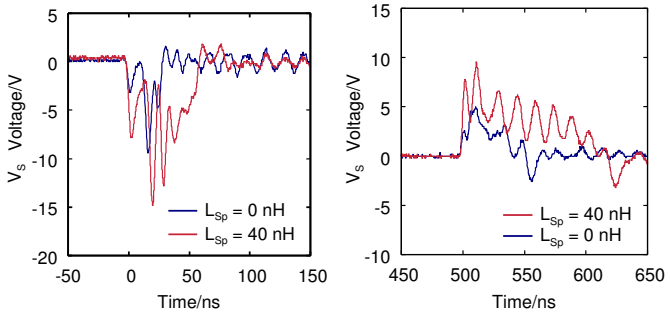


Fig. 10: Gate impedance versus Frequency.



(a) Turn OFF (b) Turn ON

Fig. 11: Source voltage comparison.

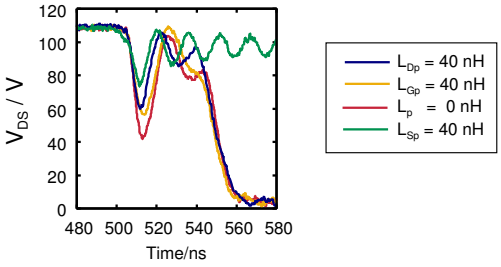


Fig. 12: Enlargement - V_{DS}turn ON characteristics.

is caused by the parasitic inductance near the drain and source terminal. It is the same theory as explained in the discussion part of L_{Dp}.

IV. Ringing Suppression by RCD Snubber Considering Location of Wiring Inductance

A. Measurement setup

We evaluate how RCD snubber suppress ringing induced by wiring inductance. Fig. 13 shows the measurement circuit.

For high frequency operation, it is necessary to select diodes with superior reverse recovery characteristics such as schottky-structure diodes. C3D04060F (CREE), which is a SiC-SBD (Schottky Barrier Diode), is used as a snubber diode D_{snub}. Snubber resistor R_{snub} of 15 Ω and capacitor C_{snub} of 470 pF are used in the measurement. The RC parameter is designed based on [8], and adjusted with the circuit simulator SIMetrix. Switching characteristics are measured with L_{Gp}, L_{Dp}, or L_{Sp} of 40 nH. The other measurement conditions are same as Sect. III-A.

B. Results and Discussion

The switching waveforms and the evaluation results are shown in Fig. 14 and Table II. Note that E_{Loss} includes the energy losses in the DUT, the snubber resistor R_{snub} and the snubber diode D_{snub} per cycle when the RCD snubber is attached (w/ snub). The detail of measured E_{Loss} is shown in table III.

When L_{Gp} = 40 nH or L_{Dp} = 40 nH, the snubber suppresses ringing V_{DSring} of 53.9% at L_{Gp} = 40 nH, 63.1% at L_{Dp} = 40 nH. The snubber has small influence on switching time and energy loss. The energy loss of SiC-MOSFET E_{MOSFET} is slightly reduced owing to suppression of the ringing by the snubber. The increase of E_{Loss} due to snubber elements R_{snub}

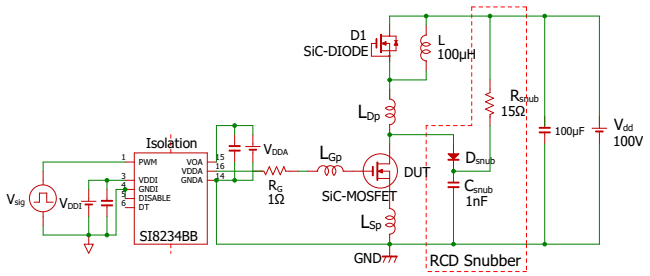
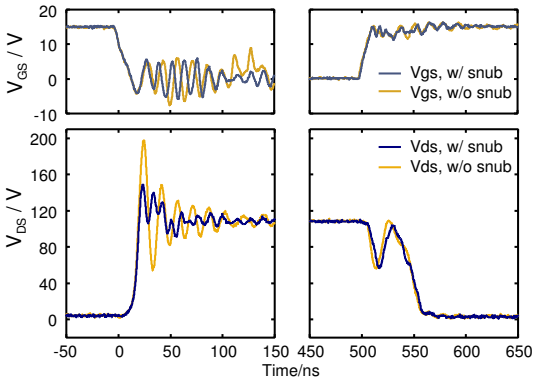


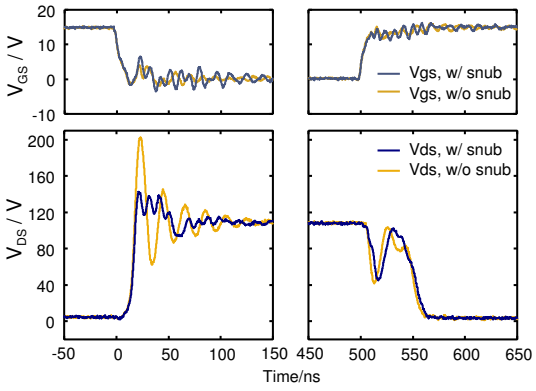
Fig. 13: Evaluation of ringing suppression by RCD snubber.

TABLE II: Comparison of switching characteristics.

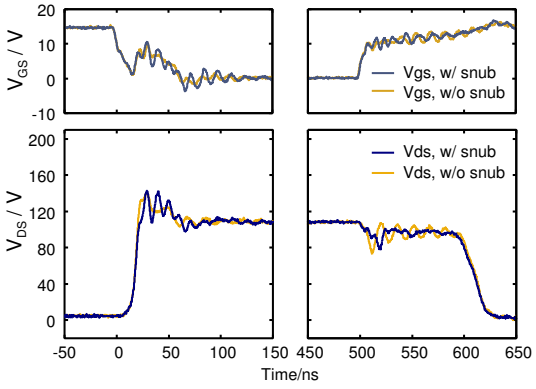
	L_{Gp} = 40 nH			L_{Dp} = 40 nH			L_{Sp} = 40 nH		
	T_{ON}	V_{DSring}	E_{Loss}	T_{ON}	V_{DSring}	E_{Loss}	T_{ON}	V_{DSring}	E_{Loss}
w/o snub	57.0 ns	89.2 V	38.2 μJ	57.0 ns	94.6 V	38.6 μJ	121.2 ns	33.0 V	61.4 μJ
w/ snub	57.9 ns	41.1 V	38.2 μJ	60.1 ns	34.9 V	40.2 μJ	120.0 ns	34.7 V	63.6 μJ



(a) L_{Gp} = 40 nH



(b) L_{Dp} = 40 nH



(c) L_{Sp} = 40 nH

Fig. 14: Switching waveforms.

and D_{snub} are within 5%. However, as shown in Fig. 14 (a), the snubber is not enough to suppress ringing on V_{GS} caused by L_{Gp}, which may cause malfunction or breakdown.

In case of L_{Sp} = 40 nH, the RCD snubber does not suppress ringing. V_{DSring} increases by 5.2%. Moreover, E_{Loss} increases by 3.7% because of the energy losses in R_{snub} and C_{snub} as shown in Table II, although T_{ON} decreases by 1.0%.

TABLE III: Detail of energy loss.

	Energy loss [μJ]		
	E_{MOSFET}	E_{Rsnub}	E_{Dsnub}
L_{Gp} = 40 nH	35.0	2.17	0.98
L_{Dp} = 40 nH	36.93	2.00	1.23
L_{Sp} = 40 nH	61.58	1.37	0.69

$E_{\mathrm{Loss}} = E_{\mathrm{MOSFET}} + E_{\mathrm{Rsnub}} + E_{\mathrm{Dsnub}}$

V. Optimal Design of RCD Snubber

From the measurement results, an optimal RCD snubber design for MHz-switching of SiC-MOSFET is summarized as follows.

1) Wiring inductance near the gate and drain terminals L_{Gp}, L_{Dp} should be considered in the calculation of the RC parameters, while L_{Sp} can be ignored. It is because L_{Gp} and L_{Dp} induce ringing.

2) Wires near the gate and source terminals should be shortened as much as possible. L_{Sp} prolongs turn ON time T_{ON}, which also increases E_{Loss}. Large L_{Sp} disturbs high-frequency operation. L_{Gp} may cause malfunction or breakdown due to the increase of ringing on V_{GS}, which cannot be suppressed by the RCD snubber circuit.

VI. Conclusion

We addressed an optimal design of the RCD snubber for MHz-switching of SiC-MOSFET considering location of wiring inductance. We investigated influence of wiring inductance on switching and the ringing suppression by the RCD snubber. The measurement results indicate (i) wires near the gate and source terminals should be minimized as much as possible. For instance, 40 nH of inductance near the source terminal increases switching time by 2.08x. (ii) Parasitic wiring inductance near the gate and drain terminals L_{Gp} ,L_{Dp} must be considered to design an optimal RCD snubber. For instance, the RCD snubber suppress ringing of 53.9%, 63.1% caused by L_{Gp} ,L_{Dp} respectively.

Acknowledgment

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