Impact of Random Telegraph Noise on CMOS Logic Circuit Reliability

Takashi Matsumoto
Department of Communications and Computer Engineering
Kyoto University, Kyoto, Japan
Email: tmatsumoto@vlsi.kuee.kyoto-u.ac.jp

Kazutoshi Kobayashi
Department of Electronics
Kyoto Institute of Technology, Kyoto, Japan

Hidetoshi Onodera
Department of Communications and Computer Engineering
Kyoto University, Kyoto, Japan

***Abstract*—The leading edge products have a feature size of 22 nm in 2014. Designing reliable systems has become a big challenge in recent years. Transistor reliability has a great impact on highly-reliable CMOS circuit operations. Random telegraph noise is one of major recent transistor reliability concerns. First, recent researches on RTN and its impact on circuits are briefly summarized. Then the impact of RTN on CMOS logic circuit reliability is described based on our results from 65 nm and 40 nm test chips. Circuit designers can change various parameters such as operating voltage, transistor size, number of logic stages and substrate bias. The impact of these parameters is clarified in view of RTN-induced CMOS logic delay uncertainty. The impact of RTN can be a serious problem even for logic circuits when they are operated under low supply voltage.**

I. Introduction

Physical feature size of a transistor has been reduced continually over time. Leading edge products have a feature size of 22 nm in 2014. Due to the device miniaturization, the number of transistors in one processor becomes as much as 4.31 billion in 2014[1]. On the other hand, designing reliable systems has become a big challenge in recent years[2], [3], [4], [5]. One of the dominant issues is a transistor performance variation. It can be classified into static variation and dynamic variation. Static variation is caused by LSI manufacturing process variation[6]. Dynamic variation is caused by an environmental noise and an intrinsic device noise. As an example of dynamic variation, jitter in oscillators can be caused by both environmental and intrinsic device noise[7], [8]. Another example of dynamic variation is an LSI performance fluctuation or a gradual LSI performance degradation. It is known as LSI reliability problems. In this paper, we deal with a reliability problem caused by intrinsic noise in transistor. It is well known today that Hot Carrier Injection (HCI), Bias Temperature Instability (BTI)[9], [10], Time Dependent Dielectric Breakdown (TDDB), and Random Telegraph Noise (RTN)[11] are main issues in transistor gate oxide reliability. Transistor reliability has a great impact on modern CMOS circuits[12] and the quality of the interface between gate oxide and silicon substrate is one of the key factors for highly-reliable circuit operations.

Nitridation process of gate oxide is widely used after 65 nm CMOS technologies. The increase of the nitrogen content at the SiO_2/Si interface promotes the Negative Bias Temperature Instability (NBTI)[13], [14]. When transistors degrade owing to NBTI, the propagation delay of combinational logics increases. The correct operation of a register may not be guaranteed under the gradual performance degradation by NBTI. A remarkable phenomenon regarding NBTI is that the degraded performance of a pMOS transistor recovers when the bias temperature stress applied to the gate oxide is removed or relaxed[15], [16], [17]. Despite the extensive research on NBTI, there is still a controversy over the NBTI mechanism due to its recovery phenomena[18], [19]. There is a strong demand for the practical compact model that can treat NBTI and other reliability issues at the circuit simulation level[20], [21]. It is indispensable for the compact model to monitor NBTI and other reliability issues at the circuit level[22].

RTN has attracted much attention in these years due to the continuous technology scaling. RTN appears as a temporal transistor performance fluctuation. It is reported that the impact of RTN-induced fluctuation may exceed manufacturing process variation in 22 nm technology[23]. RTN is considered to share some common mechanisms with NBTI because RTN is caused by the capture and emission of mobile charged carriers. This paper summarizes recent researches on RTN and introduces our results from 65 nm and 40 nm test chips.

Section II describes recent researches on RTN and its impact on circuits. Section III describes typical measurement results of RTN-induced transistor drain current fluctuation in a 65 nm CMOS technology. Section IV–VI describe the impact of RTN on CMOS logic circuit reliability followed by conclusion.

II. RTN and its Impact on Circuits

Low frequency noise or $1/f$ noise is observed in various systems[24]. As for LSI systems, $1/f$ noise can be observed as a drain current fluctuation in a transistor with moderately large gate area. On the other hand, RTN is observed in a small transistor with a few oxide traps. RTN is characterized by a $1/f^2$ spectrum that is called the Lorentzian power spectrum. One possible interpretation is that the superposition of various RTN (with a broad distribution of activation energies in RTN

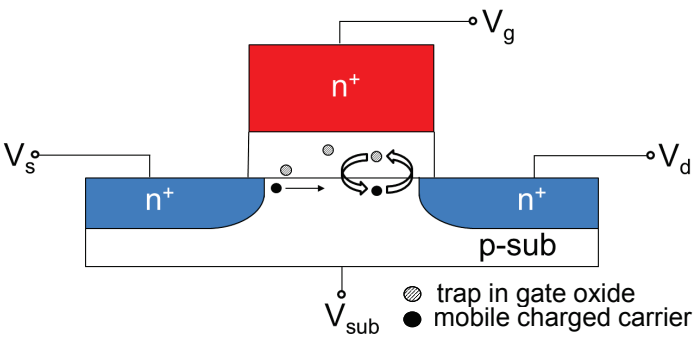

Fig. 1. Capture and emission of carriers by gate oxide traps (nMOS).

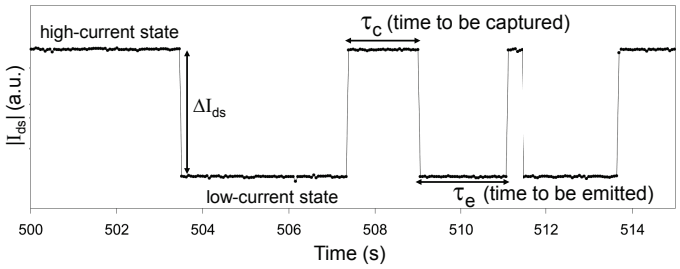

Fig. 2. RTN-induced drain current fluctuation in a pMOS.

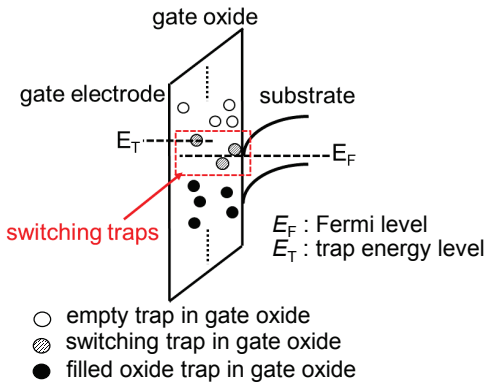

Fig. 3. Energy band diagram of an nMOS transistor.

process) generates $1/f$ noise[25]. Mobile charged carriers in a transistor channel can be trapped into or detrapped from oxide traps randomly (Fig. 1). The capture and emission of one carrier induces a two-state RTN. Figure 2 is the typical example of a measured drain current fluctuation in a commercial 40 nm CMOS transistor in our test chip that has a large two-state RTN. Time constants $\tau_{\rm c}$ and $\tau_{\rm e}$ are defined as the time when the drain current stays at high-current state (H-state) and low-current state (L-state) respectively. The fluctuation amplitude is defined as $\Delta I_{\rm ds}$. RTN is an intrinsically random phenomenon. The parameter such as $\tau_{\rm c}$, $\tau_{\rm e}$ and $\Delta I_{\rm ds}$ differ by transistor. Thus statistical characterization is required for the correct RTN modeling[26], [27], [28]. When a two-state RTN is measured for some period, distributions of $\tau_{\rm c}$ and $\tau_{\rm e}$ are obtained. The average of $\tau_{\rm c}$ and $\tau_{\rm e}$ is denoted as $\langle\tau_{\rm c}\rangle$ and $\langle\tau_{\rm e}\rangle$ respectively. We assume that the probability of a transition from H-state to L-state per unit time is given by $1/\langle\tau_{\rm c}\rangle$ and from L-state to H-state per unit time is given by $1/\langle\tau_{\rm e}\rangle$. $A(t)$ is defined as the probability that a transition from H-state to L-state does not happen after time t. Then,

$$A(t+{\rm d}t) = A(t)\left(1-\frac{{\rm d}t}{\langle\tau_{\rm c}\rangle}\right) \tag{1}$$

is obtained. Integrating Eq. (1) with $A(0)=1$,

$$A(t) = \exp(-t/\langle\tau_{\rm c}\rangle). \tag{2}$$

As a result, the probability, $P_{\rm H}(t)$, that the transition from H-state to L-state does not happen for time t, and then happens between time t and $t+{\rm d}t$ is given by

$$P_{\rm H}(t) = \frac{1}{\langle\tau_{\rm c}\rangle}\exp(-t/\langle\tau_{\rm c}\rangle). \tag{3}$$

Equation (3) shows that the time constant, $\tau_{\rm c}$ and $\tau_{\rm e}$, follow exponential distributions. It is shown later experimentally that time constants actually follow exponential distribution both for a two-state drain current fluctuation (Section 3) and for a two-state logic delay fluctuation (Section 5).

The capture and emission of a carrier also induces the threshold voltage fluctuation, $\Delta V_{\rm th}$. It is approximately expressed as

$$\Delta V_{\rm th} = \frac{e}{LWC_{\rm ox}}, \tag{4}$$

where L is the gate length, W is the gate width, $C_{\rm ox}$ is the gate capacitance per unit area, and e is the elementary charge. Equation (4) shows the impact of one charged carrier on $\Delta V_{\rm th}$ becomes larger as the gate area shrinks. When the operating voltage of a circuit decreases, the impact of $\Delta V_{\rm th}$ also becomes larger. Recent studies show that $\Delta V_{\rm th}$ caused by RTN grows more rapidly than the threshold variation caused by random dopant fluctuation. It is reported that RTN-induced $\Delta V_{\rm th}$ may exceed RDF-induced threshold variation at the 3 σ level in 22 nm technology[23]. Figure 3 shows the energy band diagram of an nMOS transistor. The Fermi level is denoted by $E_{\rm F}$ and the trap energy level is denoted by $E_{\rm T}$. Traps below $E_{\rm F}$ (filled circle) are filled and above $E_{\rm F}$ (open circle) is empty. Several traps close to $E_{\rm F}$ can act as switching traps. The $\langle\tau_{\rm c}\rangle/\langle\tau_{\rm e}\rangle$ ratio follows

$$\frac{\langle\tau_{\rm c}\rangle}{\langle\tau_{\rm e}\rangle} = \exp\left(\frac{E_{\rm T}-E_{\rm F}}{k_{\rm B}T}\right), \tag{5}$$

where $k_{\rm B}$ is the Boltzmann constant and T is temperature. When one switching trap exists, 2-state discrete drain current fluctuation is observed. If there are n switching traps, 2^n-state discrete fluctuation can be observed.

RTN in transistors is a critical issue not only for analog/RF circuits but also for digital circuits. RTN already has a serious impact on CMOS image sensors[29], flash memories[30], and SRAMs[31], [32], [33]. These circuits use small size device and the integration density is extremely high.

Recently we have reported that RTN also induces performance fluctuation to logic circuits[34]. The impact of RTN can be a serious problem even for logic circuits when they are operated under low supply voltage[35]. Circuit designers can change various parameters such as operating voltage, transistor size, number of logic stages, logic gate type and substrate bias. However, the impact of such parameters on RTN is not well understood at the circuit level[36]. This impact is clarified based on our measurement results in Section VI.

Fully-depleted SOI (FD-SOI) MOSFETs are one of the attractive devices for the present and the future planar CMOS technology[37]. As one of the FD-SOI devices, the Silicon On Thin Buried oxide (SOTB) are being developed because of the superior device characteristics for ultra-low voltage operations and the suppression of device variability caused by dopant fluctuation[38]. RTN amplitude is also considered to be suppressed by FD-SOI MOSFETs compared to bulk MOSFETs because large channel potential fluctuation in the bulk device is suppressed in the FD-SOI device[39]. Multi-gate transistors such as tri-gate device are also attractive and have already been applied to the advanced SoC in 22 nm technology[40]. RTN in multi-gate device and its impact on circuit will further be investigated in the future[41], [42].

In the following section, the impact of RTN on CMOS logic circuit reliability is described based on our measurement results from 65 nm and 40 nm test chips.

III. Transistor Drain Current Fluctuation by RTN

This section describes typical measurement results of RTN-induced transistor drain current fluctuation with respect to gate bias and substrate bias dependency. A CMOS transistor array fabricated in a commercial 65 nm CMOS technology is used. All measurements are done at room temperature. Figure 4 shows the RTN-induced nMOS drain current ($I_{\rm ds}$) fluctuation of a single transistor for various gate biases ($V_{\rm gs}$). The current integration time is 5 ms for $V_{\rm gs} = 0.4$V, 0.5V and 500 μs for $V_{\rm gs} \geq 0.6$V. When $V_{\rm gs}$ is increased from 0.6 V to 0.8 V, the two-state switching becomes more frequently but it disappears at 1.2 V. It indicates the gate bias gives a big influence on RTN. The power spectral density (PSD) of Fig. 4 is obtained by quantizing the measurement data into the 2-state waveform. Lorentzian power spectrum is obtained for $V_{\rm gs} = 0.4$V, 0.6V, 0.7V and 0.8V (Fig. 5). The large two-state switching disappears for $V_{\rm gs} = 1.2$V and only a high frequency noise with small amplitude remains. Lorentzian power spectrum is not obtained for $V_{\rm gs} = 0.5$V, because a frequent but a small two-state fluctuation and a large sharp fluctuation are superposed.

Figure 6 shows time constant ($\tau_{\rm c}$, $\tau_{\rm e}$) distributions of Fig. 5 for $V_{\rm gs} = 0.8$V. It is found that both distributions follow exponential distribution ($e^{-t/\langle\tau\rangle}$) and Eq. 3 is confirmed. Finally, $I_{\rm ds}$ fluctuation for various substrate biases ($V_{\rm sub}$) are shown in Fig. 7 at $|V_{\rm gs}| = 0.9$V. The minus and plus signs in $V_{\rm sub}$ represent reverse bias and forward bias respectively. The large two-state RTN is observed for each $V_{\rm sub}$. $I_{\rm ds}$ stays at the high-current state most of the time when the substrate is reverse-biased ($V_{\rm sub}$: -0.4V), while it stays at the low-current state most of the time when the substrate is forward-biased ($V_{\rm sub}$: $+0.4$V). $I_{\rm ds}$ stays almost equally at both states for the zero substrate bias case ($V_{\rm sub}$: 0V). It suggests that RTN time constants can be strongly influenced by the substrate bias.

From these measurement results, we are afraid that RTN-induced transistor current fluctuation can be strongly influenced by both the gate bias and the substrate bias.

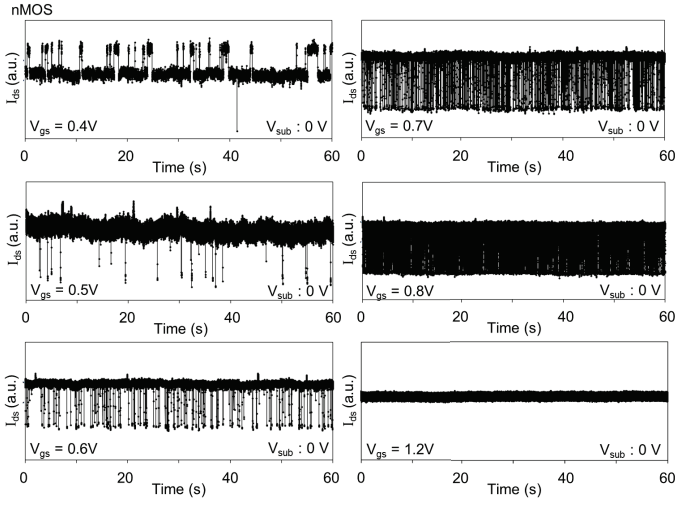

Fig. 4. RTN-induced nMOS drain current fluctuation of one transistor for various gate biases.

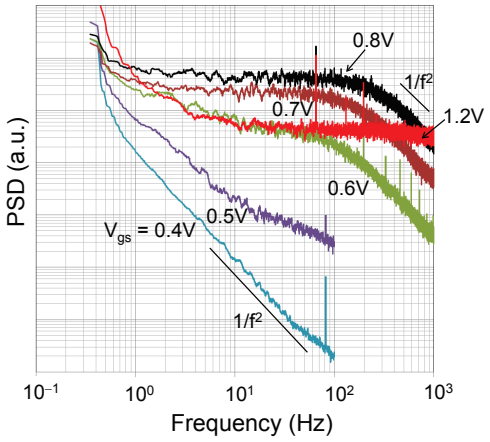

Fig. 5. Power spectral density of Fig. 4.

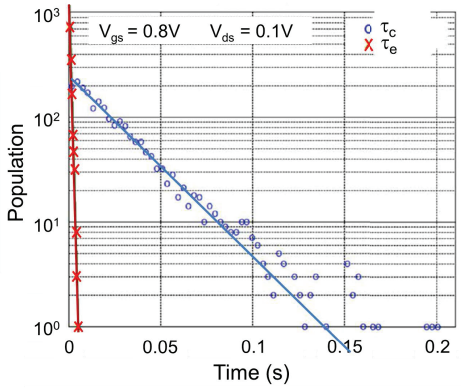

Fig. 6. Time constant distribution of Fig. 4 ($V_{\rm gs} = 0.8$ V).

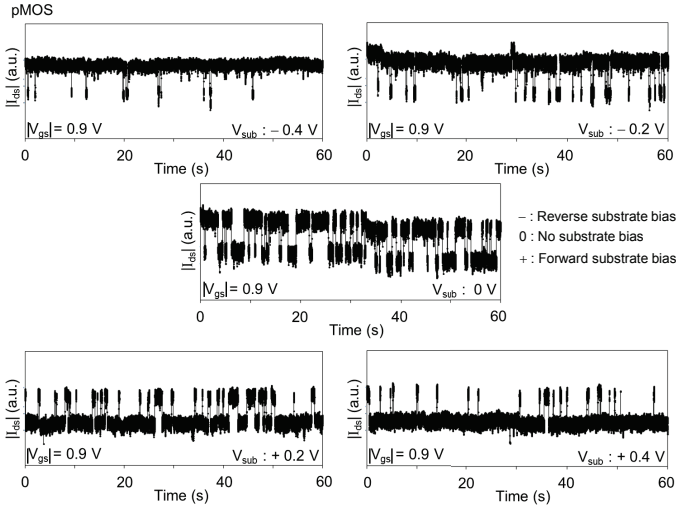

Fig. 7. RTN-induced pMOS drain current fluctuation of one transistor for various substrate biases.

IV. Test Structure for RTN Evaluation

In this section, a test structure for the statistical characterization of RTN-induced logic delay fluctuation is described. A logic path exists between two registers in a typical synchronous circuit structure (Fig. 8). Figure 9 shows the simplest test structure that can emulate the synchronous circuit operation of Fig. 8. Combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. All logic gates except NAND2 with EN input are homogeneous in this paper. Sequential circuit operation is emulated by D flip-flop (DFF) toggled by the RO output. The power supply for RO ($\mathrm{VDD_{RO}}$) and DFF ($\mathrm{VDD_{DFF}}$) can be independently supplied. We can also control the substrate bias for pMOS and nMOS. Figure 10 shows the whole test structure for the RTN measurement.

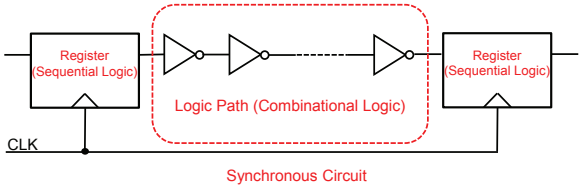

Fig. 8. Typical synchronous circuit structure.

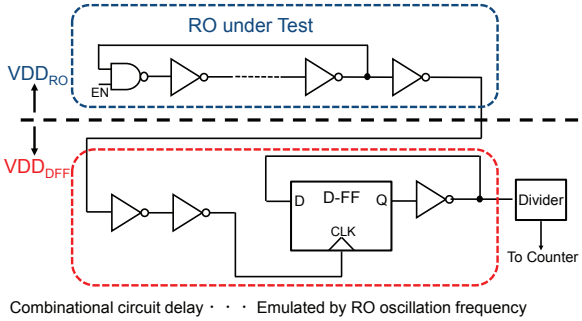

Fig. 9. Simplest test structure that can emulate the synchronous circuit operation.

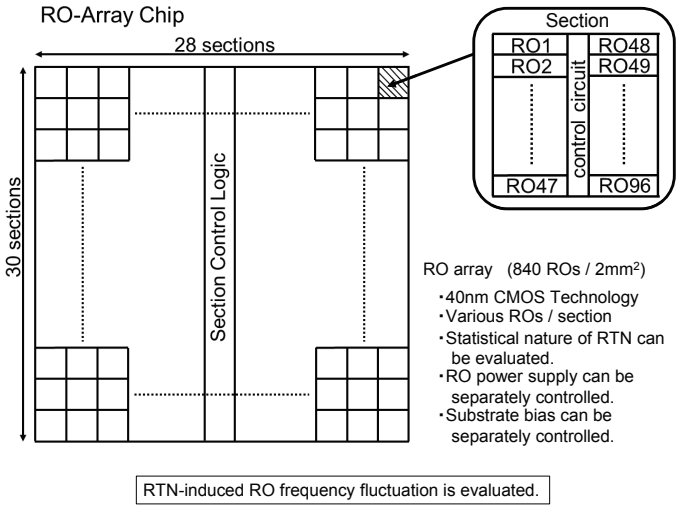

Fig. 10. Whole test structure for RTN measurement. One test structure contains 840 ROs.

RTN-induced delay fluctuation is measured by the RO frequency fluctuation. Various types of ROs are included in one circuit unit, which is called a section as depicted in Fig. 10. There are 840 sections with the same structure on 2 $\mathrm{mm^2}$ area. The statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at room temperature.

V. Measurement Results of Logic Delay Fluctuation

Figure 11 (a) shows the measurement result of the oscillation frequency of a 7-stage RO for about 80 s at $\mathrm{VDD_{RO}}$ =0.65V. The size of the inverter (INV) is smallest in this technology. The body bias for pMOS ($V_{\mathrm{bs\text{-}pMOS}}$) and nMOS ($V_{\mathrm{bs\text{-}nMOS}}$) are set to 0V. Measurement results show the large step-like frequency fluctuation. Here, $F_{\max}$ is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation as shown in Fig. 11(a). $\Delta F/F_{\max}$ is a good measure for the impact of RTN-induced frequency fluctuation for logic delay. It is 10.4% for one RO (Fig. 11(a)). However, significant fluctuation is not observed for another RO (Fig. 11(b)). Although large fluctuation such as Fig. 11(a) is a rare event, it has a large impact on circuit performance. Figure 12 shows typical measurement data of a 7-stage RO at $\mathrm{VDD_{RO}}$=0.65V where a large 2-state fluctuation is observed. Time constants τ_{c} and τ_{e} represent the time when the RO stays at high-frequency state and low-frequency state respectively. The PSD of Fig. 12 is obtained by quantizing the measurement data of Fig. 12 into the 2-state waveform.

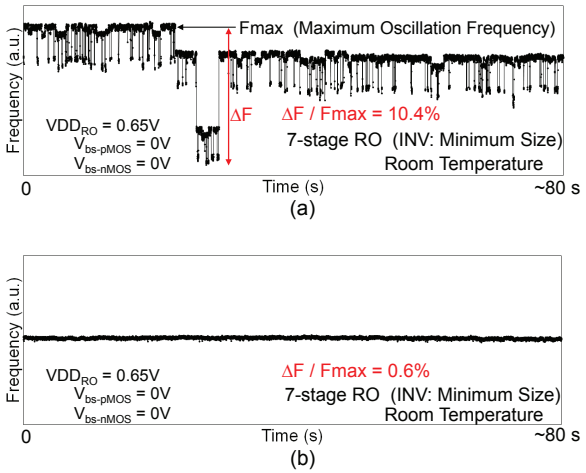

Fig. 11. Measurement result of RTN-induced RO frequency fluctuation. (a) $\Delta F/F_{\max} = 10.4\%$ (b) $\Delta F/F_{\max} = 0.6\%$.

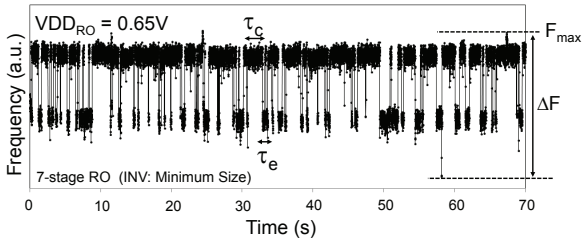

Fig. 12. Measurement results that shows 2-state fluctuation.

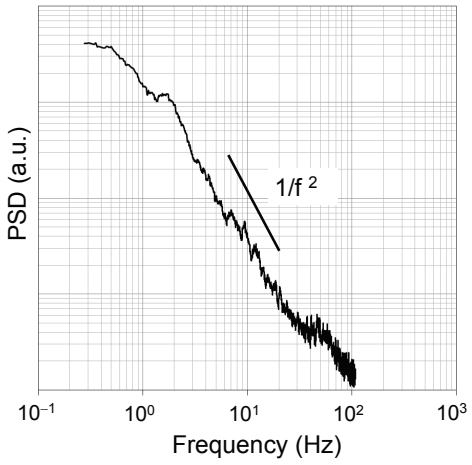

Fig. 13. Power spectral density of Fig. 12.

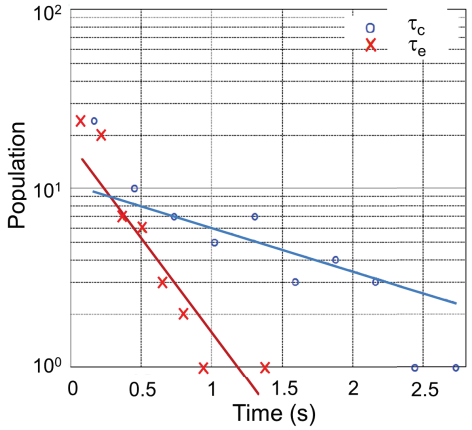

Fig. 14. Time constant distribution of Fig. 12.

Figure 13 shows Lorentzian power spectrum obtained from Fig. 12. Figure 14 shows time constant (τ_c, τ_e) distributions of Fig. 12. It is found that both distributions for τ_c and τ_e follow exponential distribution ($e^{-t/\tau}$). Lorentzian PSD and $e^{-t/\tau}$ distribution are observed for the case of a transistor where a single defect causes RTN fluctuation (Fig. 4, 5 and 6). It indicates that RTN fluctuation of Fig. 12 is caused by a single defect in a specific transistor in the 7-stage RO.

VI. Impact of RTN on Logic Circuit Reliability

In this section, the impact of RTN on logic circuit reliability is described. The distribution of RO frequency ($F_{\max}$) variation for 7-stage ROs follows a normal distribution when data are collected from the whole test structure of Fig. 10 over 15 chips (12,600 ROs) at 0.65V operation (Fig. 15). The distribution of $\Delta F/F_{\max}$ for the same ensemble follows a log-normal distribution above 50% level in CDF (Fig. 16). The maximum value of $\Delta F/F_{\max}$ becomes 16.8%. It is found that a small number of samples have a large RTN-induced fluctuation. If $\Delta F/F_{\max}$ follows log-normal distribution up to 6σ level, $\Delta F/F_{\max}$ becomes as much as 60%. Our results suggest the impact of RTN-induced fluctuation compared with the frequency variation caused by manufacturing process increases. When the supply voltage decreases, the impact

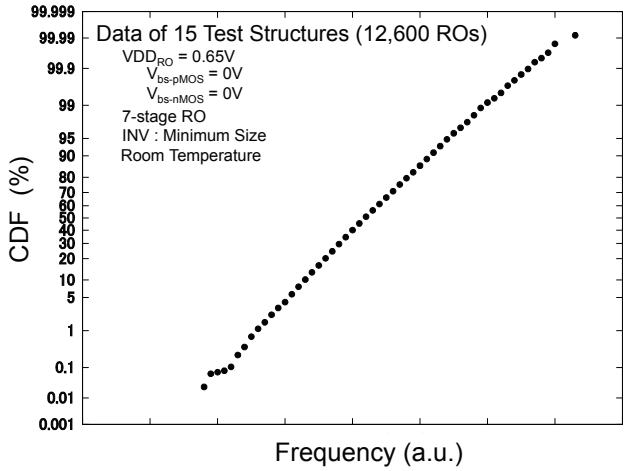

Fig. 15. Normal distribution plot of RO frequency ($F_{\max}$) variation caused by process variation.

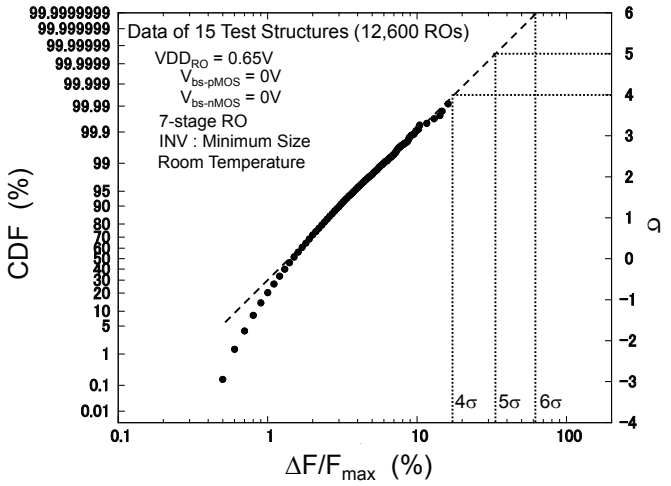

Fig. 16. CDF plot of RO frequency fluctuation ($\Delta F/F_{\max}$) using the same ensemble of Fig. 15 which follows log-normal distribution.

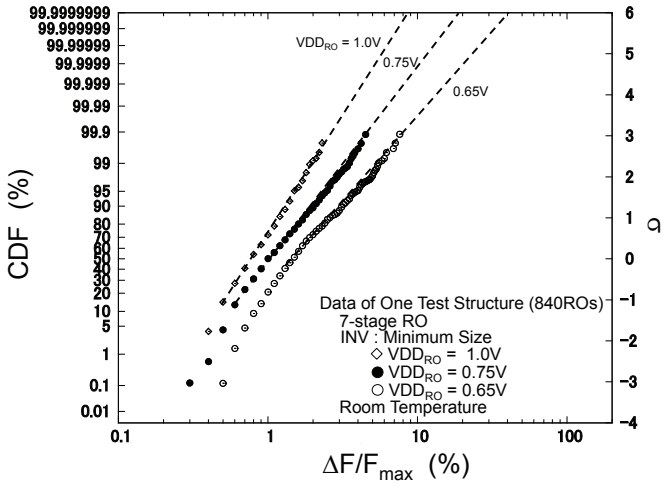

Fig. 17. CDF plot of $\Delta F/F_{\max}$ for various $\mathrm{VDD_{RO}}$ which follows log-normal distribution.

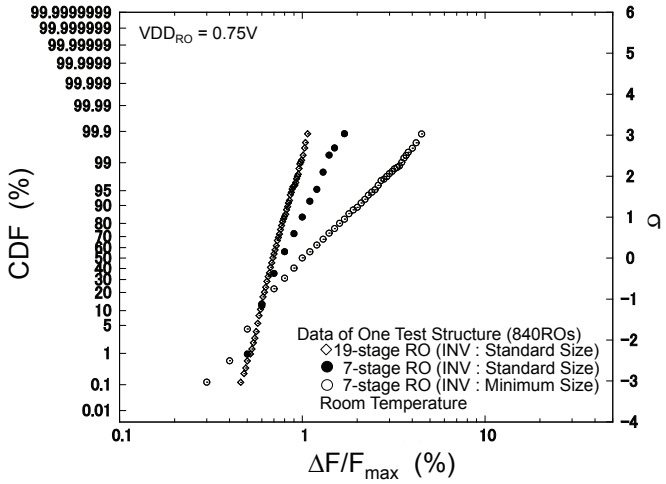

Fig. 18. The impact of gate area and number of stages on $\Delta F/F_{\max}$.

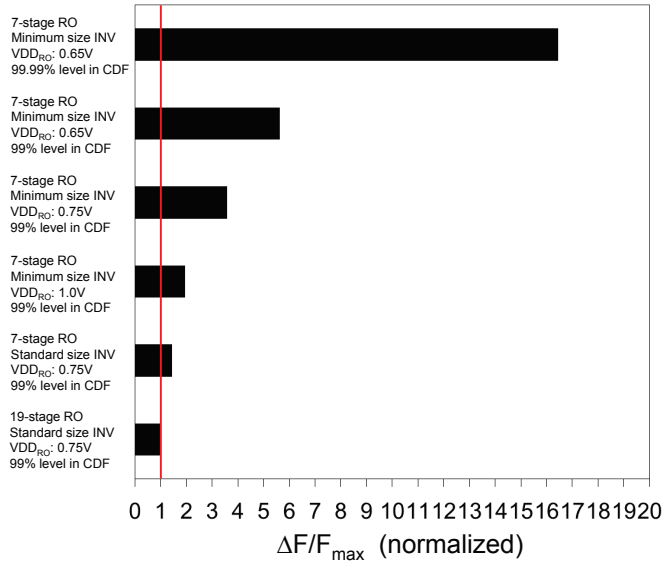

Fig. 19. The impact of supply voltage, gate area, and number of stages on $\Delta F/F_{\max}$ (normalized).

of $\Delta V_{\rm th}$ caused by RTN becomes larger (Fig. 17). Log-normal plot of $\Delta F/F_{\max}$ for $\mathrm{VDD_{RO}} = 1.0$V, 0.75V and 0.65V over the same 840 ROs indicates the rapid increase of $\Delta F/F_{\max}$ towards lower $\mathrm{VDD_{RO}}$. The impact of RTN also becomes larger as the gate area shrinks and the number of stages decreases. Figure 18 indicates more than 50% reduction of $\Delta F/F_{\max}$ (at 95% level in CDF) can be achieved by increasing the INV size for 7-stage RO under 0.75V operation. Here, the ratios of pMOS and nMOS gate areas ($W \times L$) of the minimum size INV to the standard size INV are 0.21 and 0.30 respectively. Figure 18 also shows that the impact of RTN becomes larger as number of stages decreases from 19-stage to 7-stage. The impact of supply voltage, gate area and number of stages on $\Delta F/F_{\max}$ is summarized in Fig. 19. The impact of RTN is drastically reduced by increasing supply voltage, gate area and number of stages.

An adaptive substrate bias control has been widely used to compensate for die-to-die parameter variations[43]. However, the impact of the substrate bias on RTN at the circuit level has not been well understood. It is already described in section III (Fig. 7) that the RTN time constant can be affected by the substrate bias. Figure 20 shows the measurement results of frequency fluctuation of one RO for 60 s under three substrate bias conditions. For this sample, the time constant is modulated considerably only when the pMOS substrate bias is changed from 0V to +0.2V (middlemost figure). Then PSD for the same sample of Fig. 20 for five substrate bias conditions are calculated (Fig. 21). When the pMOS substrate bias is changed from 0V to +0.2V (c, e), the large two-state fluctuation rarely happens ($\tau_{\rm c} \gg \tau_{\rm e}$). We observe the effect of one trap at the pMOS transistor in the RO that induces large noise at the circuit level (a, b, d). Figure 22 shows the frequency fluctuation of RO location (section No.) 1 for three substrate bias conditions. Four-state fluctuation due

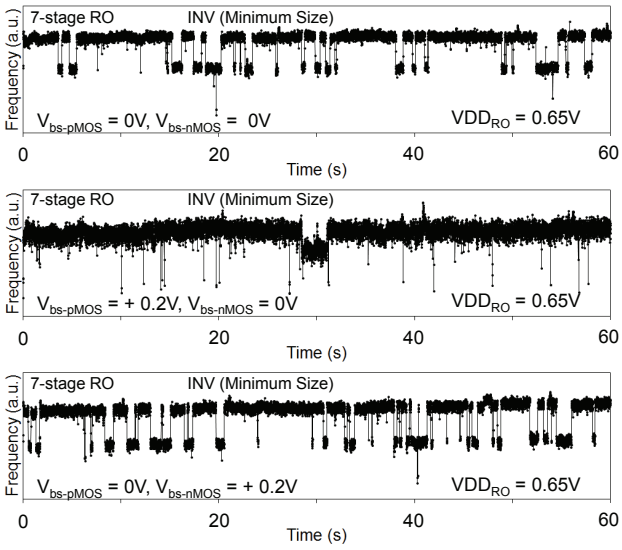

Fig. 20. RTN-induced RO frequency fluctuation for three substrate bias conditions.

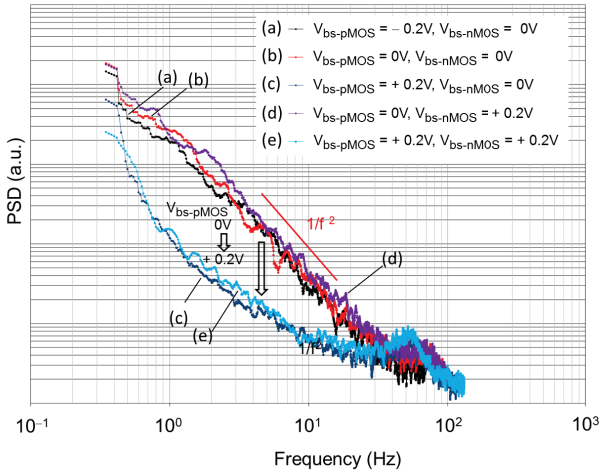

Fig. 21. PSD of RTN-induced RO frequency fluctuation for five substrate bias conditions.

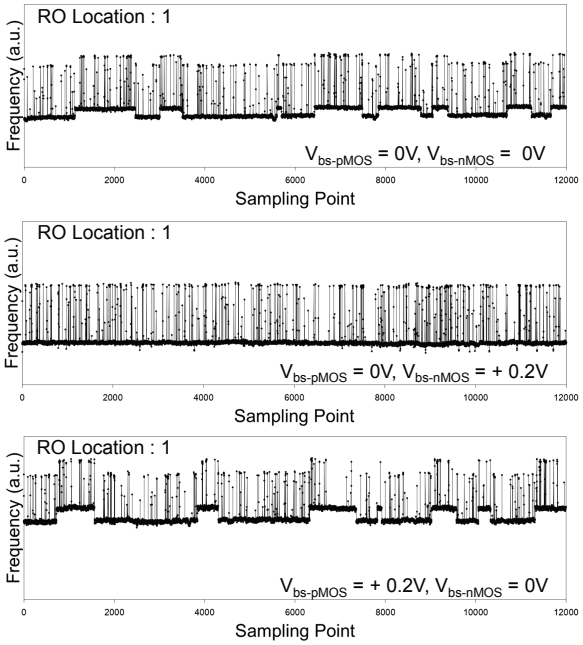

Fig. 22. RTN-induced RO frequency fluctuation for three substrate bias conditions (RO Location 1).

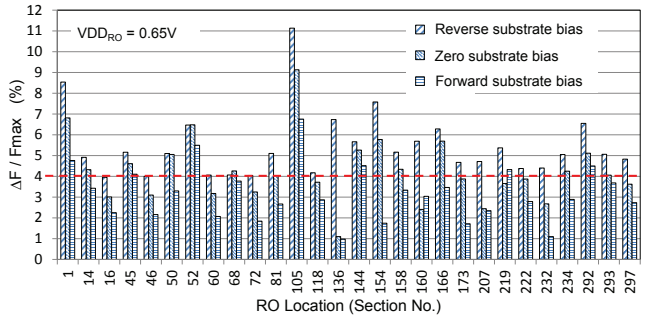

Fig. 23. $\Delta F/F_{\max}$ of different ROs for three substrate bias conditions. RO that have more than 4% fluctuation at reverse substrate bias case are shown.

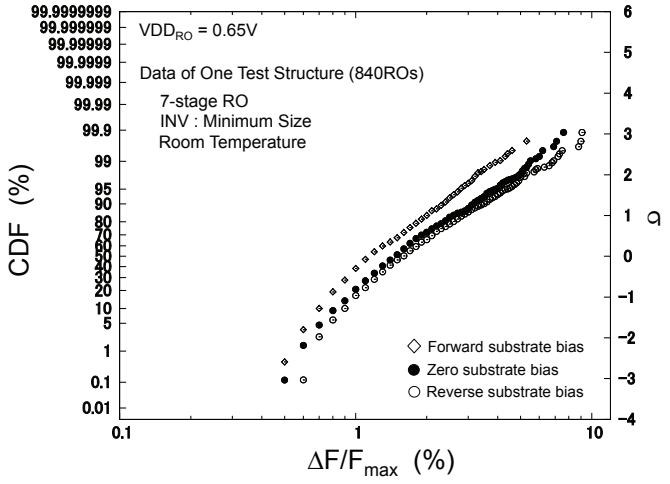

Fig. 24. Log-normal distribution plot of $\Delta F/F_{\max}$ for one test structure under three substrate bias conditions.

to two traps is clearly observed for the zero substrate bias ($V_{\text{bs-pMOS}} = 0$ V, $V_{\text{bs-nMOS}} = 0$ V) case. The effect of one of two traps disappears only when nMOS transistor is forward biased by 0.2 V (middlemost figure). The disappeared two-state fluctuation is caused by a single trap in a specific nMOS transistor in the RO.

Finally, the statistical result of the impact of RTN on logic delay fluctuation is described. Substrate bias conditions are categorized as the reverse bias case ($V_{\text{bs-pMOS}} = -0.2$ V, $V_{\text{bs-nMOS}} = 0$ V), zero bias case ($V_{\text{bs-pMOS}} = 0$ V, $V_{\text{bs-nMOS}} = 0$ V), and forward bias case ($V_{\text{bs-pMOS}} = +0.2$ V, $V_{\text{bs-nMOS}} = +0.2$ V). To evaluate the forward body-bias effect on large $\Delta F/F_{\max}$ samples, ROs that have more than 4% fluctuation at the reverse bias case (28 ROs) are shown in Fig. 23. When substrate bias is changed from the reverse bias case to the forward bias case, $\Delta F/F_{\max}$ tends to decrease monotonically due to $F_{\max}$ increase. However, it does not decrease monotonically in the case of the RO location "68", "160" and "219" when substrate bias is changed from the reverse bias case to the forward bias case. It is because the impact of substrate bias on RTN appears individually by ROs. It must be considered when forward substrate bias is applied. Next, $\Delta F/F_{\max}$ for one test structure under three substrate bias conditions is plotted in log-normal way (Fig. 24). The impact of RTN-induced delay fluctuation can be statistically reduced by the forward substrate bias control.

VII. Conclusions

Recent researches on RTN and its impact on circuits are briefly summarized. Then the impact of RTN on CMOS logic circuit reliability is described based on our results from 65 nm and 40 nm test chips. From the drain current RTN measurements in the 65 nm chip, RTN-induced logic delay fluctuation can be strongly influenced by both the gate bias and the substrate bias. Statistical nature of RTN-induced delay fluctuation is described by measuring 12,600 ROs fabricated in a commercial 40 nm CMOS technology. RTN-induced delay fluctuation denoted by $\Delta F/F_{\max}$ becomes as much as 16.8% of the nominal oscillation frequency under low supply voltage (0.65V) operation. By increasing the transistor size from the minimum to the standard size, more than 50% reduction of $\Delta F/F_{\max}$ can be achieved at 95% level in CDF under 0.75V operation. RTN-induced delay fluctuation also decreases rapidly with increasing the supply voltage. The impact of RTN-induced delay fluctuation can be statistically reduced by the forward substrate bias control. From measurement results, $\Delta F/F_{\max}$ increases log-normally when the number of logic circuits increases. We conclude that the impact of RTN can be a serious problem even for logic circuits when they are densely integrated and operated under low supply voltage.

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