A 65nm Flip-Flop Array to Measure Soft Error Resiliency against High-Energy Neutron and Alpha Particles

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***Abstract*—We fabricated a 65nm LSI including flip-flop array to measure soft error resiliency against high-energy neutron and alpha particles. It consists of two FF arrays as follows. One is an array composed of redundant FFs to confirm radiation hardness of the proposed and conventional redundant FFs. The other is an array composed of conventional D-FFs to measure SEU (Single Event Upset) and MCU(Multiple Cell Upset) by the distance from tap cells.**

I. Introduction

Process scaling makes LSIs less reliable to SEU(Single Event Upset), SET(Single Event Transient) and MCU(Multiple Cell Upset) which are collectively called soft error. To protect FFs from SET and SEU, several redundant flip-flop structures are proposed such as BISER (DMR)[1]. BISER has two FFs with a small weak keeper for voting and it can prevent SEU and SET on a combinational circuit. However, they are very weak to an SET pulse from the C-elements. On the other hand, MCU is well known as a critical issue on SRAMs, since it cannot be recovered by ECC circuits[2]. Recently, so-called tapless standard cells are widely used to control well potentials[3]. In this structure, since tap cells are sparsely placed similar to SRAMs, MCU is also critical issue for the DMR.

In this paper, we show accelerated test results of soft error. Fig. 1 shows a chip micrograph in a 65nm CMOS bulk process. We have integrated these two FF arrays. The left side of the fabricated chip is composed of two types of redundant FFs, the conventional DMR FF and the proposed BCDMR FF[4] to compare soft error rate. The right side is filled with the FF array with conventional D-FFs to measure SEU and MCU.

II. BCDMR-FF

We have proposed the Bistable Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR-FF) as shown in Fig. 2. The conventional BISER (DMR) structure has one weak keeper after each latch pair, while the BCDMR duplicates C-elements to prevent multiple latches to be flipped by an SET pulse from the C-element. Table I compares area, delay and power of the DMR and proposed BCDMR FFs without delay element τ normalized by those of the conventional FF in a 65nm CMOS. BCDMR achieves same area and better power and delay at 0.5V compared with the DMR. It is mainly because its cross-coupled structure reduces the size of the C-element that must have enough strength to flip the weak keeper.

Fig. 3 shows the error rates of DMR and BCDMR according to the clock frequency of 1, 10 and 160MHz by alpha particle irradiation. This accelerated test was performed with an Americium 241 whose activity is 3.7MBq (= 100μCi). SEUs induced by a particle hit on storage are dominant at the lower clock, while SEUs induced by a particle hit on the C-element are dominant at the higher clock. The C-element on the DMR structure is vulnerable to soft errors at the higher clock. The proposed BCDMR FF exhibits 150x better error resiliency at 160MHz than the DMR FF with almost same or better area, delay and power. Due to the limitation of the PLL and clock network, our experiments are limited to 160MHz. But the error resiliency of the BCDMR is much better than the DMR according to the increase of the clock frequency.

III. FF Array to measure SEU and MCU

To investigate SEUs and MCUs on flip-flops, we implemented an array of flip-flops constructing a 84,000bit shift register composed of tapless standard cells in a 65nm bulk CMOS process. Fig. 4 shows the detailed layout and schematic structure of the FF Array. We use no global clock to simplify layout structure. Clock is injected from the tail of the shift register, while the serial shift-in signal is injected from the head. Clock signals for all FFs are serially connected from the tail to the head, which relieves very tight hold constraint of shift registers. The drawback of such layout structure is slower clock frequency. However, shift operations are required only when reading or writing registers. Slower clock does not affect anything on the soft error measurement.

Experiments by spallation white neutron beams were carried out at RCNP. During irradiation, the clock signal is fixed to 0 or 1 to keep master or slave latches in the latch state. Stored values of the FF Array are retrieved every 5 minutes. We have 520(=26chips$\times$20times) results for CLK=0 and 1 respectively.

Table II shows number of SEUs and MCUs from measurement results. Note that number of SEUs includes MCUs. In this result, Number of MCUs on slave latches are much less than that on master latches, since distances between the nearest transistors of the adjacent latches are 0.73μm for the master and 1.06μm for the slave. Longer distance results in larger resistance, which prevents bulk potentials from going up. Fig. 5 shows number of SEUs and MCUs according to the distance from tap cells. Number of MCUs on master latches at F0 is almost 50% of those at F1 and F2 and that on slave latches is 30% respectively. It is because that tap cells prevent lateral bipolar transistors at F0 from turning on to keep the bulk potentials to the ground level. Table III summarizes SEU and MCU rates on the master and slave latches. Those latches are more vulnerable when the tristate inverters (TM and TS) are vulnerable. It is because the feedback inverters (IM and IS) are stronger than the tristate inverters.

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IV. Conclusion

We fabricated a 65 nm LSI to measure soft error resilience by alpha particles and neutron irradiations. Alpha particle irradiation on the redundant-FF array reveals that the proposed BCDMR FF achieves 150x stronger than the conventional BISER FF at 160MHz clock frequency. Neutron irradiation on the conventional FF array reveals that the number of MCU highly depends on the distance from tap cells and distance between transistors, while the number of SEU is almost constant. To improve soft error resilience of redundant-FF, we should place latches and weak keeper sparsely or close to tap cell.

Acknowledgment: The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

References

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TABLE I
PERFOMANCE NORMALIZED TO CONV. FF.

	DMR	BCDMR
Area	3.00	3.00
D@1.2V	1.47	1.45
P@1.2V	2.15	2.20
D@0.5V	1.96	1.57
P@0.5V	2.39	2.23

TABLE II
TOTAL NUMBERS OF SEUS AND MCUS.

	Master	Slave
SEU	1205	1052
MCU	154	36

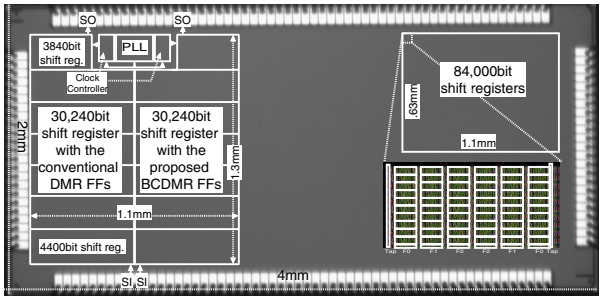

Fig. 1. Chip micrograph.

TABLE III
SEUS AND MCUS ACCORDING TO STORED VALUES IN MASTER OR SLAVE LATCHES BY NEUTRON BEAM IRRADIATION.

Vulnerable Latch	State	Vulnelable Gates	# of SEU (n/Mb/h)	# of MCU (n/Mb/h)
Master (CLK=1)	QM=0	TM	541	88
	QM=1	IM, TS	222	0
Slave (CLK=0)	QS=0	TS	493	19
	QS=1	IS	112	0

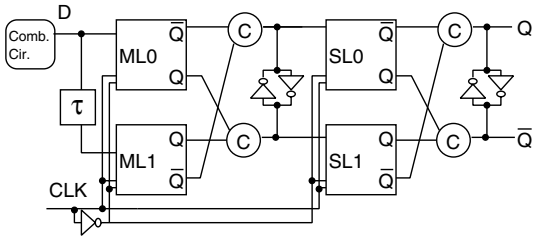

Fig. 2. BCDMR FF

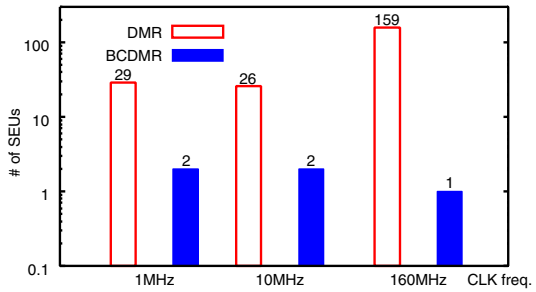

Fig. 3. Number of SEUs by clock freq. from 500 min. alpha particle irradiation.

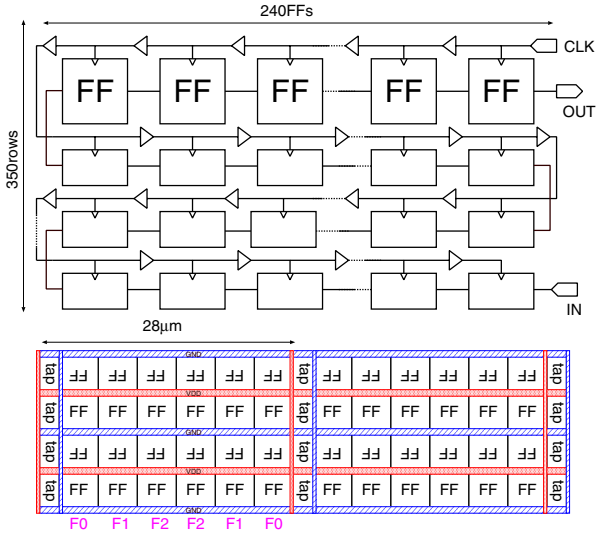

Fig. 4. Schematic and layout structure of the tapless shift register.

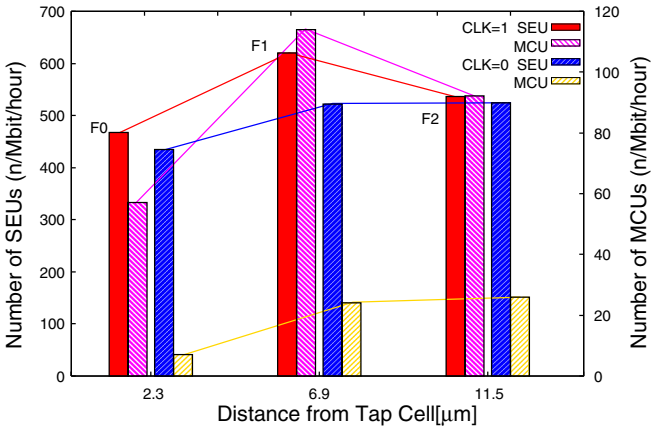

Fig. 5. Number of SEUs and MCUs per Mbit·hour according to the distance from tap cells.