Ring Oscillators with identical Circuit Structure to Measure Bias Temperature Instability

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***Abstract*—Ring oscillators (ROs) are frequently used to measure bias temperature instability (BTI). However, it is difficult to accurately compare the degradation rates of different BTI phenomenon because the parasitic components depend on circuit structures. The identical circuit structure with control signals is implemented to measure different BTI phenomenon. Test chips equipped with these ROs were fabricated in a 65 nm process. From the measurement results, well-known power-law models of BTI with time exponent *n* = 1/6 were extracted. The identical circuit structure can compare the BTI degradation rates of different BTI phenomenon based on the identical oscillation frequency.**

***Index Terms*—NBTI, PBTI, Ring Oscillator (RO), identical circuit structure**

I. Introduction

Miniaturization of integrated circuit elements brings advantages such as low power consumption and high-speed operation [1]. However, circuit reliability degradation due to aging phenomena such as bias temperature instability (BTI) has become an issue. The degradation phenomenon caused by BTI is noticeable in integrated circuits that are expected to be used for long periods of time. Degradation should be estimated during circuit design and design margins should be taken. In this study, BTI degradation was measured for 10,000 seconds in an accelerated test to compare the different degradation characteristics of MOSFETs. BTI degradation was measured from the oscillation frequency using ring oscillators (ROs). Applying high voltage under high temperature conditions accelerates degradation due to BTI.

This paper is organized as follows. Section II explains BTI. Section III shows the structures of those ROs. In section IV, measurement results are presented. Finally, section V shows our conclusion.

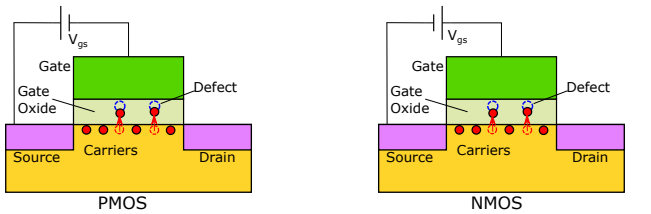
II. Bias Temperature Instability (BTI)

BTI is a phenomenon in which the characteristics of a MOSFET deteriorate due to stresses such as temperature and voltage [2]. BTI is caused by defects in the gate dielectric that trap carriers in the channel region, resulting in a decrease in the current in the channel region. Stresses such as temperature and gate-source voltage cause degradation of threshold voltage characteristics over time. Degradation of the threshold voltage causes current-voltage characteristic fluctuations, an increase delay time, and a decrease oscillation frequency. Removal of voltage or other stresses restores degraded characteristics, but not completely. There are two types of BTI: negative BTI (NBTI) which occurs in PMOS, and positive BTI (PBTI) which occurs in NMOS. Fig. 1 shows the bias conditions when NBTI in PMOS and PBTI in NMOS. NBTI occurs when the gate-source voltage is negative in PMOS ($V_{\rm gs} < 0$) and PBTI when the gate-source voltage is positive in NMOS ($V_{\rm gs} > 0$). The R-D Theory and the T-D Model have been considered the two most promising BTI generating principles [3], [4], but recently the universal model was proposed as a promising candidate [5]. The model equation for the degradation characteristic with respect to time t expresses the degradation of threshold voltage variation due to $t^{(1/6)}$.

III. Measurement Circuits

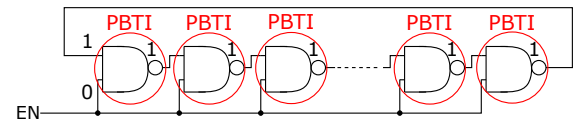
A. Conventional ROs with different circuit structures

In this paper, the BTI degradation rate is derived from the decrease of the oscillation frequency of ROs. The degradation rate of the threshold voltage is obtained by circuit simulations. Previous studies have measured the degradation rates of NBTI and PBTI using 11-stage NAND-gates ROs and 11-stage NOR-gates ROs [6]. PBTI becomes dominant in the RO composed of NAND-gates as shown in Fig. 2 (a). NBTI becomes dominant in the RO composed of NOR-gates as shown in Fig. 2 (b). The RO oscillates when the enable signal

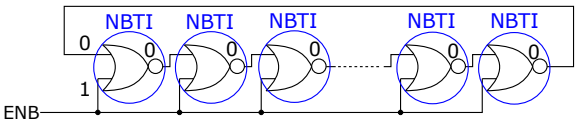


(a) NBTI occurring in PMOS (b) PBTI occurring in NMOS

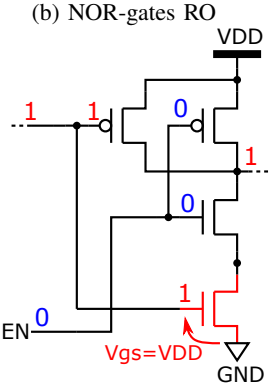
Fig. 1: BTI bias conditions



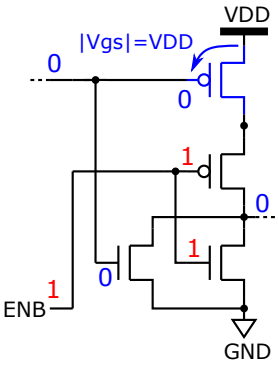
(a) NAND-gates RO



(b) NOR-gates RO



(c) NAND-gate schematic



(d) NOR-gate schematic

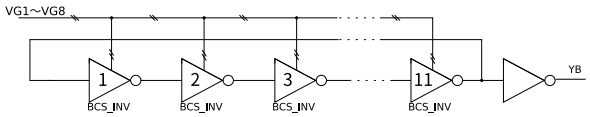
Fig. 2: Circuit structures of RO used in previous study [6]

EN $(= \overline{\text{ENB}})$ is high, and RO is stressed when EN is low. Figs. 2 (c) and (d) show the structures of NAND-gated and NOR-gated ROs, respectively. PBTI only occurs when RO is stressed because all output nodes become 1 and the V_{gs} of the bottom NMOS in the NAND-gates RO is VDD as shown in Fig. 2 (c). NBTI only occurs when RO is stressed because all output nodes become 0 and the V_{gs} of the top PMOS in the NOR-gates RO is $-$VDD as shown in Fig. 2 (d). In previous studies, the degradation rate of NBTI measured by the NOR RO was greater than that of PBTI measured by the NAND RO. However, it is difficult to accurately compare the degradation rates of circuits using PBTI and NBTI. The values of the parasitic components vary depending on the circuit structure. BTI-induced degradation must be measured with the identical circuit structure.

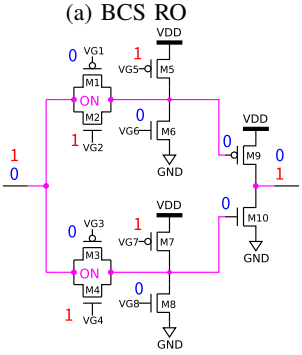
B. ROs with the identical circuit structures with different control signals

In this study, BTI is measured using an 11-stage RO called BTI-Control-Switch RO (BCS RO). Fig. 3 (a) shows the circuit structure of the BCS RO. The identical circuit structure is used to measure different stressed, and unstressed states by changing the control signals (VG1 - VG8).

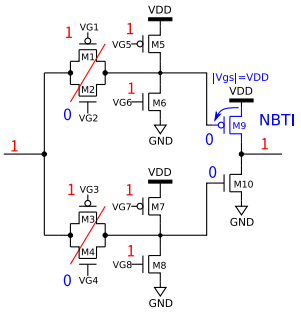
Figs. 3 (b) - (e) show the oscillating state, the NBTI state, the PBTI state, and the unstressed (NOSTR) state, respectively. The inverter composed of M9 and M10 is connected to pull-up and pull-down MOSFETs (M5 - M8) and Transmission Gates (TGs) (M1 - M4). The oscillation state and stressed state are



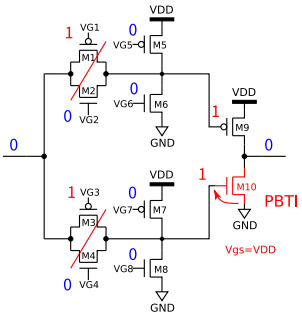
(a) BCS RO



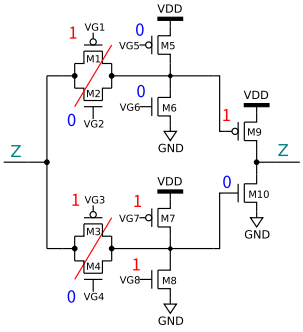
(b) oscillation state



(c) NBTI state



(d) PBTI state



(e) NOSTR state

Fig. 3: Circuit structures of BCS RO

TABLE I: Truth table for gate signals

state	Oscillation	NBTI	PBTI	NOSTR
VG1	0	1	1	1
VG2	1	0	0	0
VG3	0	1	1	1
VG4	1	0	0	0
VG5	1	1	0	0
VG6	0	1	0	0
VG7	1	1	0	1
VG8	0	1	0	1

switched by controlling the gate terminal voltage (VG1 - VG8) of each MOSFET. Table I shows the truth table for the gate signals and the enable pin (EN) at stressed state and oscillation state.

In the oscillation state, the RO is operated as an 11-stage inverter-type RO as shown in Fig. 3 (b). The 11 inverters are connected by turning on the transmission gates between them. The gate terminals of M9 and M10 are not connected to the power supply (VDD) or GND when M5 - M8 are turned off. The gate widths of M1 - M4 are four times wider than those of M9 and M10 in order not to dominate the oscillation frequencies.

There are three types of stressed states: the NBTI, PBTI, and

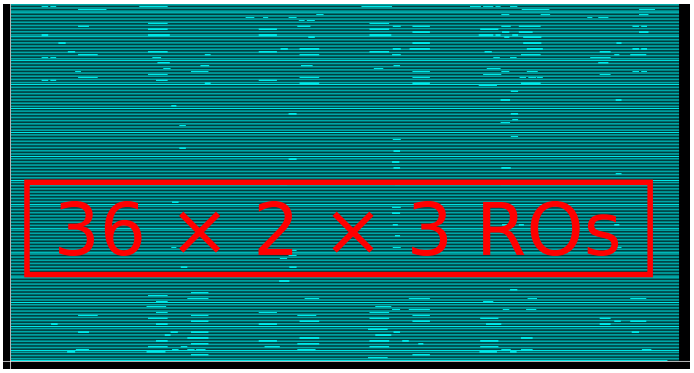


Fig. 4: Macro cell with 216 (36 × 2 × 3 type) 11-stage ROs in a 65 nm process

NOSTR states. The inverter can be disconnected by turning TGs off. M9 is stressed by turning on M6 and M8, resulting in the NBTI state as shown in Fig. 3 (c). M10 is stressed by turning on M5 and M7, resulting in the PBTI state as shown in Fig. 3 (d). M9 and M10 are not stressed by turning on M5 and M8, resulting in the NOSTR state as shown in Fig. 3 (e). The nodes between the 11 inverters are not affected by each stressed state because the TGs are turned off. Since those nodes are floated (Z) at NOSTR state, a pull-up MOSFET is added the input of the last inverter to prevent short-circuit-current. The gate voltage is also controlled by EN in order to be insensitive in oscillation state.

Fig. 4 shows the macro cell including those ROs fabricated in 65 nm process. This measurement uses MOSFETs with low threshold voltage (LVTH) and standard threshold voltage (MVTH). The chip size is 2×2 mm^2. The chip embedds the six types of 216 ROs with the NBTI, PBTI and NOSTR control signals of LVTH and MVTH flavors to measure BTI degradation. The number of oscillations is counted by a 16-bit counter attached to each RO. All ROs oscillate one by one to prevent IR drop and the number of oscillations is stored in the counters. The numbers of oscillations of all counters constructing a shift register are obtained through an output pin after stopping oscillation.

IV. Measurement Results

An engineering tester (Advantest EVA 100) was used for measurement. A Peltier element controlled by a thermostatic device (ATE Service CTS-01A) is stacked on the test chip. BTI degradation increases with stress, but starts to recover after stress voltage is decreased for oscillation. ROs oscillate only for 60 µs and they stop oscillation at least for 10 s to be stressed in order to dominate BTI stress.

The measured degradation was evaluated by threshold voltage degradation. The threshold voltage degradation rate ΔV_{th} is calculated by Eq. (1) with a and b as fitting parameters,

$$\Delta V_{\mathrm{th}} = at^{(1/6)} + b, \tag{1}$$

where t as measurement time [5].

TABLE II: Measured initial oscillation frequencies of identical circuit structures ($t = 0$ s)

RO type	frequency [MHz]	SD [MHz]
LVTH NBTI	487	5.88
LVTH PBTI	495	6.28
LVTH NOSTR	494	5.48
MVTH NBTI	371	5.72
MVTH PBTI	378	6.30
MVTH NOSTR	375	5.29

The BTI degradation rates of the NBTI and PBTI states are compared by measuring the oscillation frequencies of six-type ROs. The measurement results are averaged at 36 ROs. High temperature and high voltage accelerate BTI degradation. The stress voltage was 1.75 V, the oscillation voltage was 1.20 V, the ambient temperature was 120 °C, the oscillation time was 60 μs, and the maximum measurement time was 10,000 s.

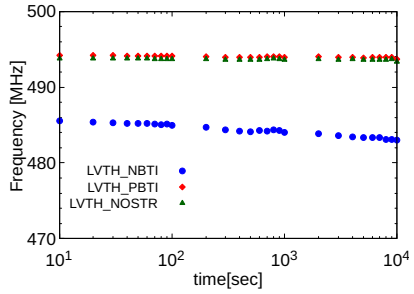
Fig. 5 shows the degradation rate of the RO over time. Figs. 5 (a) and (b) show the degradation rate of the LVTH-type ROs and MVTH-type ROs, respectively. The X- and Y-axis show the BTI stress time and oscillation frequency, respectively. Table II shows the initial oscillation frequency at $t = 0$ s. Table II shows that the averaged oscillation frequency. Standard deviations (SD) are less than 5% in the averaged oscillation frequency, meaning very few variation among the 36 ROs. SDs of PBTI-state ROs are more than 10% in the other SDs. This is because a number of PBTI-state ROs operate at higher than averaged oscillation frequencies. By using BCS RO, the BTI degradation rates of the NBTI, PBTI, and NOSTR states can be compared in the identical circuit structure extracted by circuit simulations considering parasitic components.

Fig. 6 shows the BTI degradation rate of the threshold voltage. The X- and Y-axis show the BTI stress time and degradation rate of the threshold voltage. The results in Fig. 6 is expressed in the power-law model with time exponent $n = 1/6$ in Eq. (1). The degradation rate of the oscillation frequency of RO in the NOSTR state is less than 0.1% at $t = 10,000$ s, and almost no BTI degradation occurs. Table III shows the fitting curves and the root mean square percentage errors (RMSPE) of stressed ROs.

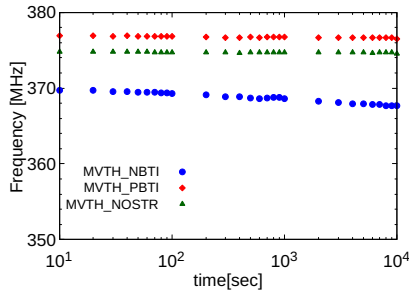
The degradation rate of the NBTI-state ROs is 6x larger than that of the PBTI-state ROs from the fitting parameter a in Table III. The degradation rate of the LVTH-type ROs is 1.5x larger than that of the MVTH-type ROs. RMSPEs are 5% in the NBTI-state ROs, and more than 10% in the PBTI-state ROs. This is because the smaller BTI-induced degradation was much more fluctuated by some environmental changes of ambient temperature or supply voltage.

V. Conclusion

Degradation rates of NBTI and PBTI were compared for the identical circuit structure by measuring BTI degradation. Oscillation frequencies was very few variation among proposed RO structures. The degradation rate of the NBTI-state ROs is 6x larger than of the PBTI-state ROs. The degradation rate



(a) LVTH-type BCS RO



(b) MVTH-type BCS RO

Fig. 5: Oscillation frequency of BCS RO over time

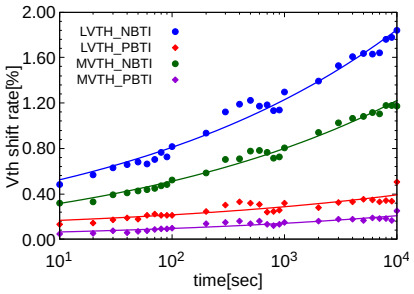


Fig. 6: Threshold voltage degradation rate of BCS RO

TABLE III: Approximation results from measurement of NBTI-state and PBTI-state ROs

RO type	Fitting Curve	RMSPE [%]
LVTH NBTI	$0.41t^{1/6} - 0.086$	5.8
LVTH PBTI	$0.070t^{1/6} + 0.064$	13
MVTH NBTI	$0.28t^{1/6} - 0.10$	5.1
MVTH PBTI	$0.045t^{1/6} - 0.0012$	17

of the LVTH-type ROs is 1.5x larger than of the MVTH-type ROs. The degradation of various of the circuit structure due to the BTI phenomenon is accurately represented by using the degradation rate of the proposed circuit as references.

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