Scalable Highly Integrated Quantum Bit Error Correction System by Classical Electronics

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ABSTRACT

In this presentation, I will introduce our project named "Development Scalable Highly Integrated Quantum Bit Error Correction System (Qubecs)." It belongs to one of the governmental-funded project called Moonshot Goal 6 "Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050."

We are going to develop an FTQC (fault-tolerant quantum computer) by using superconducting qubits developed by RIKEN. Fig. 1 compares the current and proposed structure of quantum computers. Current quantum computers have no error correction capability. The qubit controller placed at room temperature controls superconducting qubits placed inside a dilution refrigerator at cryogenic (extremely-low) temperature. The controller consists of discrete components with large volume ($\simeq$ 9U) and huge power.

The proposed structure of an FTQC is depicted in the right side of Fig. 1. The backend system at the top level correct errors by using FPGA clusters with some assistance of ASICs. We are going to reduce volume and power of the qubit controller (frontend) at the second level with customised ASICs, SiPs and SoMs. In order to reduce wires and temperature leak, optical fibers are used between the optical and cryogenic CMOS ICs and the frontend. To develop an FTQC scalable up to 1 million physical qubits, the five research topics (subjects) are in progress as shown in Fig. 2. The details of each subject based on classical electronics will be explained in the presentation.

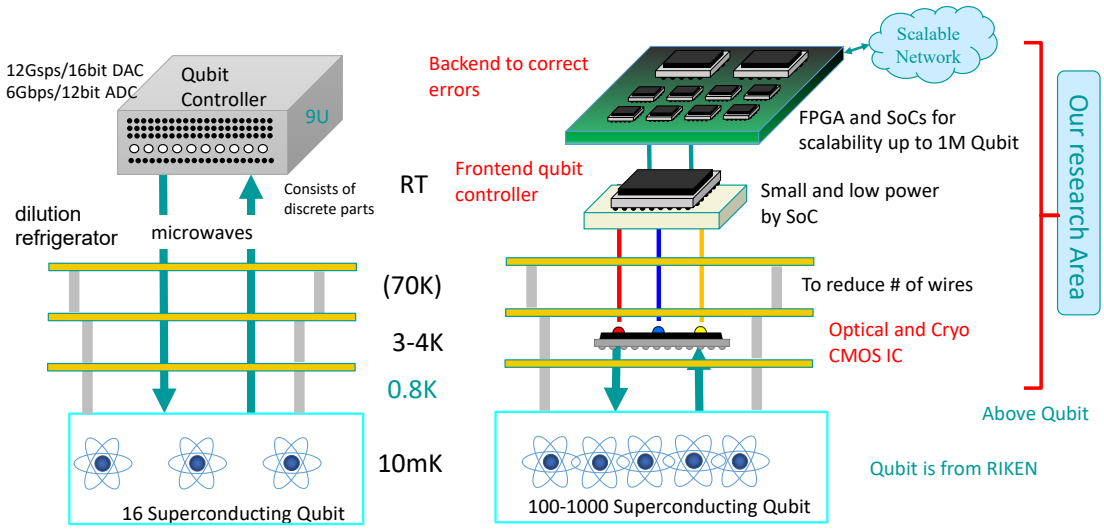

Fig. 1: Current NISQ (Noisy Intermediate-Scale Quantum Device, left) and future FTQC (Fault Tolerant Quantum Computer, right)

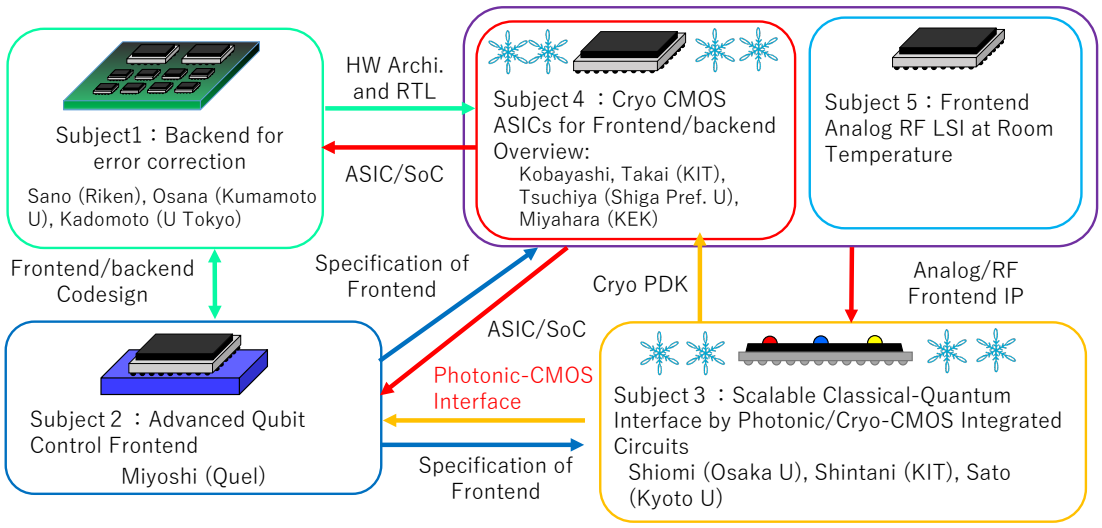

Fig. 2: Five subjects (research topics) to develop an FTQC with 1 million qubits.