Soft-Error Tolerance Depending on Supply Voltage by Heavy Ions on Radiation-Hardened Flip Flops in a 65 nm Bulk Process

Yuto Tsukita*, Mitsunori Ebara, Jun Furuta, and Kazutoshi Kobayashi

Kyoto Institute of Technology, Japan
*Email:ytsukita@vlsi.es.kit.ac.jp

Abstract – We evaluated soft-error tolerance by heavy ions on several types of flip flops (FFs) called transmission-gate FF (TGFF), Dual Interlocked Storage Cell FF (DICEFF), Bistable Cross-coupled Dual Modular Redundancy FF (BCDMRFF) and BCDMRFF with Set and Reset (BCDMRFFSR) in a 65 nm bulk process. Radiation-hardened FFs are stronger against soft errors than a standard TGFF by two or three order of magnitude. DICEFF has higher soft-error tolerance than BCDMRFF by low-LET heavy ions less than 40 MeV-cm^2/mg, while BCDMRFF is stronger against soft error than DICEFF by high-LET ions over 40 MeV-cm^2/mg. DICEFF becomes weaker by lowering supply voltage, while BCDMRFF has higher soft-error tolerance than DICEFF when supply voltages is less than 1.0 V.

1. Introduction

Reliability issues have become a significant concern due to soft errors with technology downscaling [1]. Soft errors are one of temporal failures that flip stored values in storage elements such as flip flops (FFs) or SRAMs by heavy ions from cosmic rays. When heavy ions hit transistors, the perturbation in the output node voltage is generated, which is called a single event transient (SET) pulse. A SET pulse will cause a single event upset (SEU). A flipped storage cell can be recovered by rebooting or rewriting. However, it is a serious issue especially for critical devices dealing with human life or social infrastructures.

In the circuit level, several redundant FFs such as the triple modular redundancy FF (TMRFF) [2], dual interlocked storage cell FF (DICEFF) [3][4] and Bistable Cross-coupled Dual Modular Redundancy FF (BCDMRFF) [5] have been proposed for effective countermeasures. The effect of supply voltage on the radiation tolerance of these FFs must be investigated for low-power application since Dynamic Voltage-Frequency Scaling (DVFS) is generally used to minimize power consumption of the circuit [6].

In this paper, we compared several types of FFs by heavy-ion irradiation. We also investigated soft-error tolerance of those FFs depending on supply voltage by heavy ions. We explain several types of radiation-hardened FFs in a 65 nm bulk process in Section 2. Section 3 explains experimental setup. Section 4 explains experimental results by heavy-ion irradiation and discussion. We conclude this paper in Section 5.

2. Flip Flops to evaluate soft-error tolerance

Transmission-Gate FF

Figure 1 shows a standard FF called TGFF. We used two types of TGFF. One is a standard TGFF in a process design kit. It has no tolerance against soft errors. The other is TGFF with guard ring in Pwell (TGFFWG). Figure 2 shows an inverter layout with a guard ring. It can reduce parasitic resistance of Pwell [7].The following radiation-hardened FFs also have guard rings.

Dual Interlocked Strage Cell FF

Figure 3 shows a schematic of DICEFF. The DICE structure mitigates soft errors by duplicating latches. The input and output signals of these half C-elements have cross-coupled connections to be automatically recovered from a flip on a single node. The DICE structure is area-efficient since latches are not triplicated but duplicated.

Bistable Cross-coupled Dual Modular Redundancy FF

Figure 4 shows the schematic of BCDMRFF. BCDMRFF is radiation-hardened by keeping correct values in dual-modular latches and weak keepers. The C-element intercepts transmission of a flipped value of the dual modular latches. Even if a SET pulse flips a stored value in a keeper, the other C-element restores the stored value. Duplicated C-elements result in keepers with perfectly symmetrical structures and improve radiation hardness.

BCDMRFF with Set and Reset

Figure 5 shows the schematic of BCDMRFFSR. BCDMRFFSR embeds set and reset capability required to construct ASICs with the power-on-reset functionality. The master latch consists of a conventional set and reset structure using a NAND gate and a tristate NAND gate. On the other hand, the slave latch is a simple set and reset structure using only PMOS to compare tolerance due to the difference of latch structures.

Table 1 shows the results of delay time, power consumption and area of TGFF, DICEFF, BCDMRFF and BCDMRFFSR using circuit simulations at V_{dd} = 1.2 V. All values are normalized to those of TGFF. The values in parentheses are normalized to those of TGFFWG.

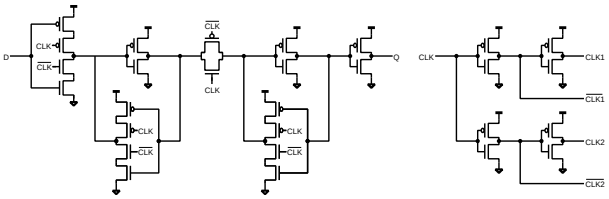

Figure 1. Transmission-Gate FF

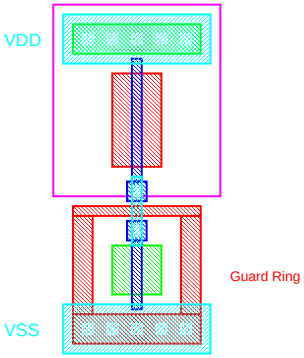

Figure 2. Inverter layout with guard ring

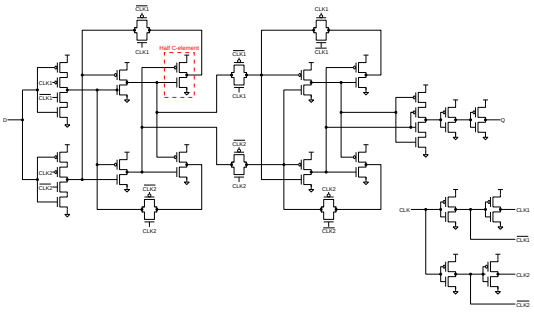

Figure 3. Dual Interlocked Strage Cell FF

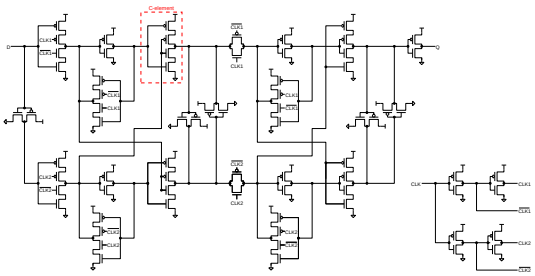

Figure 4. Bistable Cross-coupled Dual Modular Redundancy FF

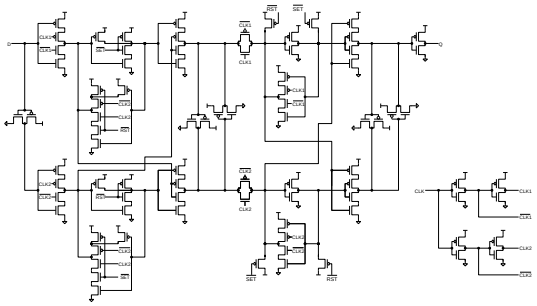

Figure 5. Bistable Cross-coupled Dual Modular Redundancy FF with Set Reset

Table 1. Simulation results of area, DQ delay and power of each FF at V_{DD} = 1.2 V.

FF	D-Q delay	Area	Power	# of Tr.
TGFF	1.00	1.00	1.00	24
TGFFWG	1.46 (1.00)	1.32 (1.00)	0.87 (1.00)	24 (1.00)
DICEFF	2.89 (1.26)	2.95 (2.24)	2.50 (2.88)	52 (2.17)
BCDMRRFF	3.03 (2.08)	3.79 (2.88)	2.12 (2.44)	72 (3.00)
BCDMRFFSR	3.67 (2.52)	4.00 (3.04)	2.38 (2.74)	84 (3.50)

3. Experimental Setup

A test chip was fabricated in a 65 nm bulk process in order to evaluate soft-error tolerance. Four chips are mounted in a package to increase the number of FFs exposed to heavy ions.

Figure 6 shows the package of test chip that contains 20,160-bit TGFFs, 7,560-bit TGFFWGs, 8,400-bit DICEFFs, 48,000-bit BCDMRFFs, and 48,720-bit BCDMRFFSRs. All FFs are connected in series to form a shift register. We evaluated soft-error tolerance by heavy-ion irradiation.

Heavy-ion irradiation tests were conducted by Ne, Ar and Kr at Takasaki Ion accelerators for Advanced Radiation Application (TIARA) in order to investigate tolerance to soft errors in outer space and the terrestrial region. Figure 7 shows the experimental setup of the heavy-ion irradiation tests. Device under tests (DUTs) are sealed in the chamber in order to keep ion energy. Table 2 shows linear energy transfer (LET), energy and average flux of heavy ions. In outer space, most of heavy ions have LET less than 60 MeV-cm^2/mg. Thus, we chose Ne for terrestrial regions and Ar and Kr for outer space.

Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1) and V_{dd} was 1.2 V. Each irradiation time was 30 sec. and irradiation was repeated for 5 times per conditions.

The irradiation procedure was as follows.

1) Initialize serially-connected FFs by all 0 or all 1
2) Stabilize CLK to 0 or 1
3) Expose heavy ions

4) Read out stored data of FFs
5) Count the number of upsets
6) Repeat 1) - 5) for four (DATA, CLK) conditions

The test chip was irradiated from the normal angle (θ = 0°) under the four DATA and CLK states.

In addition, we examined soft-error tolerance depending on supply voltage when (DATA, CLK) = (0, 1). We chose this condition because the number of errors at the condition is the largest of all. Experiments were carried out at V_{dd} = 0.6 V, 0.8 V and 1.0 V by Kr irradiation.

Cross Section (CS) is used in order to evaluate soft-error tolerance, which means an area of upsets when a particle passes a circuit block. The soft-error tolerance becomes stronger if CS becomes smaller. Equation 1 is used in order to calculate CS [8] .

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}}\ N_{\mathrm{FF}}} \tag{1}$$

N_{ion} is the effective heavy-ion fluence.

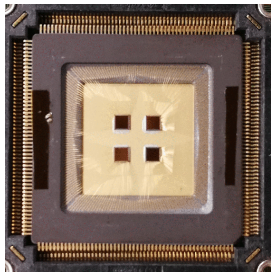

Figure 6. Package mounting four chips

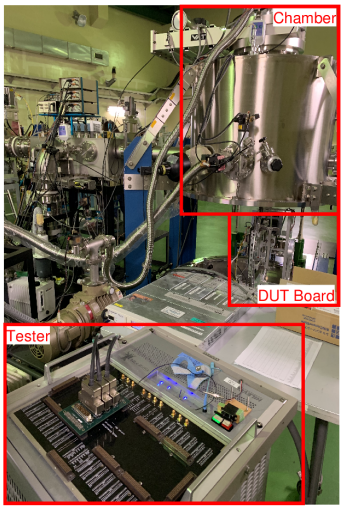

Figure 7. Heavy-ion irradiation setup

Table 2. LET, Energy and fluence of heavy ions

Ion	LET [MeV-cm^2/mg]	Energy [MeV]	Flux [n/cm^2/s]
Ne	6.38	73.9	1.01×10^5
Ar	15.4	147	5.11×10^4
Kr	40.1	315	2.83×10^4

4. Experimental Results and Discussion

Figures 8, 9 and 10 show the experimental results of the CSs by Ne, Ar and Kr with error bars of 95% (2σ) confidence. Radiation-hardened FFs are stronger against soft errors than TGFF by two or three order of magnitude. CS of TGFF and TGFFWG is almost equivalent besides (DATA, CLK) = (0, 1). Guard ring almost does nothing for SEU. At the normal incident of Ne and Ar, there was no error on DICEFF. Soft errors occurred on DICEFF when (DATA, CLK) = (0, 0) at Kr irradiation. DICEFF is weak against soft error under this condition because the distance between critical nodes is shortest. BCDMRFF is more resistant to soft errors than BCDMRFFSR because the transistors added for set and reset reduce drive current.

The average CSs of DICEFF are 1/295, 1/498 and 1/31 smaller than those of TGFFWG by Ne, Ar and Kr respectively. The average CSs of BCDMRFFSR are 1/24, 1/42 and 1/49 smaller than those of TGFFWG by Ne, Ar and Kr respectively. The average CSs of BCDMRFF are 1/46, 1/93 and 1/120 smaller than those of TGFFWG by Ne, Ar and Kr respectively. DICEFF has high soft-error tolerance by low-LET heavy ions less than 40 MeV-cm^2/mg, while BCDMRFF has higher soft-error tolerance than DICEFF when the larger-LET ions over 40 MeV-cm^2/mg is irradiated.

Figure 11 shows the experimental CSs depending on the supply voltage by Kr with error bars of 95% (2σ) confidence. All FFs except for TGFF become weaker against soft errors as the supply voltage is lowered. CS of TGFF decrease due to reduction parasitic bipolar effect. We revealed that DICEFF becomes weak to soft error when supply voltage is under 0.8 V. DICEFF is less resistant to soft errors than TGFF when

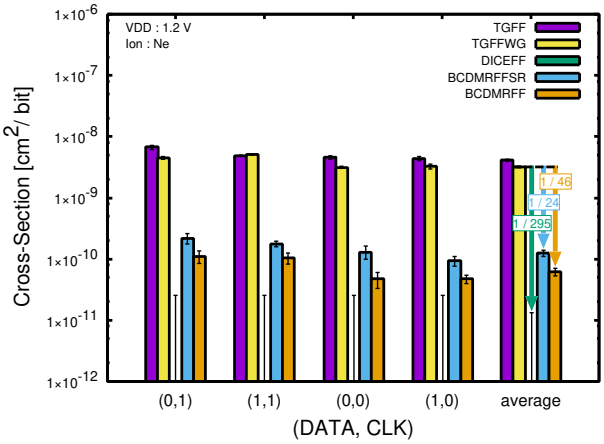

Figure 8. Experimental results of the CSs by Ne irradiation

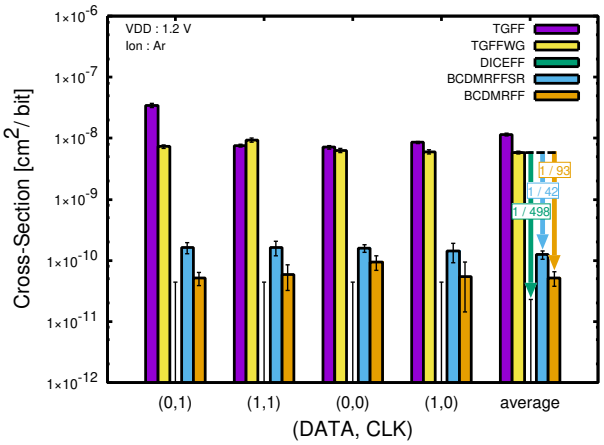

Figure 9. Experimental results of the CSs by Ar irradiation

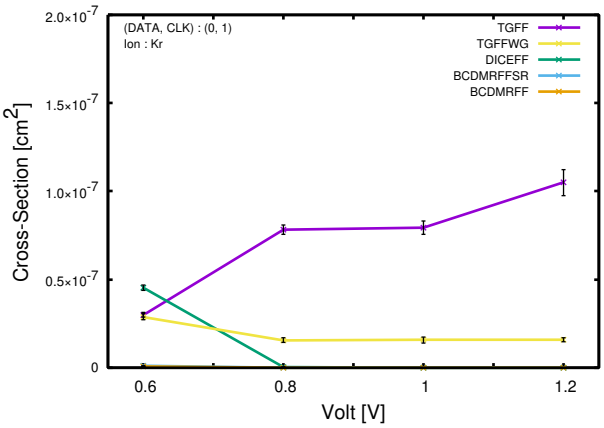

Figure 11. Experimental results of the CSs by volt

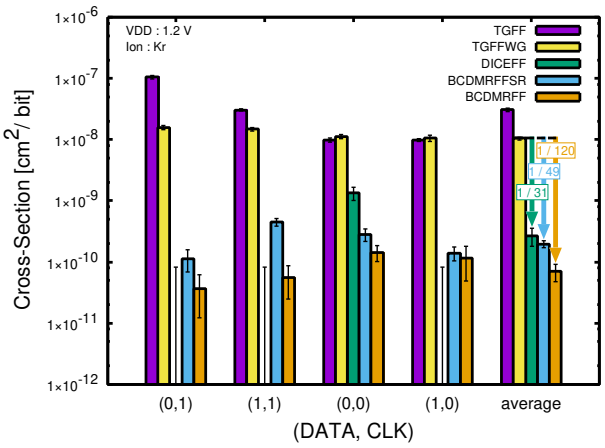

Figure 10. Experimental results of the CSs by Kr irradiation

the supply voltage is 0.6 V. As supply voltage decreases, the overdrive voltage at the gate terminals of PMOSFET and NMOSFET deceases. If one of P or NMOSFET reaches 0 overdrive voltage, it cannot restore a flipped node. This is becsuse DICEFF is a ratio circuit. On the other hand, BCDMRFF is a ratioless circuit. Thus, BCDMRFF is resilient to soft errors at lower supply voltage. DICEFF with set and reset is more sensitive to supply voltage since transistors are stacked. DICEFF has high soft-error tolerance at supply voltages over 1.0 V. BCDMRFF has higher soft-error tolerance than DICEFF when supply voltages is less than 1.0 V.

5. Conclusion

We measured radiation hardness of TGFF, TGFFWG, DICEFF, BCDMRFF and BCDMRFFSR in the 65nm bulk process by Ne, Ar and Kr ions.

Radiation-hardened FFs are stronger against soft errors than TGFF by two or three order of magnitude. DICEFF has high soft-error tolerance by low-LET heavy ions less than 40 MeV-cm^2/mg. BCDMRFF has higher soft-error tolerance than DICEFF when the larger-LET ions over 40 MeV-cm^2/mg is irradiated.

We also investigated supply voltage dependence of those FFs by heavy ions. All FFs except for TGFF become weaker against soft errors as the supply voltage is lowered. DICEFF can not recover from upset when supply voltage becomes lower due to its ratio structure. DICEFF becomes weaker against soft errors when set and reset is added. On the other hand, BCDMRFF and BCDMRFFSR have high soft-error tolerance at any supply voltage due to its ratioless structure. DICEFF has high soft-error tolerance at supply voltages over 1.0 V. BCDMRFF has higher soft-error tolerance than DICEFF when supply voltages is less than 1.0 V.

References

[1] R. Baumann. The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction. In *Digest. International Electron Devices Meeting,*, pages 329–332, Dec. 2002.

[2] D. G. Mavis and P. H. Eaton. Soft error rate mitigation techniques for modern microcircuits. In *2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320)*, pages 216–225, April 2002.

[3] T. Calin, M. Nicolaidis, and R. Velazco. Upset hardened memory design for submicron cmos technology. *IEEE Transactions on Nuclear Science*, 43(6):2874–2878, Dec 1996.

[4] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera. A low-power and area-efficient radiation-hard redundant flip-flop, dice acff, in a 65 nm thin-box fd-soi. *IEEE Transactions on Nuclear Science*, 61(4):1881–1888, Aug 2014.

[5] R. Yamamoto, C. Hamanaka, J. Furuta, K. Kobayashi, and H. Onodera. An area-efficient 65 nm radiation-hard dual-modular flip-flop to avoid multiple cell upsets. *IEEE Transactions on Nuclear Science*, 58(6):3053–3059, Dec 2011.

[6] T. Ishihara and H. Yasuura. Voltage scheduling problem for dynamically variable voltage processors. In *Proceedings. 1998 International Symposium on Low Power Electronics and Design (IEEE Cat. No.98TH8379)*, pages 197–202, Aug 1998.

[7] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf. Charge collection and charge sharing in a 130 nm cmos technology. *IEEE Transactions on Nuclear Science*, 53(6):3253–3258, Dec 2006.

[8] J. S. Kauppila, T. D. Loveless, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. W. McCurdy, R. A. Reed, B. L. Bhuva, L. W. Massengill, and K. Lilja. Utilizing device stacking for area efficient hardened SOI flip-flop designs. In *IEEE International Reliability Physics Symposium*, pages SE.4.1–SE.4.7, June 2014.