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Correlations between Well Potential and SEUs Measured by Well-Potential Perturbation Detectors in 65nm

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Abstract— **We measures and investigate the correlation between well potential and SEUs to effectively detect SEUs by well potential perturbation. Cell-based perturbation detectors are implemented adjacent to FFs constructed a shift register. They measures the locations of voltage levels over 0.6 or 0.8 V. The measurement results by neutron irradiation on a 65nm bulk CMOS shows that almost 90% of SEUs are generated without any well potential perturbation. We also shows that the well-potential elevation over 0.8 V activates bipolar actions on neighbourhood transistors which prevents SEUs.**

I. Introduction

According to process scaling and increase in the clock frequency, SEU (Single Event Upset) and also SET become more significant issues for LSI reliability[1]. They are collectively called soft error caused by a particle hit on LSIs. A particle hit generates electron-hole pairs and minority carriers are collected by drain through drift and diffusion. SEU flips a stored value on SRAMs or flip-flops (FFs), while SET generates a temporal pulse on logic gates. In addition, MCU (Multiple Cell Upset) which flips several stored values on SRAMs also increases and becomes a critical issue.

To improve soft-error mitigation, several redundant FFs are proposed such as TMR, DICE[2], and BISER FFs[3]. They can reduce soft error rate on LSIs, but they have large area and delay overhead. For another solution to improve soft-error resilience, the bulk Built-In Current Sensor (bulk-BICS) has been proposed[4]. It is connected to the bulk, and monitors on-chip current caused by a particle hit to detect soft-error occurrence. Compared with redundant FFs, its area-overhead is relatively small. However, there is no measurement result of bulk-potential perturbation caused by a particle hit.

The contributions of this paper are as follows.

1) A simple well-potential perturbation detector is developed to monitor well potential by the threshold voltage of skewed inverters.
2) First measurement results of well potential perturbation caused by a particle hit from spallation neutron irradiation.
3) Almost 90% of SEUs are generated without any well potential perturbation.
4) Parasitic bipolar actions by well potential elevation on adjacent transistors prevent SEUs.

The paper is organized as follows. Section II explains the test circuit structure in detail. Section III shows our neutron-beam experimental setup in RCNP, followed by Section IV which discusses experimental and simulation results. Section V concludes this paper.

II. Test Circuit Structure

Fig. 1 shows the well-potential perturbation sensors. They consist of NAND / NOR chains, a pulse amplifier and a time-to-digital converter (TDC) based on [5]. An input port of the NAND/NOR gate is connected to the p-well or n-well through an inverter. If a particle hit on a chip and well-potential is elevated over the threshold voltage, the inverter is flipped until well-potential goes back to less than the threshold. Therefore, well-potential perturbation is converted to a rectangular pulse by the NAND / NOR chain. The pulse is prolonged by the pulse amplifier. Finally, the TDC detects well-potential perturbation and measure its duration. Two types of detectors are implemented by skewing the inverter. Their threshold voltages are 0.6 V and 0.8 V, respectively. The voltage levels of 0.6 V and 0.8 V are half of the supply voltage (1.2 V) and the voltage level that parasitic bipolars can flip the inverter. Thus, outputs of transistors may be flipped by the parasitic bipolar effect when the proposed circuit detects 0.8 V perturbation of well-potential. In the circuit level simulation, 0.8V threshold voltage changes $\pm$ 0.06 V at FF or SS corner model compared with FF corner model. In order to remove parasitic bipolar effect on the chains caused by well-potential perturbation, they are placed on wells different from the measured ones.

Fig. 2 shows a block diagram of the fabricated test circuit. Tap-cell arrays are inserted into every 55 μm and 11 columns of the proposed circuits and FF arrays are implemented between the tap cells. Therefore, they are implemented in every 5 μm. To place NAND/NOR chains of the proposed circuits, there are about 5 μm interval every three FF columns. We assume that when the proposed circuit detects 0.8 V perturbation of well-potential, FFs which are adjacent to it may be flipped by the parasitic bipolar effect. Note that, in this test structure, the proposed circuits only measure potential of p-well and n-well shared by two FF columns as shown in Fig. 2. Therefore, 1/3 of all p-well and n-well are not monitored and 1/3 of SEUs on FFs are expected to be happened in the unmonitored p/n-wells.

III. Experimental Setup

Fig. 3 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It includes twin-well and triple-

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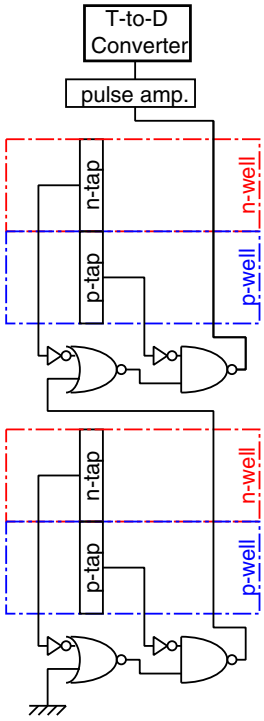

Fig. 1. Well-Potential perturbation detector composed of NAND/NOR chains, pulse amplifier and T-to-D converter.

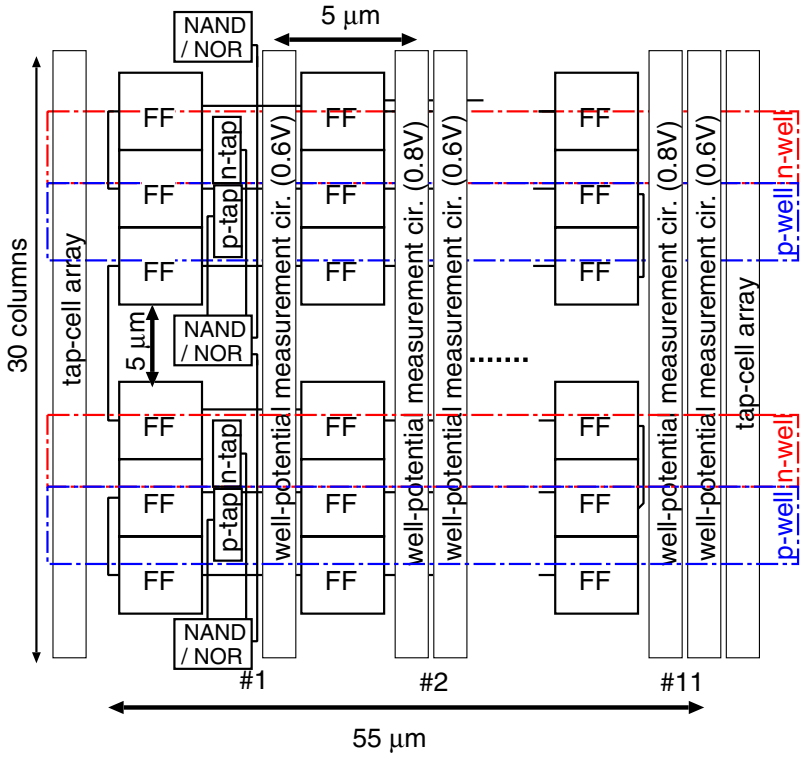

Fig. 2. Block diagram of measurement circuit with detector and shift register.

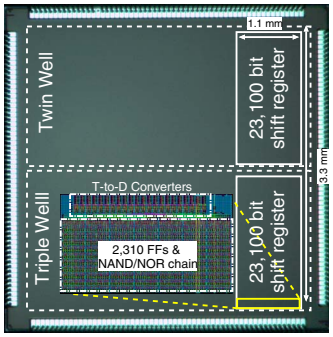

Fig. 3. Chip micrograph and floorplan.

well areas and its supply voltage is 1.2 V. It is implemented by tapless standard cells[6]. In order to measure neutron-induced well-potential perturbation and SEU rate on FFs, a 23,100 bit shift register is implemented on each well area and its total area is a 1.1×3.3 mm^2 on a 4×4 mm^2 die.

Accelerated tests were carried out at RCNP (Research Center for Nuclear Physics, Osaka University). The average accelerated factor is 3.8×10^8. In order to increase error counts, we measured 12 chips at the same time using stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data. During irradiation, all stored values of the shift register are initialized to "0" and the clock signal is fixed to "0" in which slave latches are in the latch state. Stored values are retrieved every 5 minutes.

IV. Experimental Results and Discussions

Fig. 4 and 5 show the number of well-potential perturbations on the twin-well and triple-well respectively. X-axis shows the number of well-potential measurement circuits which detect well-potential perturbation simultaneously. In this measurement, rate of well-potential perturbation is about 8x bigger than SEU rate on FFs. We assume that well-potential perturbation may happen when a particle hits on whatever except slave latch which has hold state. Compared with triple-well, well-potential on twin-well is more easily perturbed with wider range. It is because that triple-well structure has bigger capacitance of NP-diode between deep n-well and p-well. Fig. 6 shows one example of measurement results on the twin-well. Well-potential is perturbed for over 1000 ps at 0.8 V. This results shows that if such long perturbation affects an inverter, SET pulse over 1000 ps injected into output of the inverter. Table I shows the relation between well-potential perturbation and SEU occurrence on FFs. As described in Sec. II, 1/3 of SEUs may happen in the unmonitored p/n wells. Excluding these SEUs, the correlation between well-potential perturbation and SEUs are still very weak. It is impossible to detect SEUs by measuring well-potential perturbation. On the other hand, even if the proposed circuits detect perturbations over 0.8 V, 95% of FFs adjacent to the proposed circuits are not flipped. Therefore, stored values of FFs can not be flipped by the parasitic bipolar effect when slave latches of the FFs hold "0". Next paragraph, we explain why SEU does not occur on FFs although the test circuit detects well-potential perturbation from circuit-level simulation results.

To analyze measurement results, we calculate SEU rate on FFs from circuit-level simulations. We use a single-exponential current source as shown Eq. (1) to obtain the critical charge Q_{crit} which is defined as the minimum charge

TABLE I

RELATION BETWEEN WELL-POTENTIAL PERTURBATION AND SEU OCCURRENCE ON FFS.

well	# of SEU w/o perturb.	# of SEU w/ perturb.	# of perturb. 0.6 V	# of perturb. 0.8 V
twin	118	18	953	368
triple	132	9	481	243

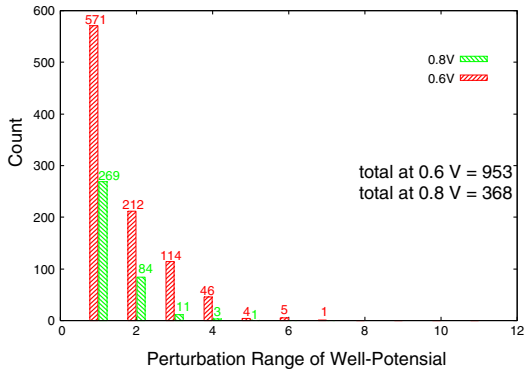

Fig. 4. Measurement result1 : perturbation Range of well-potential on the twin-well.

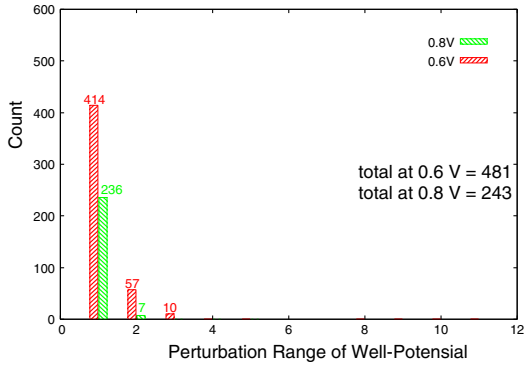

Fig. 5. Measurement result2 : perturbation Range of well-potential on the triple-well.

to flip stored value of FF[7].

$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(\frac{-t}{T}\right) \quad (1)$$

where T is a time constant depending on a fabricated process. Then, the SEU rate is computed from the empirical model in Ref. [8] as follows.

$$N_{\mathrm{SET}} = F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \quad (2)$$

F : Neutron Flux, A : Drain Area

Q_{s} : Charge Collection Efficiency

From [8], the parameter T and Q_{s} are 30 ps and 10 fC, respectively.

In this simulation, we use a circuit structure as shown in Fig. 7 to consider well-potential perturbation by a particle hit. IS and TS are an inverter and a tristate inverter which construct a slave latch in a FF as shown in Fig. 8. It has two single-exponential current sources, parasitic bipolar, and R/C ladder as well resistance and capacitance. One current source injects current induced by drift, diffusion and funneling into the output of the inverter IS, while the other injects current

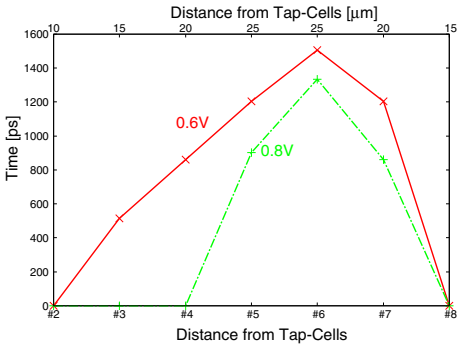

Fig. 6. Example of measurement results for well-potential perturbation on the twin-well.

by hole injection into the bulk of NMOS transistors in IS and TS. The well resistance and the parameter β of parasitic bipolar are 730 Ω/μm and 10 respectively obtained from measurement results while well capacitance is 1 fC/μm obtained from the drain capacitance by circuit level simulations.

Fig. 9 and 10 show simulation results of SEU on a FF and well-potential perturbation at Q = 10 fC and 20 fC, respectively. At Q = 10 fC, the outputs IS and TS are flipped by a particle hit and SEU occurs on the FF while well-potential under the slave latch rises to just 0.6 V. This simulation result shows that the fabricated test circuit cannot detect well-potential perturbation when a particle hit generates less than 10 fC charge injection. On the other hand, at Q = 20 fC, the output of TS is not flipped by a particle hit, though the output of IS transiently falls to lower voltage than that at Q = 10 fC. It is because that parasitic bipolar of TS turns on by well-potential perturbation and prevents the output of TS from rising to VDD (1.2 V). After falling well-potential and turning off parasitic bipolar, the output of IS and TS start rising towards 1.2V as their input ports are almost 0 V. Then, output of IS rise to 1.2 V and that of TS remains 0 V since IS has 4x bigger drive strength and shorter rise delay than TS as shown in Fig. 8. As a result, SEU does not occur at Q = 20 fC. It is one of the reasons why SEU does not occur on FFs although the test circuit detects well-potential perturbation. In this simulation, Q values are 9.5 $\sim$ 13.7 fC when an SEU occurs on a FF and SEU rates decrease about 1/3 compared with simulation result of SEU without considering parasitic bipolar actions. This simulation result also shows that MCU on FFs does not occur by parasitic bipolar effect when output of tristate inverter in FF is "0". It is consistent with our previous measurement result of MCU rates on FFs as shown in Table II[9]. In our previous measurement result, MCU does not occur at this measurement state, IS = 0 and CLK = 0.

V. Conclusion

We show measurement results of well potential perturbation caused by a particle hit from spallation neutron irradiation. The implemented well-potential detector can measure arbitrary voltage level of well-potential by using skewed inverters. Experimental results show that rate of well-potential perturbation is 3x$\sim$7x bigger than SEU rate on FFs and over 1000 ps duration of perturbation is also measured. Its longer

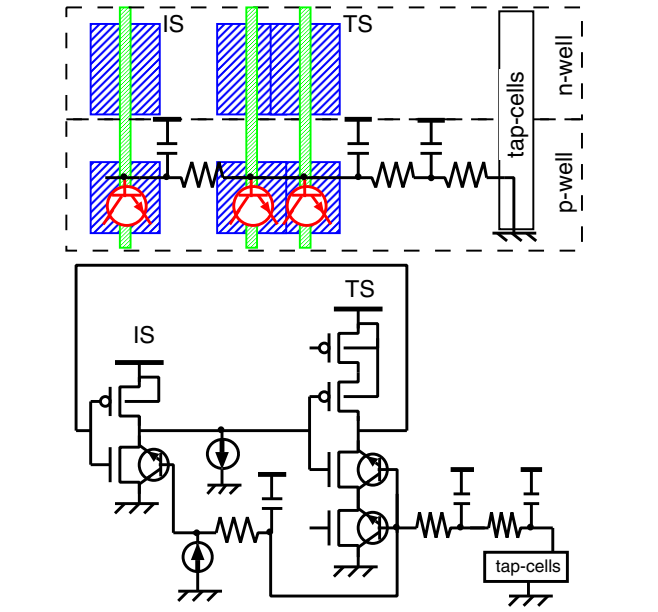

Fig. 7. Simulation circuit considering parasitic bipolar and distance from tap-cell array.

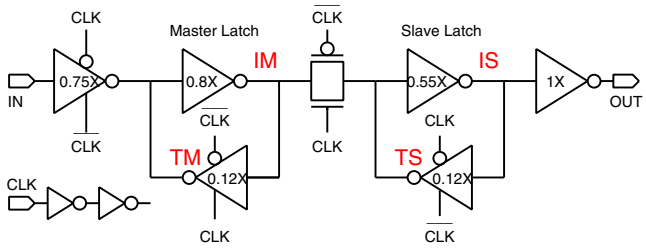

Fig. 8. Schematic diagram of a FF.

perturbation may cause long SET pulses. The measurement results by neutron irradiation on a 65nm bulk CMOS shows that almost 90% of SEUs are generated without any well potential perturbation. On the other hand, there is very weak correlation between well-potential perturbation and SEUs on FFs. In the circuit level simulations, well-potential does not rise to over 0.6 V while SEU occurs on a FF by the generated charge around 10 fC. That phenomena is one of the reasons why SEUs happens without perturbation. Parasitic bipolar actions are becoming dominant by the charge over 13.7 fC. FFs are prevented from flipping through the well-potential rise over 0.8 V activating the parasitic bipolar transistors. That is the one of the possibilities why the correlation is very weak.

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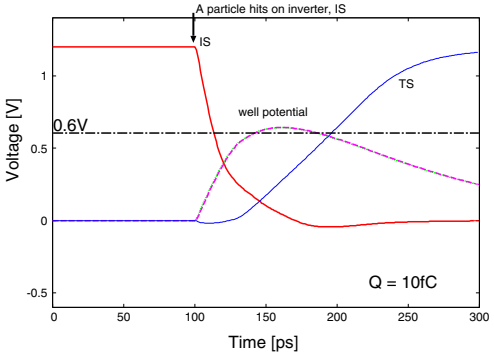

Fig. 9. Simulation result of SEU and well-potential perturbation at Q= 10 fC.

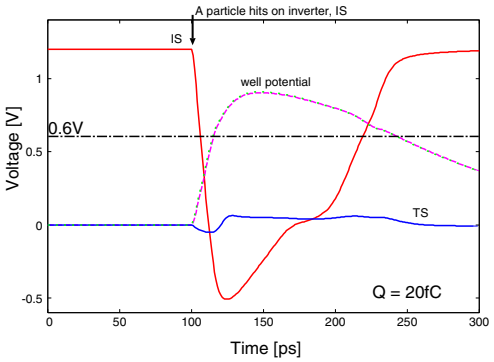

Fig. 10. Simulation result of SEU and well-potential perturbation at Q= 20 fC.

TABLE II

SEUs AND MCUs RATES ON FFs ACCORDING TO STORED VALUES IN MASTER OR SLAVE LATCHES BY NEUTRON BEAM IRRADIATION[9].

Vulnerable Latch	State	# of SEU (n/Mb/h)	# of MCU (n/Mb/h)
Master (CLK=1)	IM=0	541	88
	IM=1	222	0
Slave (CLK=0)	IS=0	493	19
	IS=1	112	0

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