Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era

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Abstract

Ultralow-voltage (ULV) operation of CMOS circuits is effective for significantly reducing the power consumption of the circuits. Although operation at the minimum energy point (MEP) is effective, its slow operating speed has been an obstacle. The silicon-on-thin-buried-oxide (SOTB) CMOS is a strong candidate for ultralow-power (ULP) electronics because of its small variability and back-bias control. These advantages of SOTB CMOS enable power and performance optimization with adaptive V_{th} control at ULV and can achieve ULP operation with acceptably high speed and low leakage. In this paper, we describe our recent results on the ULV operation of the CPU, SRAM, ring oscillator, and, other logic circuits. Our 32-bit RISC CPU chip, named "Perpetuum Mobile," has a record low energy consumption of 13.4 pJ when operating at 0.35 V and 14 MHz. Perpetuum-Mobile micro-controllers are expected to be a core building block in a huge number of electronic devices in the internet-of-things (IoT) era.

Introduction

Highly energy efficient CMOS circuits are required in the internet-of-things (IoT) era since a great number of small electronic apparatuses process and communicate data. It is well known that the operating voltage (V_{dd}) is an important parameter for reducing the energy consumption of CMOS. The energy is a sum of active (E_{ac}) and leakage (E_{leak}) energy, and the minimum energy (E_{min}) point (MEP) exists roughly at ~0.4 V. Scaling has improved E_{ac}; however, most of the circuits operate with far higher energy than E_{min}. In recent generations, scaling has increased the V_{dd} at MEP, as shown in Fig. 1 below [1, 2]. In an energy-efficiency conscious design like [1], the E_{min} already hit the bottom (minimum point of E_{min} at 90 nm). The MEP operation is generally very slow, e.g. less than 1 MHz. The variable V_{th} approach with adaptive back-bias control can mitigate the situation of decreasing energy as low as possible down to MEP while satisfying the required frequency. Another obstacle is the variability of transistors, especially at low V_{dd}. The variability tolerant design, that is, increasing W, smaller pipeline-stage number, etc., tends to increase the power or decrease the speed. To solve these problems, we are developing silicon on thin buried oxide (SOTB) [3, 4]. In this paper, we demonstrate SOTB's small variability, back-bias control, and ULV circuit operation.

SOTB Device Results

A cross-section of the SOTB/bulk hybrid CMOS and a TEM photo are shown in Figs. 2 and 3. The back-bias voltages, V_{bn} and V_{bp}, are applied to the well regions below BOX. The local interconnect by the silicide at the well contact region contributes to improving the back-bias voltage stability. Details of the SOTB process and electrical characteristics are described in [3, 4].

Very small V_{th} and I_{on} variability was demonstrated [4] for one million transistors (Figs. 4 and 5). The Pelgrom coefficient was ~1.3 mVμm, the smallest level taking the gate-oxide thickness (T_{inv} = 2.4 nm) into account. With this improvement, we confirmed 6-T SRAM operation (2 Mbit) at less than 0.4 V (Fig. 6) with a 5.5-ps access time and demonstrated that the minimum operating voltage can be controlled at <0.4 V by back-bias against temperature variation [4].

SOTB Circuit Design and ULV Operation

We developed a standard cell library for the SOTB technology. The delay library was calibrated through a ring oscillator (RO) measurement [5]. The delay of SOTB was 42% smaller than that of the bulk at V_{dd} = 0.4 V, where the V_{th}s of the SOTB and bulk were the same (Fig. 7). The delay variability σ_{tpd} of the SOTB exhibited a very weak $1/\sqrt{N}$ dependence (Fig. 8). Assuming a global component, the estimated local factor was very small. We also demonstrated a significant reduction in die-to-die delay variation with a proper back-biasing in consideration of the drivability balance of N and PMOS transistors [6].

The SOTB design flow is basically the same as that for the bulk technology. Using our SOTB flow, various logic circuits were designed and ULP operations were confirmed, such as an accelerator [7] and flex-power FPGA with back biasing [8]. We designed a micro-controller chip named "Perpetuum Mobile," dedicated to the sensor-node application [9]. A block diagram and die photo are shown in Figs. 9 and 10. A two-stage level shifter was used between the SOTB ULV and bulk I/O circuits. The standby leakage of the chip was significantly reduced by the back-bias regardless of temperature (Fig. 11). This chip operated at V_{dd} = 0.35 V and consumed only E = 13.4 pJ (Figs. 12 and 13). Note that the E values for the SOTB and bulk at $V_{dd} \geq$ 0.8 V are identical because the values are determined by E_{ac} (depending on the load capacitance). The sleep current was only 0.14 μA. We demonstrated sensor-node operation. The CPU was operated with a single PV cell at <0.4 V. Temperature and acceleration were monitored, and only in an emergency (health problems), an alert was sent via Bluetooth low energy (BLE) to a tablet.

Acknowledgment

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References

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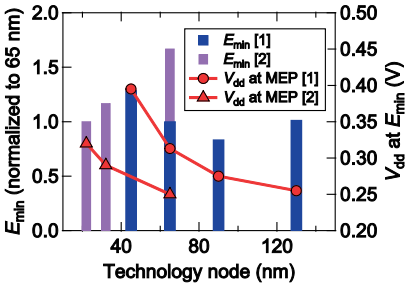

Fig. 1 Minimum energy E_{min} and V_{dd} at MEP as function of technology-node number

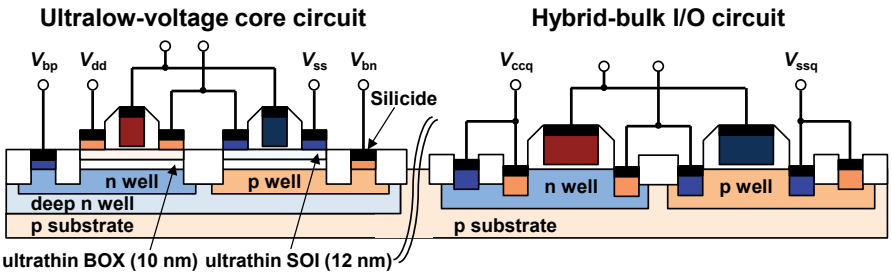

Fig. 2 Schematic cross section of SOTB/bulk hybrid CMOS

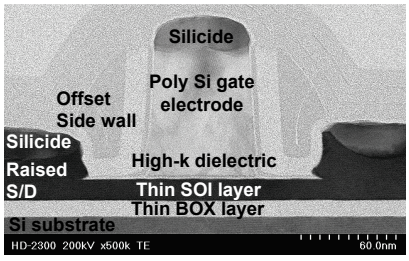

Fig. 3 Cross-sectional TEM image of SOTB transistor

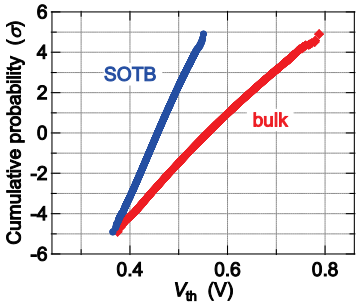

Fig. 4 V_{th} distribution of 1M transistors

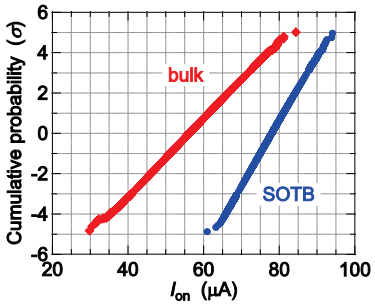

Fig. 5 I_{on} distribution of 1M transistors

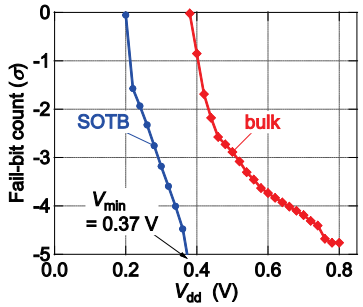

Fig. 6 Fail-bit count of 2-M bit SRAM array as function of V_{dd}

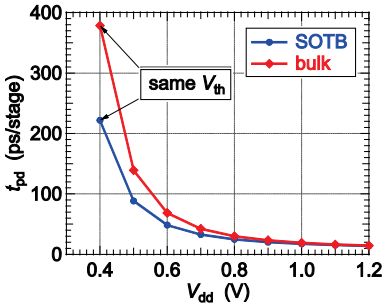

Fig. 7 Inverter delay t_{pd} as function of V_{dd}

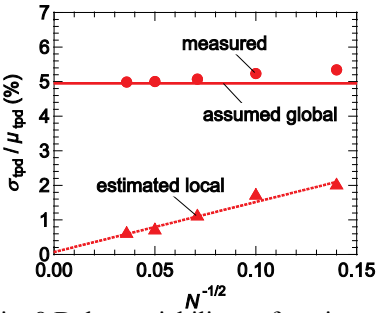

Fig. 8 Delay variability as function of number of RO stages

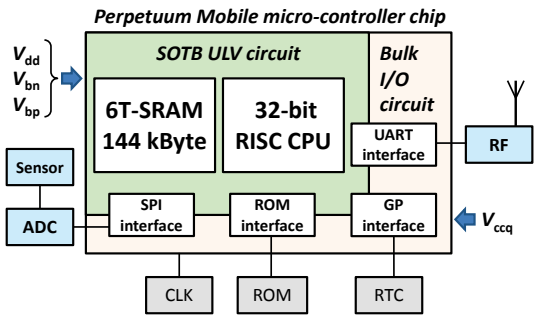

Fig. 9 Block diagram of Perpetuum Mobile micro-controller chip for sensor-node application

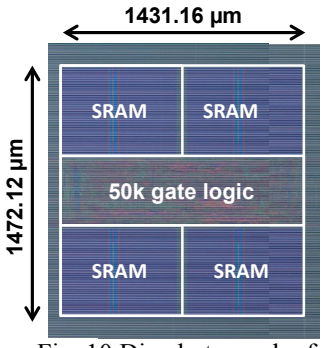

Fig. 10 Die photograph of Perpetuum Mobile CPU

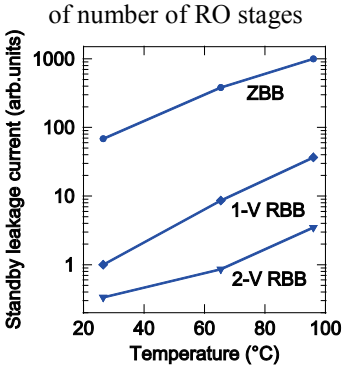

Fig. 11 Standby leakage reduction of CPU logic by reverse back bias

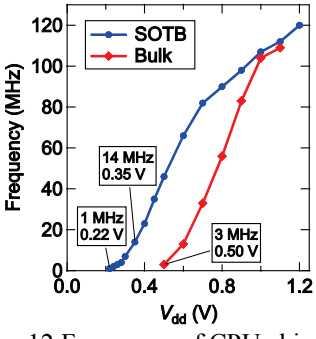

Fig. 12 Frequency of CPU chip as function of V_{dd}

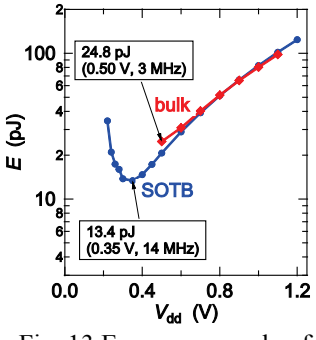

Fig. 13 Energy per cycle of CPU chip as function of V_{dd}

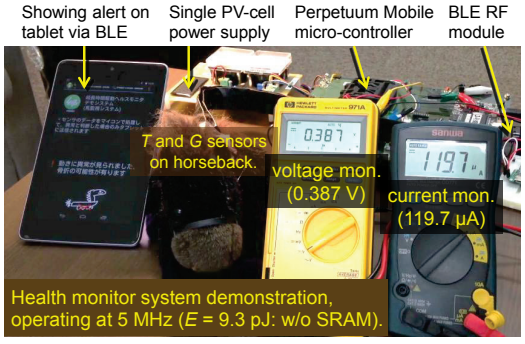

Fig. 14 Photograph of sensor-node system setup. Event driven operation is demonstrated.