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Initial and long-term frequency degradation of ring oscillators caused by plasma-induced damage in 65 nm bulk and fully depleted silicon-on-insulator processes

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The degradation of reliability caused by plasma-induced damage (PID) has become a significant concern with the miniaturization of device size. In particular, it is difficult to relieve PID in silicon-on-insulator (SOI) because it contains buried oxide (BOX) layers. In this work, we compare PID between a bulk and a silicon on thin BOX (SOTB), which has BOX layers of less than 10 nm. We measure frequencies of ring oscillators with an antenna structure on a single stage. In the bulk, PID is relieved by first connecting an antenna to a drain because electric charge flows to a substrate. The difference in initial frequency is 0.79% between structures, which cause and relieve PID. SOTB also relieves the same amount of PID. Initial frequencies are affected by PID, but there is no effect of PID on the long-term degradation mainly caused by bias temperature instability (BTI).

1. Introduction

As the device size of LSI decreases, LSI reliability also decreases. In particular, the degradation of reliability caused by plasma-induced damage (PID) has become a significant concern with the miniaturization of device size because it is inevitable.[1–4] In the worst case, PID breaks the gate oxide of MOSFETs. Silicon fabricators define an antenna rule so as not to break MOSFETs. If a designer does not violate the antenna rule, MOSFETs work normally. However, PID generates defects in the gate oxide even if the designer obeys the antenna rule. Defects increase the threshold voltage (V_{th}), degrade device performance, and cause bias temperature instability (BTI).[5–19] We evaluate the relationship between PID and oscillation frequency. We fabricate a chip including ring oscillators with an antenna structure on a single stage and measure the initial and long-term frequencies of the ring oscillators.

In Sect. 2, we describe PID. In Sect. 3, we explain the circuits for evaluating PID. In Sect. 4, we show the measurement results. In Sect. 5, we conclude this paper.

2. Degradation caused by plasma-induced damage

An antenna is a metal wire that collects charge in the plasma etching process. During the production of MOSFETs, an aluminum wire collects charge because it is processed by plasma etching directly. Although a copper wire is not processed by plasma etching, it collects static charge, as shown in Fig. 1. Charge is induced in a metal wire when an interlayer dielectric around metal wires is processed. PID appears when an antenna is connected to a gate of MOSFETs, as shown in Fig. 2. V_{th} and gate leakage current are increased by PID because defects are generated in a gate oxide.[20–24] V_{th} increases when defects trap carriers. It is called the atomistic trap-based BTI model,[5–10] as shown in Fig. 3. These defects have a time constant (τ) ranging from 10^{-9} to 10^{9} s. Defects with small time constants affect the initial frequency and those with large time constants affect aging degradations such as BTI.[5–19]

There are several methods of relieving PID. Figure 4 shows one of those methods using the drain of a bulk as a discharge path. A tunneling current flows when a high reverse voltage is applied to a PN junction. By first connecting an antenna to the drain, charge flows to a substrate through the drain because the drain and substrate regions form the PN junction. A high electric field is applied by a charge collected in the antenna. However, the silicon-on-insulator (SOI) does not relieve PID in the drain because it has buried oxide (BOX) layers embedded on a wafer between a body and a substrate.[25] Charge remains in the drain and flows to another gate of MOSFETs. We use a silicon on thin BOX (SOTB) to evaluate the PID of the SOI process. SOTB is a type of fully depleted SOI (FD-SOI) process.[26–30] It reduces variations due to impurities because it does not add any dopant to a channel of MOSFETs. A special feature of SOTB is that the BOX layer is less than 10 nm. SOTB may

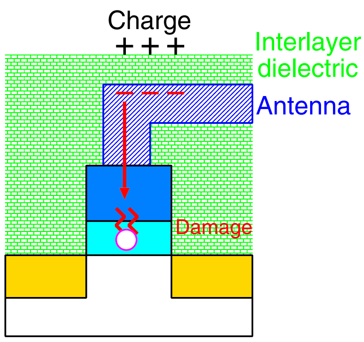

Fig. 1. (Color online) PID by interlayer dielectric processes.

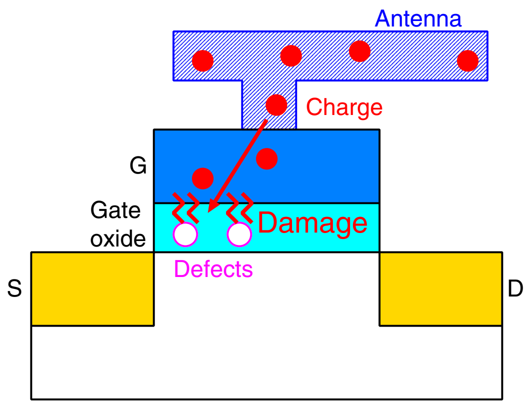

Fig. 2. (Color online) PID of the gate oxide.

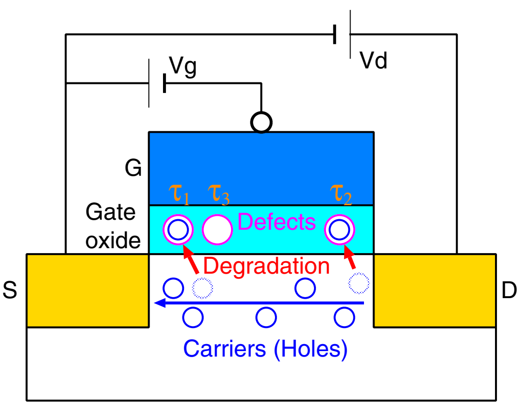

Fig. 3. (Color online) Atomistic trap-based BTI model.

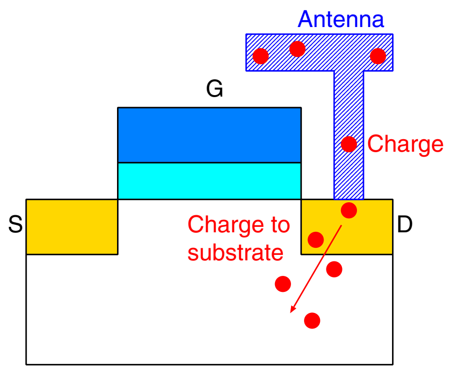

Fig. 4. (Color online) Relieving PID in the drain of bulk.

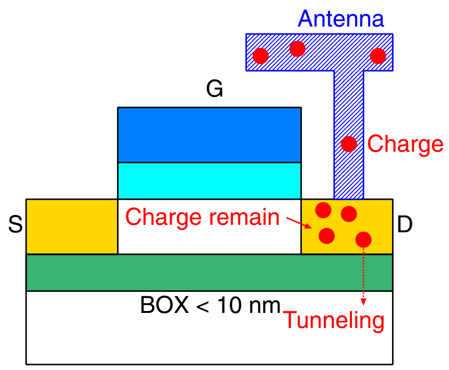

Fig. 5. (Color online) Charge remaining in the drain of SOTB.

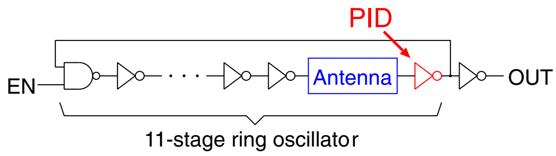

Fig. 6. (Color online) 11-stage ring oscillator for measuring frequencies.

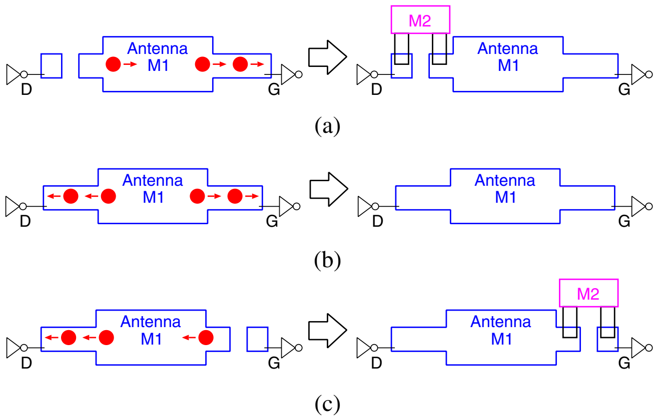

Fig. 7. (Color online) Connection structures of antennas. (a) AG structure. (b) ADG structure. (c) AD structure.

relieve PID because charge flows to the substrate by quantum tunneling, as shown in Fig. 5. We compare PID in the bulk with that in the SOTB.

3. Measurement circuits

We fabricated a chip including 11-stage ring oscillators (ROs) that have different antenna structures in 65 nm bulk and SOTB processes. Note that the layout patterns are exactly the same in both processes except for the BOX layer. Figure 6 shows the 11-stage ROs. The inverter next to the antenna is degraded by PID.

Figure 7 shows connection structures of antennas. M1 and M2 are the first- and second-level metal wires, respectively. AG (antenna is connected to the gate first) causes PID because all charge of the antenna flows to the gate. ADG (antenna is connected to the drain and gate simultaneously) relieves PID to some extent because a certain amount of charge flows to the substrate through the drain. AD (antenna is connected to the drain first) relieves PID at most because most of the charge flows to the substrate through the drain. However, in ADG and AD, SOTB may have PID because of BOX layers.

The antenna ratio (AR), which is the area of an antenna divided by the area of a gate, is correlated to the damage caused by plasma. The upper limit of AR is 500 in the antenna rule. According to the antenna rule, ADG relieves PID 0.08 times. The PID of AR 6250 ADG will be the same as that of AR 500 AG. We consider that AR values are 500 and 6250 on the basis of that rule.

4. Results and discussion

We measure average frequencies from both bulk and SOTB chips. One chip contains 98 ROs of the same structure.

4.1 Initial frequency

We measure the initial frequencies of ROs at 25 °C and 1.2 V. We calculate the frequency ratio (FR) on the basis of the frequency of simulation using the following equation:

$$\mathrm{FR} = \frac{F_{\mathrm{meas}} - F_{\mathrm{sim}}}{F_{\mathrm{sim}}}. \tag{1}$$

Here, FR is the frequency ratio based on the frequency of simulation. F_{meas} is the average frequency of measurement. F_{sim} is the frequency of simulation on each structure.

We simulate frequencies of ROs including only resistance and capacitance (RC). The frequencies before an inverter is damaged by plasma are different among antenna structures because the metal wire connections of the last stage are

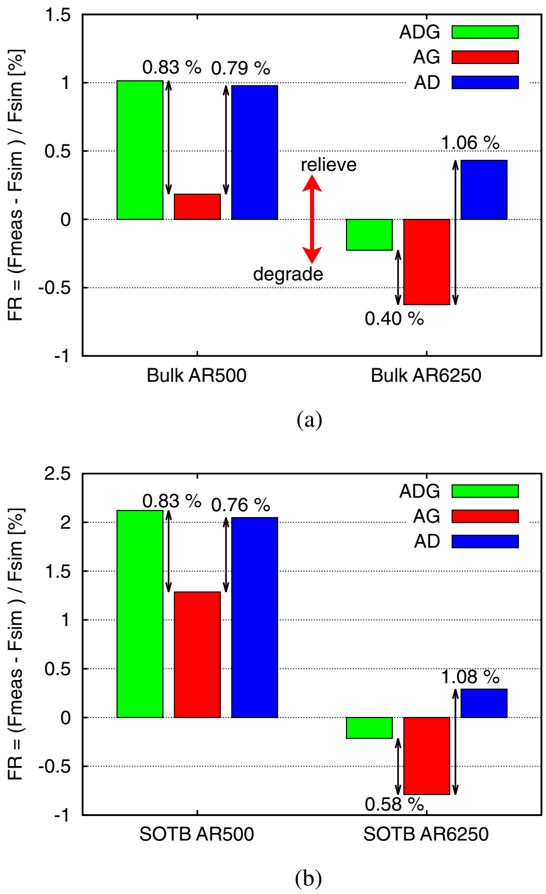

Fig. 8. (Color online) Comparison of initial FR with measurement and simulation results. (a) Bulk. (b) SOTB.

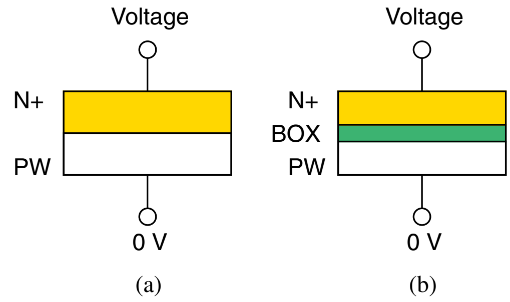

Fig. 9. (Color online) Circuits for measurement of substrate leakage. (a) Bulk. (b) SOTB.

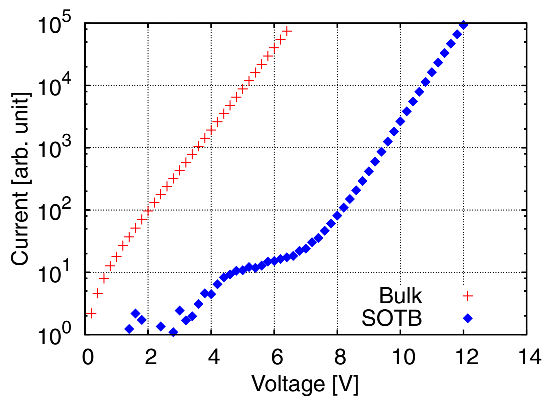

Fig. 10. (Color online) Results of substrate leakage measurement.

different. We extract parasitic components from a layout. We obtain frequencies from circuit-level simulations using these parasitic components. These frequencies are compared with the measured ones. If PID is larger, the difference between them is also larger. This difference in frequency among antenna structures originates from only the RC of the wire connection in the antenna.

We assume that AG structures are damaged by the same amount both in the bulk and SOTB structures because the gate structures are the same between these structures. If AD or ADG structures are damaged by the same amount, the FR is equivalent to AG. If they relieve PID larger than the AG, the FR is above the AG.

Figure 8(a) shows a comparison of initial frequencies with measurement and simulation results in the bulk. Its vertical axis is FR. The bar graph on the left side is AR500 in the bulk. The right side one is AR6250 in the bulk. The FRs of ADG and AD are increased by 0.83 and 0.79% from the AG in AR500, respectively. PID is relieved in AR500 by connecting an antenna to the drain. The frequency of the ADG structure is relieved by 0.40% in AR6250. It does not sufficiently relieve PID in AR6250. However, the AD structure relieves PID by 1.06%. It relieves PID more than the ADG. PID is more relieved by the antenna connected to the drain first (AD) than by that connected to the drain and gate at the same time (ADG).

Figure 8(b) shows results of initial frequencies in the SOTB chip. ADG and AD relieve PID by 0.83 and 0.76% in AR500, respectively. These values are 0.58 and 1.08% in AR6250, respectively. Both structures have almost the same values as the bulks. SOTB can relieve PID by connecting an antenna to a drain, the same as the bulk. We assume that charge flows to the substrate by quantum tunneling. PID occurs at a gate oxide thickness less than 11.6 nm.[31,32] Charge can pass through a smaller gate oxide thickness if a high electric field is applied to the BOX layer. A flash memory with a gate oxide thickness less than 10 nm also uses quantum tunneling by applying a high electric field.[33] During the production of MOSFETs, a high electric field is applied to the BOX layer by a charge collected in the antenna. Thus, charge can flow to the substrate through the drain by quantum tunneling in the thin BOX layer.

We measure the substrate leakages of the SOTB and bulk. Figure 9 shows the circuits used for the measurement of substrate leakage. The voltage of the substrate is 0 V. We measure currents between the drain (N+ region) and the substrate by changing the drain voltage. Figure 10 shows the results of the measurement of substrate leakage. These results are the averages of five transistors. Both substrate leakages of the bulk and SOTB start to increase from more than 2 V. Although the leakage current is too low to cause any problem in nominal operations, charge can pass through the thin BOX layer by quantum tunneling. Thus, the SOTB can relieve PID by connecting the antenna to the drain, the same as the bulk. The thin BOX layers of 10 nm in SOTB are also effective in relieving reliability issues besides the back bias controllability.

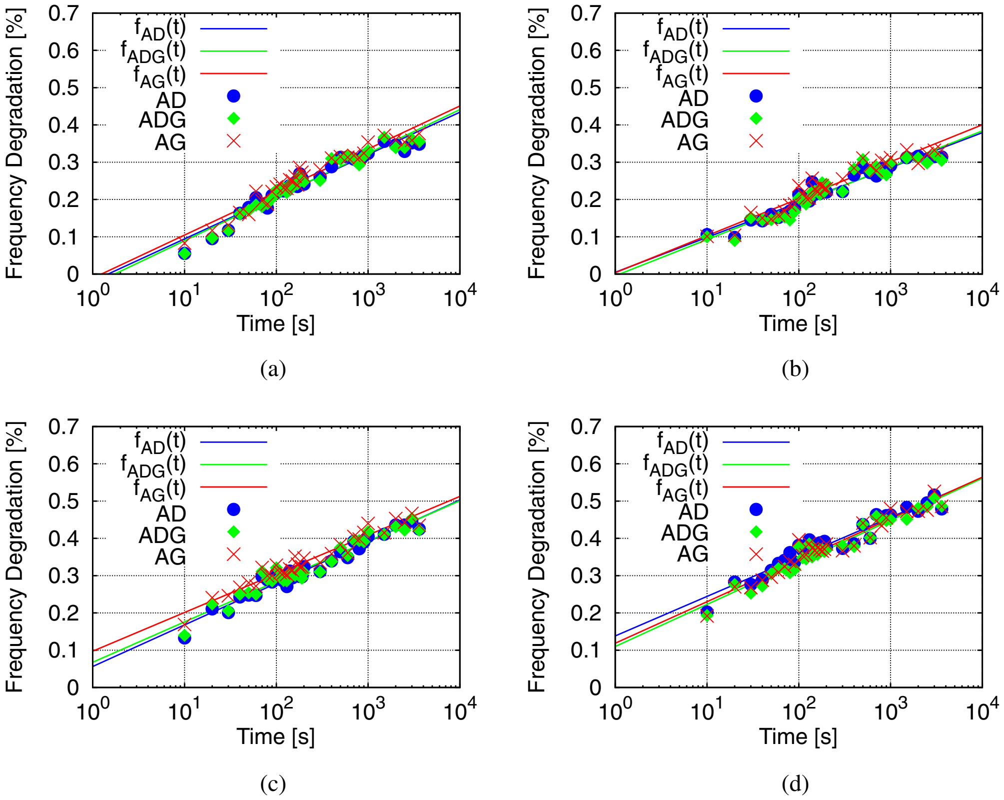

Fig. 11. (Color online) Results of measurement of long-term degradation. (a) Bulk in AR500. (b) Bulk in AR6250. (c) SOTB in AR500. (d) SOTB in AR6250.

Table I. Fitting parameter a of values all structures.

	AG	ADG	AD
AR500:Bulk	0.0501	0.0509	0.0492
AR6250:Bulk	0.0431	0.0422	0.0407
AR500:SOTB	0.0451	0.0470	0.0485
AR6250:SOTB	0.0484	0.0490	0.0461

4.2 Long-term frequency (BTI)

We measure the BTI degradation of ROs. The measurement temperature is 80 °C to accelerate BTI degradation by the temperature. The inverter connected to an antenna is stressed by BTI when EN is "0". We keep EN as "0" except when measuring the oscillation frequencies of the ROs. We keep EN as "1" when measuring frequencies. Frequency degradation is based on the initial average frequency of each structure by calculating the following equation:

$$\text{Frequency degradation} = \frac{F_0 - F(t)}{F_0}. \tag{2}$$

F_0 is the initial frequency at $t = 0$ and $F(t)$ is the frequency at each time t.

Figures 11(a) and 11(b) show BTI degradations in the bulk process. Their vertical axis is the frequency degradation and their horizontal axis is the stress time. The points are measurement frequencies and the solid lines are along the fitting functions of $f = a \cdot \log t + b$. If the fitting parameter a is larger, degradation is larger. Table I shows the fitting parameter a values of all the structures. The a values of AG, ADG, and AD in AR500 are 0.0501, 0.0509, and 0.0492, respectively. These a values are almost similar to those of antenna structures in the bulk process.

Figures 11(c) and 11(d) show BTI degradations in the SOTB process. These results are almost the same as those in the bulk process. There is no effect of PID on the long-term degradation rate. It might be considered that defects with large time constants are not generated by PID.

5. Conclusions

We fabricated ring oscillators with an antenna structure in 65 nm bulk and SOTB processes and measured their frequencies. The AD structure relieves PID by 1.06% in the bulk of AR6250. In SOTB, the AD structure relieves PID by 1.08%. Both bulk and SOTB relieve PID by connecting an antenna to a drain. We assume that charge passes through thin BOX layers of less than 10 nm by quantum tunneling. The BTI degradations are almost similar to those of antenna structures. Initial frequencies are affected by PID, but there is no effect of PID on the long-term degradation. We assume that defects with small time constants are generated, but those with large time constants are not generated by PID.

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