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Radiation-Hardened Flip-Flops with Low-Delay Overhead Using PMOS Pass-Transistors to Suppress SET Pulses in a 65 nm FDSOI Process

Kodai Yamada, *Member, IEEE,* Haruki Maruoka, Jun Furuta, *Member, IEEE,* Kazutoshi Kobayashi, *Member, IEEE*

***Abstract*—In this paper we propose radiation-hardened flip-flops (FFs) based on the adaptive coupling FF (ACFF) with low dynamic power and short delay overhead in a 65 nm fully depleted silicon on insulator (FDSOI) process. We designed four FFs composed of a master latch with PMOS pass-transistors to reduce a delay time overhead and a slave latch with stacked transistors for high soft-error tolerance. We evaluated the radiation hardness of the newly designed FFs using TCAD simulations, α particle test and neutron irradiation test. TCAD simulations show that the proposed structure has enough radiation hardness against secondary particles generated by neutrons. The α irradiation results show that error probabilities of the proposed FFs are 1/400 - 1/130 smaller than conventional radiation-hardened stacked FF. Neutron irradiation results show that soft error rates of the proposed FFs are 1/16 - 1/7 lower than stacked FF. No significant differences in soft-error tolerance was observed in any of the proposed FFs under all static conditions. The experimental results suggest that PMOS pass-transistors can effectively suppress soft errors in terrestrial regions with a low-delay overhead.**

***Index Terms*—soft error, α particle, neutron, FDSOI, flip-flop, low delay overhead, pass-transistor, stacked transistor.**

I. Introduction

Highly-reliable semiconductor chips are crucial for autonomous and assisted driving. Continuous technology downscaling has resulted in soft errors becoming a significant threat to the reliability of semiconductor chips. These soft errors are mainly caused by α particles from packages or neutrons from cosmic rays in terrestrial regions.

Radiation-hardened flip-flops (FFs) that withstand soft errors are frequently used in highly-reliable chips. Triple modular redundancy (TMR) [1] and dual interlocked storage cell (DICE) [2][3] are widely used. Radiation-hardened FFs with small overheads are ideal, however, TMR and DICE, have larger delay, area and power overheads than conventional FFs. Fully-depleted silicon on insulator (FDSOI) is a device-level mitigation technique that prevents soft errors without any delay, area and power penalties. Single event latch-up (SEL) does not occur in FDSOI processes, because there is no parasitic bipolar structure [4]. FDSOI also has 50x - 110x higher tolerance for soft errors than bulk, because buried oxide (BOX) layers prevent charge from being collected from substrate [5].

In this paper, we propose four radiation-hardened FFs with small dynamic power and short delay overheads especially for FDSOI processes [6]. We evaluated the radiation hardness of the proposed FFs using TCAD simulations, α particle test and neutron irradiation test. Section II explains the circuit structure of a low-power FF and proposed FFs. Section III shows the results of TCAD simulations. Section IV shows the results by α particle and spallation neutron irradiation tests. Section V concludes this paper.

K. Yamada, H. Maruoka, J. Furuta and K. Kobayashi are with the Graduate School of Science & Technology, Kyoto Institute of Technology (e-mail: kyamada@vlsi.es.kit.ac.jp, kazutoshi.kobayashi@kit.ac.jp).

II. Radiation-Hardened Flip-Flops

Conventional transmission gate FF (TGFF) has very low resistance to soft errors (Fig. 1). Adaptive coupling FF (ACFF) [7] has a lower dynamic power than TGFF, because it lacks a local clock buffer (Fig. 2). ACFF has AC elements, in which PMOS and NMOS transistors are connected in parallel to easily overwrite a stored value of the master latch (ML). Although they prolong delay time, they suppress single

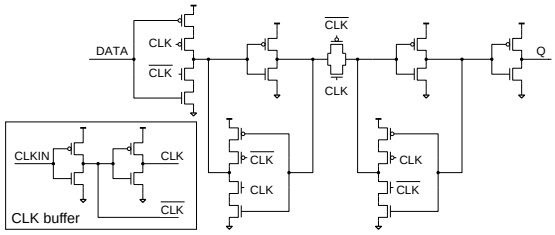

Fig. 1. Transmission-gate FF (TGFF).

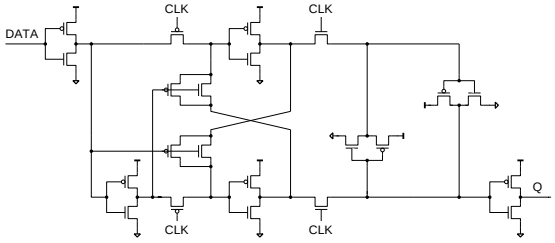

Fig. 2. Adaptive Coupling FF (ACFF).

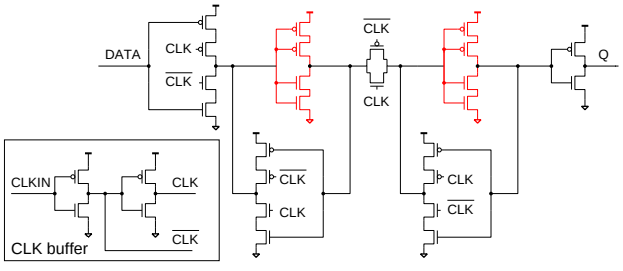

Fig. 3. Stacked FF.

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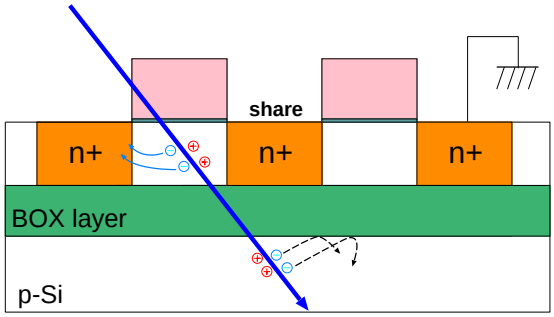

Fig. 4. The cross section of NMOS transistors in stacked inverters.

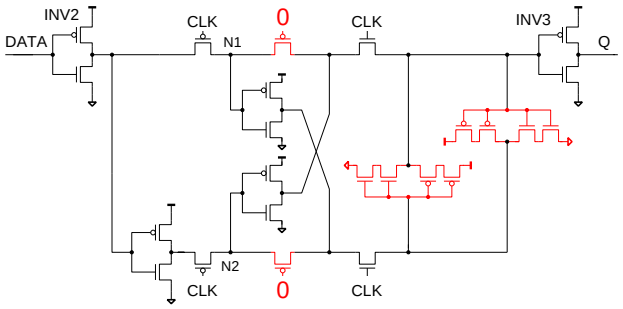

Fig. 5. Pulse Blocking Low Dynamic Power FF (PBLDPFF).

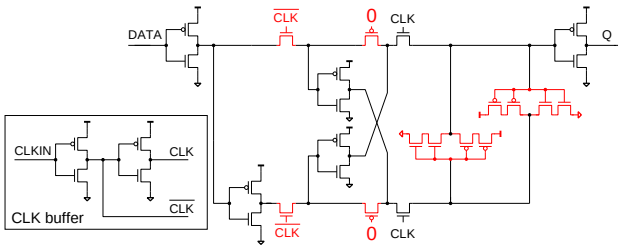

Fig. 6. Pulse Blocking FF (PBFF).

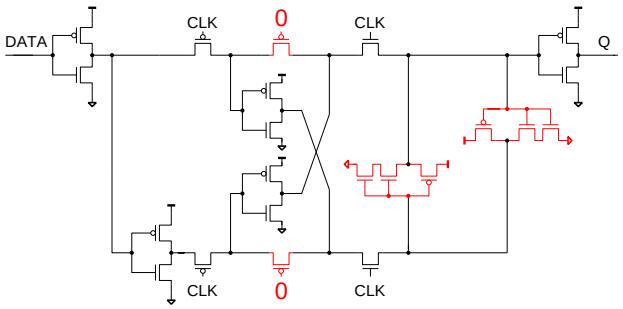

Fig. 7. Pulse Blocking Low Dynamic Power FF with Stacked NMOS (PBLDPFF_SN).

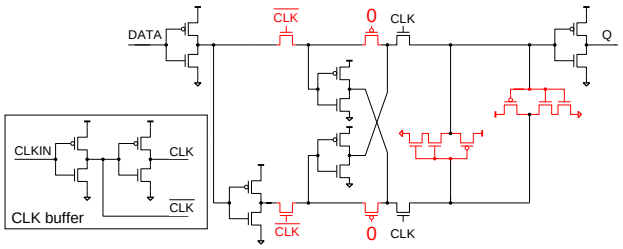

Fig. 8. Pulse Blocking FF with Stacked NMOS (PBFF_SN).

event transient (SET) pulses when CLK = 1 [8]. NMOS pass-transistors suppress SET pulses from PMOS transistors in INV0 and INV1 inverters, while PMOS pass-transistors suppress SET pulses from NMOS transistors. Transistors in FDSOI processes decrease charge collection volume less than the bulk and partially depleted SOI (PDSOI) processes because sensitive volume is fully isolated by a BOX layer and shallow trench isolation (STI) in FDSOI. Larger sensitive volume means higher soft error rates because a particle hit generates more charge. Large charge collection perturb the drain voltage when particle hits on pass-transistors, which cause soft errors. Thus the pass gate technique is effective in FDSOI. In PDSOI, the pass gates is less effective than FDSOI because the sensitive volume in PDSOI is bigger than that in FDSOI. However, the slave latch (SL) consists of two mutually-connected inverters without any transistors between them. To guarantee the radiation hardness of ACFF, the SL must be resilient. In fact, we observed higher radiation-hardness as expected in another version of ACFF in which the weak SL was simply replaced with a strong stacked-latch similar to the structure described in the next section [8]. However, we also found that this simple replacement resulted in a larger overhead than the original version. Another approach to reduce overheads is desired.

A. Conventional Radiation-Hardened Flip-Flop for SOI

Stacked FF [9] has inverters in latches composed of two series-connected NMOS and PMOS transistors (Fig. 3). As shown in Fig. 4, stacked transistors in FDSOI are isolated by a BOX layer and STI as we mentioned, while they are connected through substrate in bulk. When a radiation particle hits the stacked inverter, its output does not flip unless both of NMOS transistors are influenced at the same time. Thus stacked FF is also strong against soft errors in FDSOI. However the downside is that stacked structures have 1.52x larger area and 1.97x delay overheads than the conventional inverter.

B. Proposed Radiation-Hardened Flip-Flops for SOI

1) Circuit Structure: We propose four ACFF-based radiation-hardened FFs that have high soft-error tolerance and short delay time using PMOS pass-transistors. The pass transistors are conventionally used to reduce overheads but are not used to suppress SET pulses. We combine with the pass transistor technique and the FDSOI process for radiation-hardened structures. In Fig. 5, the proposed FF named pulse blocking low dynamic power FF (PBLDPFF) is shown. NMOS transistors are weaker against soft errors than PMOS transistors mainly due to differences in mobility[10]. Pass-transistors between inverters suppress SET pulses from inverters. PMOS pass-transistors are better at suppressing SET pulses because they can suppress SET pulses from NMOS transistors which are more frequent than those from PMOS transistors. The ML of our newly designed PBLDPFF has PMOS pass-transistors so it suppresses SET pulses from NMOS transistors. The PMOS pass-transistors have a shorter delay time overhead than AC elements because they are always in an ON-state. The SL is composed of stacked inverters and has a small impact on delay time because the ML is directly connected to INV3 through the NMOS pass-transistors. However, PBLDPFF has

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N1 or N2 node that exceeds the threshold voltage in all static conditions. In Fig. 6, the proposed FF named pulse blocking FF (PBFF) is shown. PMOS pass-transistors between the ML and INV2 in the PBFF are replaced with NMOS pass-transistors to stabilize the potential on N1 and N2 nodes. However, it needs a local clock buffer. Figures 7 and 8 depict the PBLDPFF with stacked NMOS described as PBLDPFF_SN and PBFF with stacked NMOS called PBFF_SN. Both FFs have stacked inverters in the SL composed of two NMOS and one PMOS transistors because latter is more resilient against soft errors. PBLDPFF contains different numbers of PMOS and NMOS transistors that generate an unoccupied area while PBLDPFF_SN contains the same number of PMOS and NMOS transistors. Thus PBLDPFF_SN is smaller than PBLDPFF. We evaluated whether the stacked inverter consisting of stacked NMOS and unstacked PMOS transistors was strong against soft errors. The ML and SL of four proposed FFs have symmetrical structures with stacked inverters while those of the stacked FF have asymmetrical structures with tristate inverters. It is presumed that proposed FFs have high soft error tolerance because stacked inverters are stronger than tristate inverters.

2) Performance of Proposed Flip-Flops: In order to compare the circuit performance of the proposed FFs, we used the downhill simplex method [11] to optimize transistor sizes in PBFF and PBLDPFF except for output inverter. Changing the transistor size minimizes ED (Energy Delay) product, however we did not change the transistor width in SN structures: instead, we removed two PMOS transistors from non-SN structures.

We measure D-Q delay and power consumption in FFs using SPICE simulation at a supply voltage (V_{DD}) of 1.2 V in a 65 nm FDSOI process with a thin BOX layer. Circuit A and B were used to evaluate power consumption (Fig. 9). Table I shows the simulation results of delay time, dynamic power at 10% data activity, static power, area and the number of transistors. All values except for the number of transistors are normalized to those of TGFF. The values in parentheses are normalized to those of stacked FF.

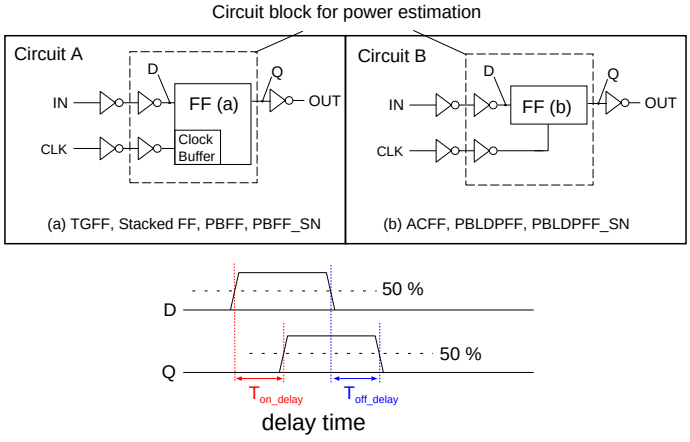

Fig. 9. Circuit structures to evaluate power consumption and D-Q delay. Circuit A and B were used to evaluate power consumption. An average of T_{on_delay} and T_{off_delay} is D-Q delay.

TABLE I
SIMULATION RESULTS AT V_{DD} = 1.2 V OF D-Q DELAY, POWER ,AREA AND NUMBER OF TRANSISTOR OF EACH FF. ALL VALUES EXCEPT FOR THE NUMBER OF TRANSISTORS ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKED FF.

FF	D-Q delay	Power consumption		Area	# of Tr.	
		Dynamic	Static		NMOS	PMOS
TGFF	1	1	1	1	12	12
DICEFF	1.24	1.84	2.47	2.35	28	28
TMRFF	1.61	2.99	4.06	6.12	54	54
ACFF	1.46	0.470	2.35	1.00	11	11
Stacked FF	1.66	1.02	1.13	1.12	14	14
PBFF	1.19 (0.72)	0.872 (0.86)	0.926 (0.82)	1.47 (1.31)	15	13
PBFF_SN	1.17 (0.71)	0.872 (0.86)	0.970 (0.86)	1.47 (1.31)	15	11
PBLDPFF	1.30 (0.78)	0.488 (0.48)	38.9 (34.4)	1.29 (1.15)	11	13
PBLDPFF_SN	1.38 (0.83)	0.483 (0.47)	41.8 (37.0)	1.18 (1.05)	11	11

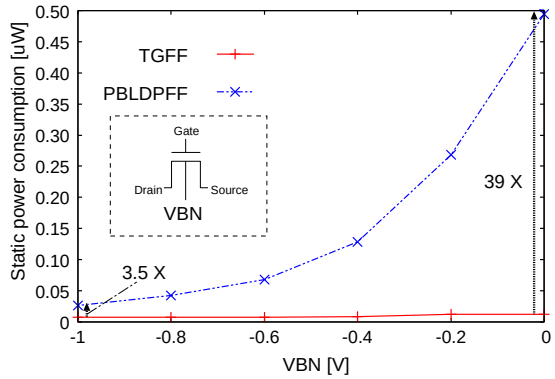

Fig. 10. The static power of PBLDPFF depending on substrate bias (VBN) of NMOS transistors.

Radiation-hard FFs by duplication or triplication and voting, such as the TMRFF or DICEFF, have an area and power consumption overhead that is 2x - 3x larger than TGFF.

Stacked FF has a 1.66x longer delay time than TGFF because stacked inverters both in the ML and the SL lengthen its delay time. The proposed FFs have a 5.58% - 19.9% shorter delay time than ACFF. This is because PMOS pass-transistors are always ON-state in the proposed FFs while a PMOS transistor and an NMOS transistor in the AC element alternately repeat ON-state and OFF-state in response to the stored value. This switching time provides the longer delay time of ACFF. PBFF provides an 8.46% shorter delay time than PBLDPFF. PBFF has NMOS pass-transistors between the ML and INV2, while the PBLDPFF has only PMOS pass-transistors. The NMOS pass-transistors used in the tested circuits had a higher drive current than the PMOS pass-transistors. The N1 or N2 node that exceeds the threshold voltage in PBLDPFF worsen the delay overhead when INV3 changes its output.

The dynamic and static power of PBFF and PBFF_SN are relatively similar to that of TGFF. As well, the dynamic power of PBLDPFF and PBLDPFF_SN are relatively similar to that of ACFF. This is because PBLDPFF and PBLDPFF_SN have no local clock buffer. However, their static power is about

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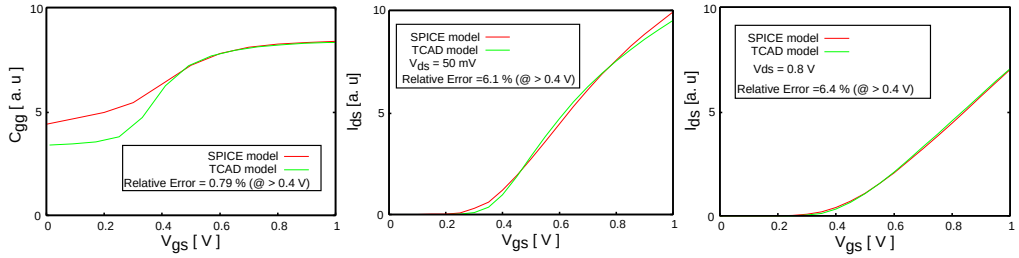
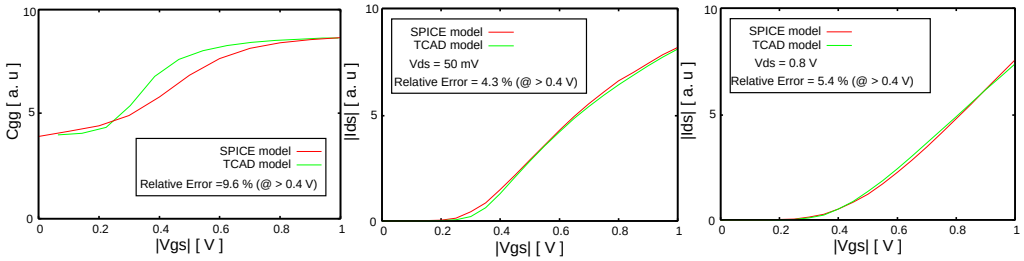


(a) NMOS transistor



(b) PMOS transistor

Fig. 11. (1) Simulated $C_{\rm gg}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 0 V. (2) Simulated $I_{\rm ds}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 50 mV. (3) Simulated $I_{\rm ds}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 0.8 V. Characteristics on TCAD simulations are optimized to decrease the relative error between TCAD simulations and SPICE simulation to less than 9.6 % in region of $|V_{\rm gs}| > 0.4$ V.

TABLE II
SYNTHESIZED AREA OF A 32-BIT MICRO CONTROLLER NORMALIZED BY THE TGFF.

	TGFF	PBFF
Conmbinational	0.70	0.69
Flip-flops	0.30	0.38
Total	1.00	1.07

40x higher than that of TGFF, because some nodes exceed the threshold voltage in static conditions. It is possible to suppress the static power of PBLDPFF by applying back bias to the body of NMOS transistors as shown in Fig. 10. The static power of PBLDPFF is reduced by 90% at the substrate bias (VBN) of -1 V on NMOS transistors. Since the threshold of NMOS transistors at VBN = -1 V is 1.5x higher than that at VBN = 0 V, short-circuit current through the inverter is decreased. The static power of PBLDPFF is reduced by 70% when PMOS pass-transistors of the ML are replaced with low-threshold transistors. Radiation hardness is described in Section III and Section IV.

The proposed FFs have bigger area overheads than TGFF. This is because the proposed FFs except for PBLDPFF_SN contain different numbers of PMOS and NMOS transistors that generate an unoccupied area as we mentioned in section II B. 2). Although PBLDPFF_SN has the smaller number of transistors than TGFF, PBLDPFF_SN is bigger than TGFF. Proposed FFs has more contacts and fewer shared diffusions of transistors than TGFF. A 32-bit micro controller is synthesized from Register Transfer Level (RTL) using PBFF or TGFF. Table II shows the synthesized results. The total area with PBFF is only 7% bigger than the conventional area although the area of PBFF is 47% bigger.

III. TCAD Simulation Analyses

Three-dimensional TCAD simulations are carried out using the Synopsys Sentaurus to evaluate the radiation hardness of the ML in the proposed FFs.

A. Simulation Setup

We constructed three-dimensional structures in a 65 nm FDSOI process with a thin BOX layer for TCAD simulations. The capacitance-voltage ($C_{\rm gg}$-$V_{\rm gs}$) and current-voltage ($I_{\rm ds}$-$V_{\rm gs}$) of the transistor on TCAD simulations were adjusted to match those on SPICE simulation which are calibrated with real devices. We calibrated $C_{\rm gg}$-$V_{\rm gs}$ curve by changing the work function of the poly-silicon gate and the gate oxide thickness. Figure 11 (1) shows $C_{\rm gg}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 0 V on TCAD and SPICE simulations. By changing the surface roughness and phonon scattering parameters to affect transistor mobility, we calibrated the $I_{\rm ds}$-$V_{\rm gs}$ curve in the linear region. Figure 11 (2) shows the $I_{\rm ds}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 50 mV on TCAD and SPICE simulations. We calibrated the $I_{\rm ds}$-$V_{\rm gs}$ curve in the saturated region by changing the saturation velocity. Figure 11 (3) shows the $I_{\rm ds}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 0.8 V on TCAD and SPICE simulations. The relative errors between these simulations were calculated at each characteristic and described in Fig. 11. Characteristics on TCAD simulations were optimized to decrease the relative error between TCAD simulations and SPICE simulation to less than 9.6 % in the region of $|V_{\rm gs}| > 0.4$ V.

B. Soft-Error Tolerance

Figures 12 (a) and (b) depict the schematic at CLK = 1 and the cross section of devices on the ML. The transistors to upset the stored value in the ML are T1, T2 and T3. We evaluate

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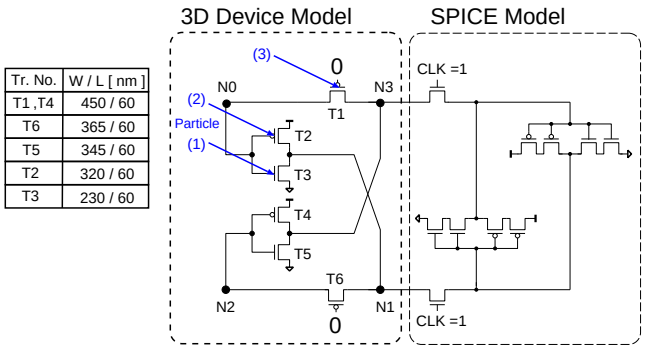
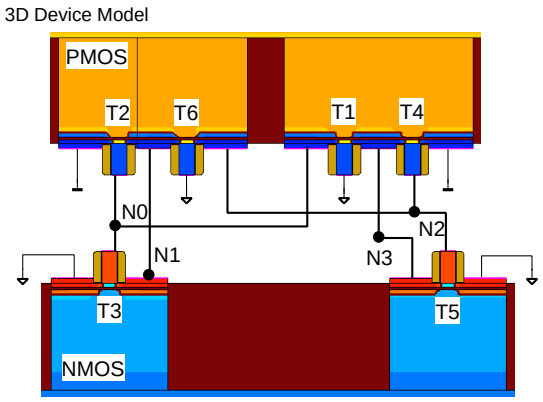


(a) Schematic



(b) Cross section

Fig. 12. Schematic (a) and cross section (b) of devices on the ML. T1, T2 and T3 are respectively injected with heavy ions at V_{DD} = 0.8 V. The transistor width and length are shown on the left side of the schematic.

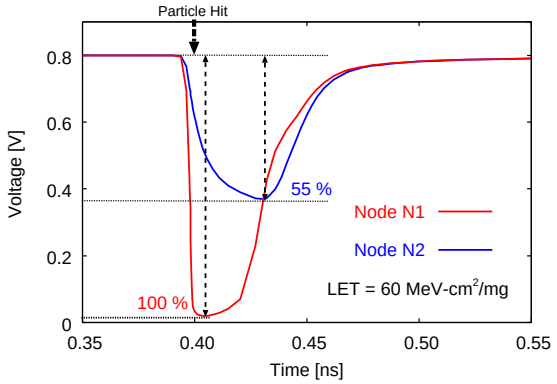
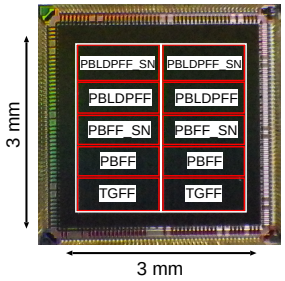


Fig. 13. TCAD simulations results. N1 and N2 are influenced by a particle hits in Fig. 12. The ML of proposed FFs is stable up to LET = 60 MeV-cm^2/mg.

soft error tolerance in outer space on TCAD simulations. These transistors are injected with heavy ions up to a liner energy transfer (LET) of 60 MeV-cm^2/mg since there are more particles in outer space that fall within this range [12]. We investigated the threshold LET value (the minimum LET value at which the latch upsets) at V_{DD} = 0.8 V. The simulation of SEUs caused by a heavy ion impact is achived using a heavy ion model of the Synopsys Sentaurus. The spatial distribution of a charge cloud is defined as a Gaussian function with the standard deviation of 30 nm [13].



Flip-Flop	bit/chip
TGFF	83,520
PBFF	60,320
PBFF_SN	60,320
PBLDPFF	64,960
PBLDPFF_SN	69,600

Fig. 14. Fabricated chips in a 65 nm FDSOI process with a thin BOX layer.

(1) NMOS Transistor, T3: By setting the initial value of N0 to 0, particles hit at T3. The stored value of the latch is not upset even though a particle has LET of 60 MeV-cm^2/mg, which is 10x larger than the threshold LET of the conventional latch under the same condition. Note that the conventional latch was fabricated as follows: We copied the ML TCAD structure as shown in Fig 12 (b) and simply removed T1 and T6 to make a simple (no pass-transistor) cross-coupled inverter latch. In Fig. 13, voltage waveforms of N1 and N2 are shown. The amplitude of the SET pulse is attenuated by 45% after passing through the PMOS pass-transistor. This is because a PMOS pass-transistor cannot pass low levels signal under the threshold voltage.

This latch is also evaluated under the same condition after PMOS pass-transistors of the ML are replaced with low-threshold transistors. There is no upset in the stored value of the latch even though a particle has the LET of 60 MeV-cm^2/mg.

(2) PMOS Transistor, T2: By setting the initial value of N0 to V_{DD}, particles hit at T2. The threshold LET is 26.2 MeV-cm^2/mg. This is about 3x larger than the threshold LET of the conventional latch under the same condition. This is due to the PMOS pass-transistor creating resistance and the SL which keeps the stored value disturbs soft errors in the ML.

(3) PMOS Pass-Transistor, T1: Particles hit at T1 when N0 has the initial value of 0. The stored value of the latch is not upset even though a particle has LET of 60 MeV-cm^2/mg. Parasitic bipolar junction transistor effect (PBE) is the dominant cause of soft errors in FDSOI devices [5]. Although, the PBE in the pass-transistor flows current, it does not influence soft errors rates.

Secondary ions generated by neutrons in Si is up to about 20 MeV-cm^2/mg [14]. These results prove that the proposed ML structures have a high enough resilience to soft-error to make them appropriate for highly-reliable devices in terrestrial regions.

IV. Experimental Results

A. Test Chip

Figure 14 shows the fabricated test chip in a 65 nm FDSOI process. It has 12 nm thick SOI, 10 nm thick BOX layers [15] and is 3.0 × 3.0 mm. Well-contacts were inserted every 104 um to control substrate potential of transistors inside triple-wells. All FFs are serially connected as a shift register.

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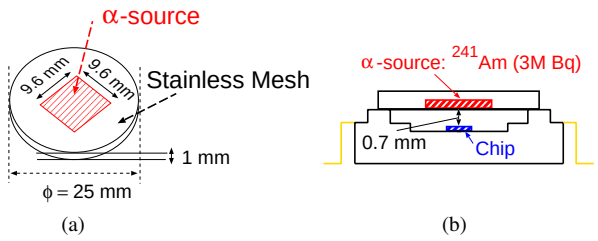


Fig. 15. α source (a) and setup of α particle irradiation test (b). The red mesh shows the α source.

B. α Particle Irradiation

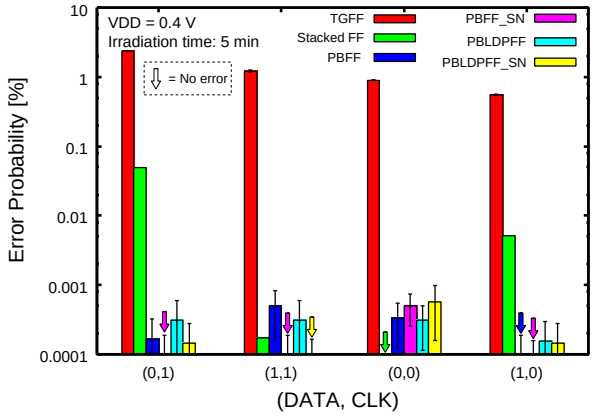
α particle irradiation tests were carried out using a 3 MBq ^{241}Am. Fig. 15 shows the 9.6 $\times$ 9.6 mm α source and the setup of the α particle irradiation test. The distance between the α source and the chip is 0.7 mm. All measurements were done by repeatedly initializing all FFs : the α source was placed on the chip for five minutes and the data were read after removing the α source. We measured the radiation hardness at these static conditions (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1,0) to evaluate all possible states. The error probability (EP) used to evaluate soft-error tolerance was calculated using Eq. 1. Measurements were carried out ten times under each condition and data were the average of these results. The error bars are within 68% confidence.

$$EP = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}}} \quad (1)$$

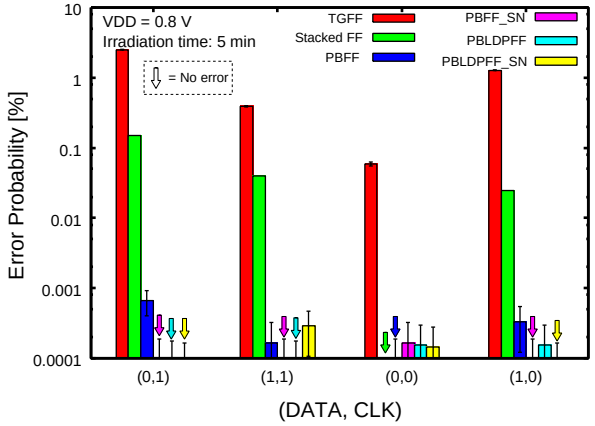
The EP was calculated from the number of errors (N_{error}) and the number of FFs (N_{FF}).

In our previous study [16], which is also based on the 65nm FDSOI structure, the α particle-induced EP increased 18x when the supply voltage was reduced from 1.2 V to 0.4 V. Hence, to increase the number of soft errors in the present study, irradiation tests were carried out at similar lower supply voltage. Figures 16 (a), (b) and (c) show experimental results of α particle-induced EP at V_{DD} = 0.4 V, 0.8 V and 1.2 V respectively. The EPs of stacked FF are from [17]. When CLK = 1, the ML should hold data, while the SL should hold data when CLK = 0. PBFF_SN and PBLDPFF_SN have slave latches which consist of stacked NMOS and unstacked PMOS transistors. No significant differences were observed in the EPs of the four proposed FFs under all static conditions. The maximum N_{error} of all proposed FFs for ten experiments is 2 when V_{DD} = 0.4 V, 1.2 V, and 1 when V_{DD} = 0.8 V out of 60,320 - 69,600 FFs.

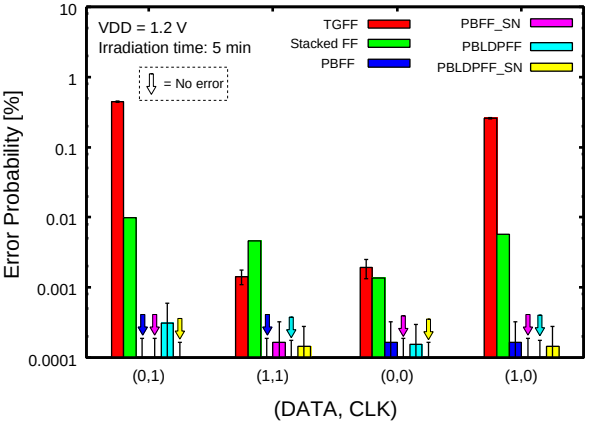
Figures 17 (a), (b) and (c) show the average number of α particle-induced EPs of four static conditions at V_{DD} = 0.4 V, 0.8 V and 1.2 V. When V_{DD} = 0.4 V, the EPs of stacked FF is 1/92 smaller than that of TGFF. The EPs of the proposed FFs are 1/60 - 1/35 smaller than that of stacked FF. When V_{DD} = 0.8 V, the EP of stacked FF is 1/20 smaller than that of TGFF. The EPs of all proposed FFs are 1/400 - 1/130 smaller than that of stacked FF. When V_{DD} = 1.2 V, the EP of stacked FF is 1/33 smaller than that of TGFF. The EPs of all proposed FFs are 1/14 - 1/10 smaller than that of stacked FF. All proposed FFs were more resilient to soft errors by α particle than stacked FF at V_{DD} = 0.4 V, 0.8 V and 1.2 V. We can find that the



(a) V_{DD} = 0.4 V



(b) V_{DD} = 0.8 V



(c) V_{DD} = 1.2 V

Fig. 16. Experimental results of α particle-induced error probabilities under each condition. The α particle-induced error probabilities of the stacked FF are from [17]. The error bars are within 68% confidence. Down arrows mean no error.

EP of stacked FF is dependent on the stored value. This data-pattern-dependence was removed in the four proposed FFs. This is due to the symmetrical structures in the four proposed FFs.

We measured the radiation hardness when VBN = -1 V. Figure 18 shows the experimental results of α particle-induced EPs when V_{DD} = 0.8 V and VBN = -1 V. The EPs of TGFF when VBN = 0 V are 1/100 - 1/10 smaller than that at VBN = -1 V. This is because the reverse body bias suppresses the

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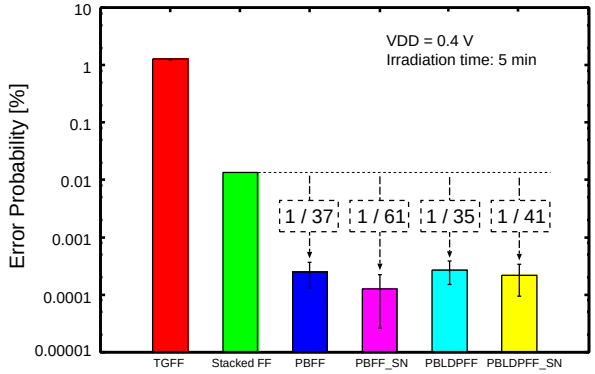
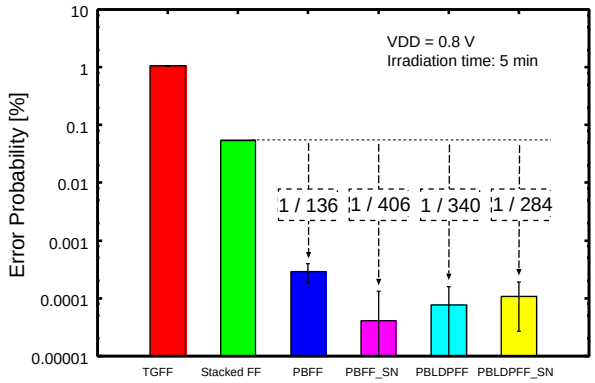
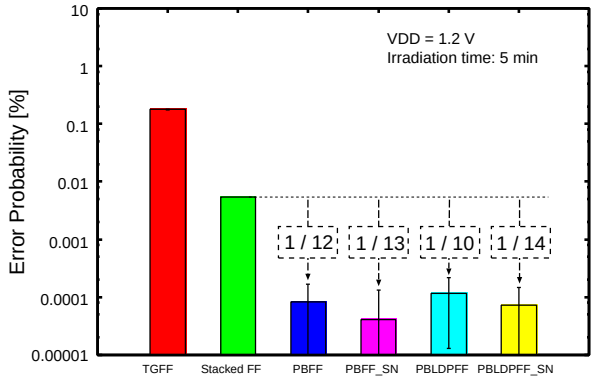


(a) V_{DD} = 0.4 V



(b) V_{DD} = 0.8 V



(c) V_{DD} = 1.2 V

Fig. 17. Average α particle-induced error probabilities under all four static conditions. The α particle-induced error probabilities of the stacked FF are from [17]. The worst values in error bars of the proposed FFs were compared with the true value of stacked FF.

PBE [18]. The experimental results of all proposed FFs when VBN = 0 V and VBN = -1 V are almost equivalent since all proposed FFs have sufficiently low SERs when VBN = 0. The reverse body bias suppresses static power consumption of PBLDPFF and PBLDPFF_SN while maintaining soft-error tolerance.

C. Spallation Neutron Irradiation

The spallation neutron experiments were carried out at the research center for nuclear physics (RCNP), Osaka University, Japan [19]. Figure 19 shows the neutron beam spectrum in comparison with the terrestrial neutron spectrum at sea level in New York. The average acceleration factor (AF) is about

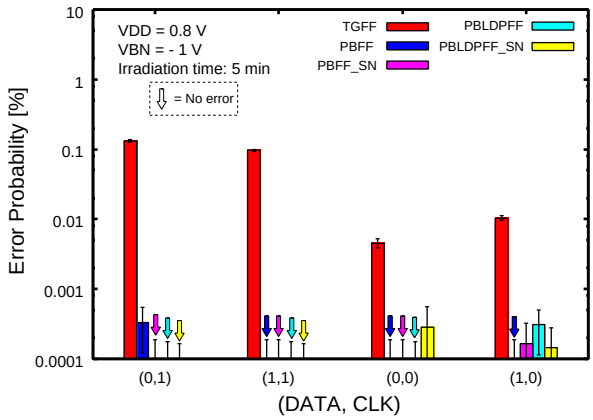


Fig. 18. Experimental results of α particle-induced error probabilities under each condition when VBN = -1 V. The error bars are within 68% confidence. Down arrows mean no error. The worst values in error bars of the proposed FFs were compared with the true value of stacked FF.

4.3×10^8 compared with sea level in New York. To increase the number of upset FFs within a limited time, stacked device under test (DUT) boards with four test chips were used. We measured soft error rates (SERs) under the four static conditions used in the five-minutes α particle irradiation tests. The SER was calculated using Eq. 2. Tests were performed a total of 20 times under each condition and data are the average of all tests. The error bars are within 68% confidence.

$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\mathrm{error}} \times 10^9 \times 1024^2}{5/60 \times \mathrm{AF} \times N_{\mathrm{FF}}} \qquad (2)$$

Table III summarizes the average number of errors by neutrons under each static condition when V_{DD} = 0.8 V. There are no errors in the proposed FFs except for PBLDPFF_SN. The sum N_{error} of PBLDPFF_SN in all experiments was 3 out of 69,600 FFs, while TGFF had 93 out of 83,520 FFs. When CLK = 0, the SERs of PBFF_SN and PBLDPFF_SN were very small. These results clearly show that we can eliminate SERs by suppressing soft errors originating only from NMOS transistors.

Figure 20 shows neutron-induced SERs when V_{DD} = 0.8 V. The experimental results of the stacked FF at V_{DD} = 0.8 V when (DATA, CLK) = (0, 0) and (1, 0) are from [17]. The SER of stacked FF is 1/4 smaller compared with TGFF at 0.8 V when (DATA, CLK) = (1, 1). The stacked-transistor structure is an effective method to decrease soft errors from stacked inverters. Similar to the results of the α particle test, no distinct difference was observed in the SERs of all proposed FFs under all static conditions.

Figure 21 shows the average neutron particle-induced SERs under all four static conditions. The SERs of the proposed FFs are 1/16 - 1/7 smaller than those of stacked FF.

V. Conclusion

We propose four FFs with PMOS pass-transistors in master latches and stacked inverters in slave latches. PBLDPFF and PBLDPFF_SN have similar structures except for the stacking structure in slave latches. PBLDPFF has inverters with stacked NMOS and PMOS transistors, while PBLDPFF_SN has inverters with stacked NMOS and unstacked PMOS transistors. SET

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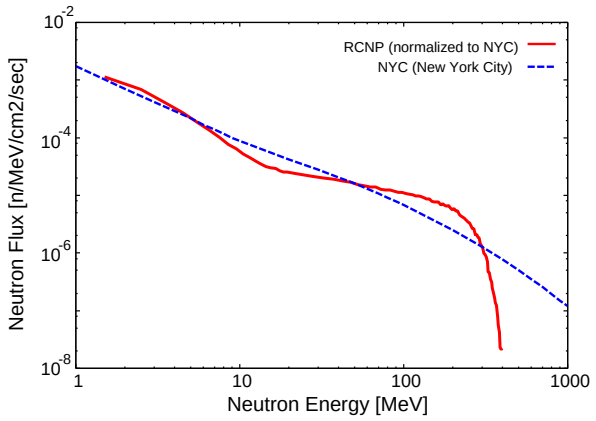

Fig. 19. Energy spectrum of spallation neutron beam at RCNP and NYC.

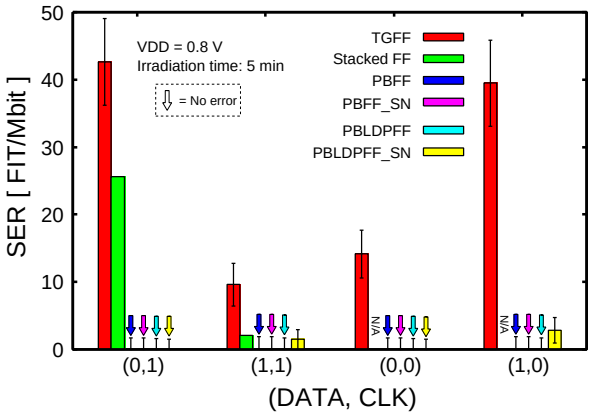

Fig. 20. Neutron irradiation results under each condition. The error bars are within 68% confidence. The neutron particle-induced soft error rates of the stacked FF are from [17]. Down arrows mean no error. N/A means no data.

TABLE III
THE NUMBER OF ERRORS BY NEUTRONS ON AVERAGE UNDER EACH STATIC CONDITION WHEN V_{DD} = 0.8 V IN 20 EXPERIMENTS.

	# of errors			
(DATA, CLK)	(0, 1)	(1, 1)	(0, 0)	(1, 0)
TGFF	1.95	0.40	0.65	1.65
PBFF	0.00	0.00	0.00	0.00
PBFF_SN	0.00	0.00	0.00	0.00
PBLDPFF	0.00	0.00	0.00	0.00
PBLDPFF_SN	0.00	0.05	0.00	0.10

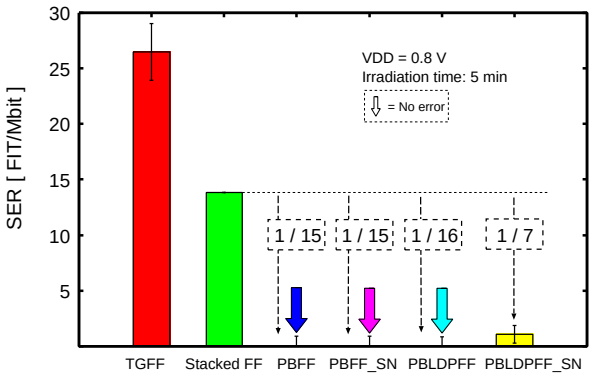

Fig. 21. Average neutron particle-induced soft error rates under all four static conditions. Down arrows mean no error. The neutron particle-induced soft error rates of the stacked FF are from [17]. The worst values in error bars of the proposed FFs are compared with the true value of stacked FF.

pulses are effectively suppressed even in PBLDPFF_SN since NMOS transistors are more sensitive to a particle penetration than PMOS transistors. PBFF and PBFF_SN are modified versions of PBLDPFF and PBLDPFF_SN, respectively, which have clock buffers to decrease the static power consumption and shorten the delay time with an area overhead.

PBFF and PBFF_SN have 30% shorter delay and 15% less dynamic and static power overheads than the conventional radiation-hardened stacked FF. PBLDPFF and PBLDPFF_SN have 20% shorter delay, 50% less dynamic power but 35x higher static power overheads than stacked FF. Static power can be suppressed using the reverse body bias or low-threshold transistors while maintaining soft-error resilience. We should use low-threshold transistors for PMOS pass-transistors or apply reverse body bias when we design or use the proposed FFs.

We investigated the radiation hardness of our FFs by α particle and neutron irradiation tests. The α particle results show that error probabilities of the proposed FFs are 1/400 - 1/130 smaller than that of stacked FF. The neutron irradiation results show that soft error rates of the proposed FFs are 1/16 - 1/7 smaller than stacked FF. These simulation and experiment results clearly show the proposed FFs have better radiation hardness and smaller overheads than stacked FF. It is possible to eliminate soft errors in terrestrial regions using PMOS pass-transistors and stacked inverters consisting of stacked NMOS and unstacked PMOS transistors.

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