Monolithically integrated GaN power ICs designed using the MVSG compact model for enhancement-mode p-GaN gate power HEMTs, logic transistors and resistors

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***Abstract*—This paper presents the models for several components needed for GaN IC design. MVSG model works very well in modelling the high-voltage p-GaN gate power HEMTs and low-voltage GaN logic transistors. The 2DEG resistor can be modelled either using MVSG model or empirical spice model. Low ohmic resistance can be easily modelled with empirical equation. Circuit simulations and measurements demonstrate the convergence and accuracy of the models.**

Keywords—p-GaN gate HEMT, MVSG model, GaN IC, Circuit simulation, Half-bridge.

I. INTRODUCTION

Enhancement mode p-GaN gate HEMTs are promising for power switching applications thanks to their high threshold voltage and good stability. To unlock the full potential of E-mode p-GaN gate HEMTs for power applications, monolithically integrated GaN ICs are essential to enable faster switching than power systems using discrete components, because of suppressed parasitic inductance and capacitance.

Designing circuits requires accurate and physics-based compact device models. The MIT virtual source GaN (MVSG) HEMT model has been accepted by the compact model coalition (CMC) as one of the industry standard models for GaN HEMTs [1]-[3]. The MVSG model will be validated for high voltage p-GaN gate power HEMTs with large gate width and gate-to-drain distance as well as the low-voltage logic transistors with narrow gate width and short gate-to-drain distance. Because the MVSG model is lack of physics of back-to-back diodes for gate structure, we adapted the MVSG model to simulate the gate current using Pool-Frenkel tunneling equations.

High resistive 2DEG resistors are used as resistive loads in circuit designs because the GaN HEMT technology does not support a complementary device. In this paper, we model the 2DEG resistor using the MVSG model. Alternatively, empirical models in spice for 2DEG resistors and low ohmic resistors work well too.

Final focus of this paper is the verification of the models in circuit level. We report two ICs on GaN-on-SOI (or poly-AlN) as examples. The benchmarking of the switching waveform of switching circuit and half bridge by simulations and measurements demonstrates the usefulness of the MVSG model in facilitating GaN power ICs design.

II. DEVICE MODEL

A. Core MVSG model

The core MVSG model equations calculate the terminal current and non-linear device charges as a function of bias and temperatures as given in [1]. The MVSG-HV model extends the quasi-ballistic transport for short channel device to the drift-diffusion transport for long channel devices by a suitably adapted formulation. Modelling attention went to five distinct regions of the device, which are the intrinsic transistor under the gate, two regions next to the gate on the drain side called the field plate regions, and two access regions, as shown in Fig. 1. More details on the equations, verilog-A code and manual are available online [2]-[3].

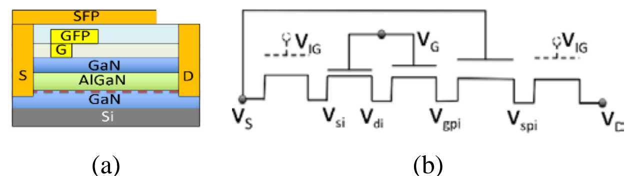


Fig. 1. (a) Cross-sectional schematic of GaN HEMTs on Si for high voltage applications. (b) The equivalent circuit for the MVSG model with intrinsic transistor, gate-field plate, source-field-plate and implicit-gate access region transistors [3].

B. p-GaN power HEMTs MVSG model verification

Modelling results are compared with measurements of currents and capacitances, for 200V p-GaN gate power HEMTs fabricated in imec's pilot line, as shown in Fig. 2. The simulated transfer characteristics and derived trans-conductance match well with the measurement results. The output characteristics sweeping V_{ds} from 0 to 10V, and varying V_{gs} from 0V to 7V at 25°C and up to 150°C are well modelled, capturing the temperature dependence of the carrier transport. Self-heating effect were simulated using a thermal impedance equivalent network. The off-state capacitances C_{gs}, C_{gd} and C_{ds} at V_{gs}=0 with V_{ds} from 0V to 200V, are nicely modelled, capturing the impact of the field plates that modulate the 2DEG distribution at high V_{ds}.

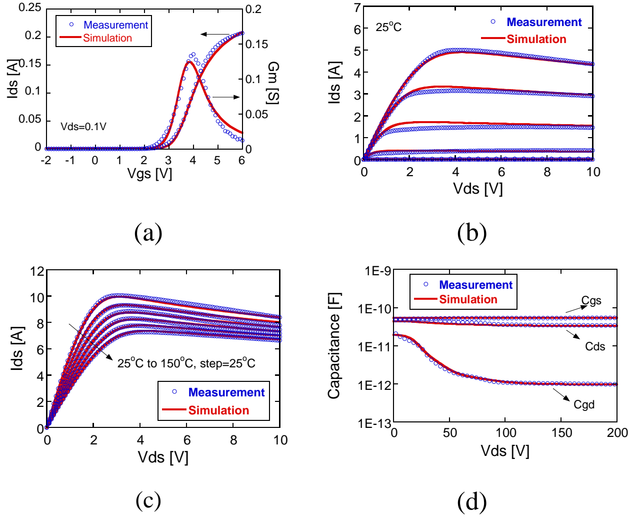


Fig. 2. MVSG model validation against the 200V power transistor of L_g=1.3µm, L_{gd}=6µm, and W_g=36mm. (a) Transfer IV curve and transconductance, at V_{ds}=0.1V, (b) output IV curve at 25°C, (c) output IV curves at V_{gs}=7V varying temperature from 25°C to 150°C by step of 25°C, (d) off-state capacitance of device at V_{gs}=0.

C. p-GaN gate leakage simulation

P-GaN gate HEMTs, fabricated at imec, feature a TiN gate metal on top of the p-GaN layer in order to form a Schottky contact on the p-GaN to 2DEG gate input diode, to reduce the leakage current. Therefore, the gate leakage follows a path along this "back-to-back diode" structure [4]. The MVSG model lacks the physics for modelling the Schottky-pGaN gate leakage. The model is adapted by taking into account the fact that the gate leakage is dominated by the Schottky metal/p-GaN at V_{gs}>0, and the gate leakage is perimeter dependent at V_{gs}<0. Both branches can be modelled using Pool-Frenkel tunneling equation (1). The benchmark of the model with the measurement data in Fig. 3 shows good overlay of the modelling and measurement results at different temperatures.

$$J_{PF} \propto E exp\left(-\frac{q\left(\varphi_B - \sqrt{\frac{qE}{\pi \epsilon}}\right)}{kT}\right) \qquad (1)$$

Where E is the applied electric field, φ_B is the voltage barrier, ϵ is the permittivity, T is the temperature, k is the Boltzmann's constant.

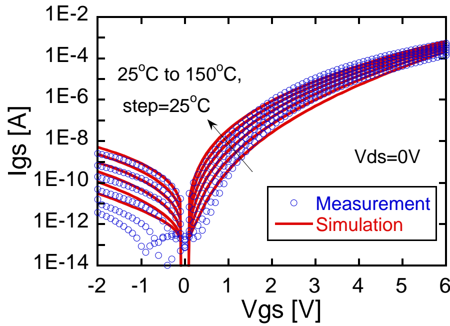


Fig. 3. Gate leakage modelling vs measurement at multiple temperatures. The transistor has L_g=1.3µm, L_{gd}=6µm, and W_g=36mm.

D. Logic device modelling

Low-voltage analog/logic transistors are needed for control logic and driving the power transistors. The key factor to achieve fast switching of the power HEMTs is to monolithically integrate the gate driver using the low-voltage driver transistors with the high-voltage power HEMTs. Therefore, it is also important that the MVSG model can model the low-voltage GaN analog/logic devices. The fabricated low-voltage devices modelled, feature W_g of 6 µm and L_{gd} of 1.5 µm. Fig. 4 confirms the functionality of the logic devices and accuracy of the MVSG model for the logic devices.

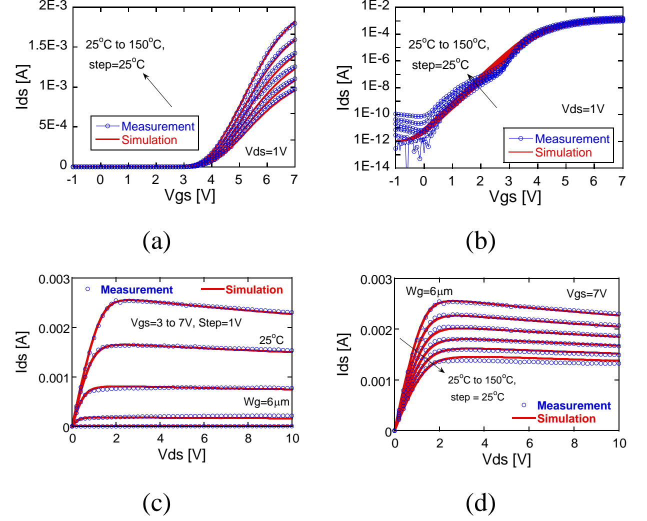
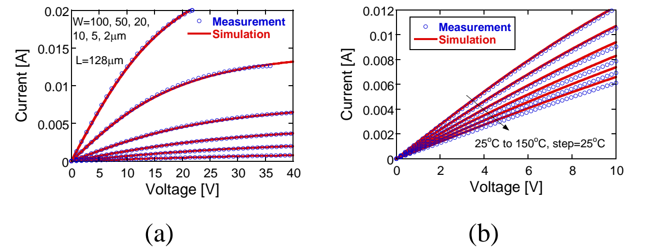


Fig. 4. MVSG model validation against the logic transistor of L_g=1.3µm, L_{gd}=1.5µm, and W_g=6µm (a) and (b) Transfer IV curve at V_{ds}=0.1V in linear and in logarithmic axis (c) output IV curve at 25°C (d) output IV curves at V_{gs}=7V varying temperature from 25°C to 150°C by step of 25°C.

E. MVSG model for 2DEG resistors

Modelling attention went to the access region because this region is either a part of the transistor or can be an independent component as a 2DEG resistor for the RTL logic circuits. The access region is modelled as a transistor with implicit-gate. This model is verified using 2DEG resistors with multiple dimensions and at multiple temperatures, shown in Fig. 5. The non-linear behavior of IV curves can be reproduced by simulation using the implicit-gate MVSG model, which is a result of the combined effect of velocity saturation and self-heating.



(a) (b)

Fig. 5. MVSG model verification using 2DEG resistors.

F. Alternative spice model for high ohmic resistor (2DEG resistor)

An alternative model for the 2DEG high ohmic resistor is the classic spice model using empirical equations for voltage non-linearity and temperature dependence. The 2DEG resistor is isolated from other devices by N implantation. Scattering of the N atoms below the active area mask edges

causes a reduction in effective width (δW), which can be determined by (2).

$$1/R = (W - \delta W)/(2 \cdot R_c + R_{sh} \cdot L) \quad (2)$$

where R is the total 2DEG resistance, R_{sh} is the 2DEG sheet resistance, R_c is the contact resistance, L and W are the length and the width of the 2DEG resistors. From the plotted 1/R vs W, the total width reduction of 2DEG resistor δW is 0.26µm, shown in Fig. 6(a).

Temperature dependence of the 2DEG resistance can be described by the follow equation (3):

$$\frac{R(T)}{R_0} = [1 + T_{c1}(T - T_0) + T_{c2}(T - T_0)^2] \quad (3)$$

where R_0 is the resistance at T_0=25°C, T_{c1} and T_{c2} are the first and second order temperature coefficients of the resistance. As seen in Fig. 6 (b), all the measured 2DEG resistors follow the quadratic function in (3). The temperature coefficients can be extracted as T_{c1}=6.38e-3K^{-1} and T_{c2}=1.61e-5K^{-2}.

Bias dependence of the resistance of the 2DEG resistors follows an empirical function as (4):

$$\frac{R(V)}{R_0} = [1 + V_{c1} \cdot V + V_{c2} \cdot V^2] \quad (4)$$

where R_0 is the resistance measured at low bias and V_{c1} and V_{c2} are empirical first and second order voltage coefficients. V_{c1} and V_{c2} are a function of the length of the resistors, which can be written as (5) and (6).

$$V_{c1} = J_{c1a}/L + J_{c1b} \quad (5)$$

$$V_{c2} = J_{c2a}/L^2 + J_{c2b}/L + J_{c2c} \quad (6)$$

where J_{c1a}, J_{c1b}, J_{c2a}, J_{c2b} and J_{c2c} are fitting parameters, L is the length of the 2DEG resistor. As a result, the first order voltage coefficient can be expressed as:

$$V_{c1} = \max(0.5316/L - 0.012, C) \quad (7)$$

where C is the clamping parameter and equals to 0.0016 V^{-1}. The fitting parameter can be extracted J_{c2a}=-0.365 m^2·V^{-2}, J_{c2b}=0.121 m·V^{-2} and J_{c2c}=7e-4 V^{-2}. The fitting results in Fig. 6 (c) and (d) show that the empirical model has a good agreement with the measured resistance.

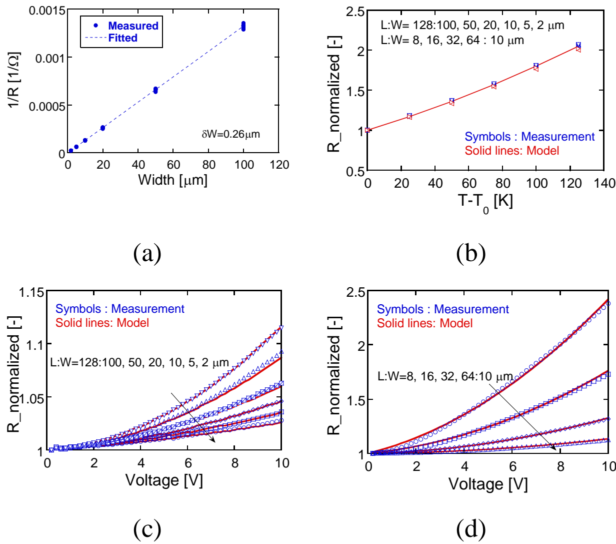


Fig. 6. Measurement vs modelling of 2DEG resistors (a) 1/R vs W to determine the encroachment δw (b) Temperature dependence (c) and (d) bias dependent.

G. Low ohmic resistor model

Some circuits require a resistor with very low value, e.g. for gate stabilization. The metal layer used to fabricate ohmic contacts has an attractive sheet resistance. For these low ohmic resistors, the same model equations (2) to (7) are used. The width encroachment δW is -0.41µm, which is a result of the sloped edge of the ohmic metal line. The coefficients modelling the temperature dependence of the resistance are T_{c1}=1.6e-3K^{-1} and T_{c2}=0. Bias dependence of the resistance can be described as

$$\frac{R(V)}{R_0} = \left[1 + \left(\frac{1.23}{L} - 0.00471\right)V + \left(\frac{24.7}{L^2} + \frac{8.46}{L} - 0.035\right)V^2\right].$$

Good agreement of the model with the measurement results is shown in Fig. 7.

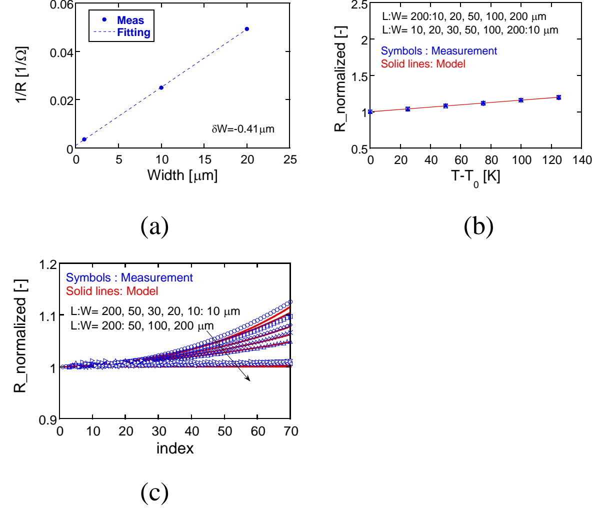


Fig. 7. Measurement vs modelling of low ohmic resistors (a) 1/R vs W to determine the encroachment δw (b) Temperature dependence (c) bias dependent.

III. Circuit Level Verifaction

Co-integration of power devices in a half-bridge configuration, requires a modification of the GaN-on-Si technology, as the Si substrate is a common back-gate for the low-side and high-side power devices [5]. GaN-on-SOI or GaN-on-polyAlN substrates have a thin silicon layer on top of a buried oxide on a carrier wafer. The buried oxide together with oxide filled deep trench isolation, as shown in the schematic cross-section of Fig. 8, allows to locally contact the thin Si layer for each power device, logic block or driver stage to fully suppress the back-gating effect, and to reduce the coupling of the switching noise of the power transistors into the sensitive logic and analog blocks.

With the models described above for the high-voltage power transistors, low voltage logic and analog transistors and drivers, high-ohmic and low-ohmic resistors, monolithic integrated power systems can be simulated.

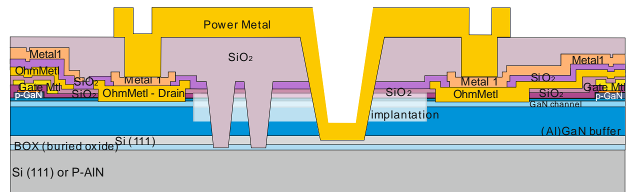
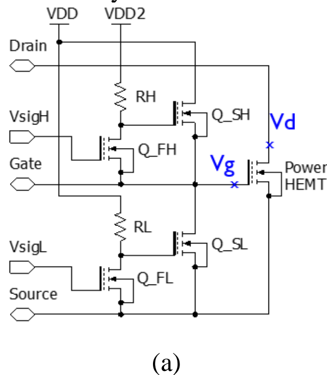


Fig. 8. Schematic cross-section of GaN-on-SOI (or poly-AlN) with deep trench isolation

In this section, we will verify our models on circuit level with 2 examples. Fig. 9 (a) shows as a first example the proposed GaN IC of [6], comprising of a power HEMT with two-stage integrated driver. Fig. 9 (c) shows the overlay of

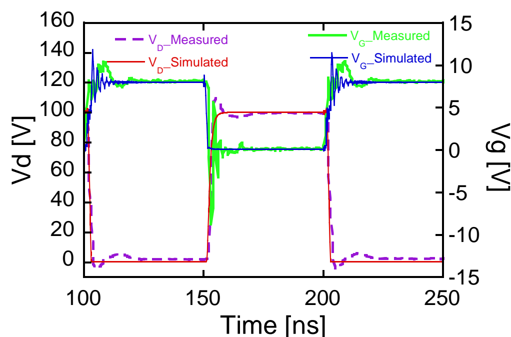
the switching waveforms of the simulations and the measurements, where the circuit operated at 10MHz switching frequency, 100V of off-state V_{DS} and 4A of on-state I_D. This circuit involves 5 transistors of different dimensions. Thanks to the scalability of the MVSG model, a nice benchmark between the simulation results and the measurement results is achieved, which demonstrates the convergence and accuracy of the models.



(a)

	W_g	L_{gd}	L_{gs}	L_{fp}	L_g
PowerHEMT	70	4	0.75	0.65	1.3
Q_SH	24	1.5	0.75	0.25	1.3
Q_SL	24	1.5	0.75	0.25	1.3
Q_FH	8	1.5	0.75	0.25	1.3
Q_FL	8	1.5	0.75	0.25	1.3

(b)



(c)

Fig. 9. (a) Monolithically integrated GaN switching circuit (b) Geometry parameters of the device in circuit (a). (c) Simulation results overlay with measurement results of circuit (a).

Fig. 10 shows as a second example the fabricated GaN drivers and half-bridges, switching at 1MHz and 200V. The switching speed is determined pre-dominantly by the Miller capacitance in the gate driver. Due to the accurate modelling of C_{gd} by the MVSG model, the switching waveform can be accurately reproduced in simulation, as shown in Fig. 11.

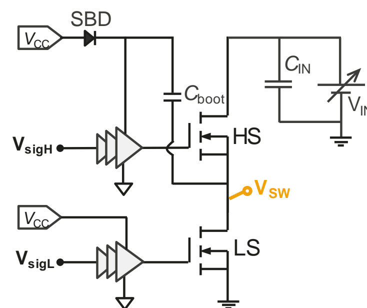


Fig. 10. Monolithically integrated GaN drivers and half-bridge.

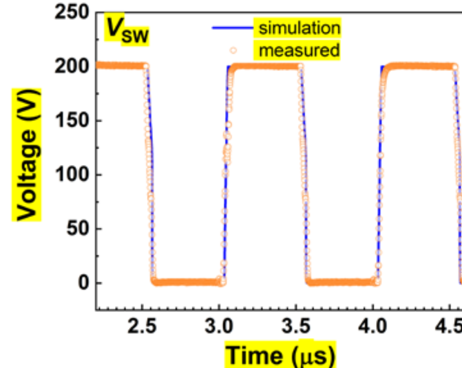


Fig. 11. Simulation results overlay with measurement results of circuit in Fig. 10.

IV. Conclusions

We have validated the MVSG model on device level by comparing the modelling results with the measurement results of the high-voltage p-GaN gate power HEMTs with large gate width and long gate-to-drain distance and the low-voltage GaN analog/logic low-voltage devices with narrow gate width and short gate-to-drain distance. The high-resistive load 2DEG resistor of the GaN IC platform is modelled either using the MVSG model or the empirical spice model. The Low-ohmic resistor can be easily modelled with the empirical SPICE resistor equation accounting for the temperature dependence and the bias dependence of the resistance. Accurate circuit simulations demonstrate the convergence and accuracy of the models.

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