# A Bit-Error Rate Measurement and Error Analysis of Wireline Data Transmission using Current Source Model for Single Event Effect under Irradiation Environment

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**Abstract**

A high-speed wireline interfaces, e.g. LVDS (Low Voltage Differential Signaling), are widely used in the aerospace field for powerful computing in artificial satellites and aircraft. This paper describes Bit Error Rate (BER) prediction methodology for wireline data transmission under irradiation environment at the design stage of data transmitter, which is useful in proactively determining if the design circuit meets the BER criteria of the target system. Using a custom-designed LVDS transmitter (TX) to enhance latch-up immunity, the relationship between transistor size and BER has been analyzed with focusing on Single Event Effect (SEE) as a cause of the bit error. The measurement was executed under $^{84}Kr^{17+}$ exposure of 322.0 MeV at various flux condition from $1\times10^3$ to $5\times10^5$ count/cm$^2$/sec using cyclotron facility. For the analysis of the bit error, circuit simulation by SPICE was utilized with expressing the irradiation environment by a current source model. The current source model represents a single event strike into the circuit at drain and substrate junctions in bulk MOSFETs. For the construction of the current source model, a charge collection was simulated at the single particle strike with the creation of 3D Technology CAD (TCAD) models for the MOS devices of bulk transistor process technology. The simulation result of the charge correction was converted to a simple time-domain equation, and the single-event current source model was produced using the equation. The single-event current source was applied to SPICE simulation at bias current related circuits in the LVDS transmitter, then simulation results are carefully verified whether the output data is disturbed enough to cause bit errors on wireline data transmission. By the simulation, sensitive MOSFETs have been specified and a sum of the gate area for these MOSFETs has 29% better correlation than the normal evaluation index (sum of the drain area) by comparison to the actual BER measurement. Through the precise revelation of the sensitive area by SPICE simulation using the current model, it became possible to estimate BER under irradiation environment at the pre-fabrication design stage.

## 1. Introduction

Recent space electronics require higher computing power to complete more difficult missions because of the necessity for extra-terrestrial development, and utilization of advanced semiconductor devices is accelerating for space applications [3-7]. These devices for space applications have to prepare radiation hardness to be operable under the space radiation environment [8-11]. In this paper, we focus on CMOS latch-up and single event effects (SEE) at a heavy-ion radiation environment. Under heavy ion radiation, one or more types of energetic particles may cause latch-up and/or a single event (SE) on MOSFETs in CMOS structure. Latch-up directly leads to circuit malfunction. SE is similar to a soft error caused by alpha particles from the radioactive decay of package materials [12-16], but ions at the

space environment are usually much heavier than alpha particles and cause malfunction even on analog parts such as DC bias circuit by SEE [17-22]. When an energetic nuclear particle penetrates silicon substrate, it loses energy through Rutherford scattering with the semiconductor lattice structure, and the energy to the lattice generates free electron-hole pairs in silicon substrate [23, 24]. The free electron-hole pairs are drifted to high and low voltage potential respectively and accordingly generate a transient current on nodes of MOSFETs [23, 24] as shown in Fig.1.

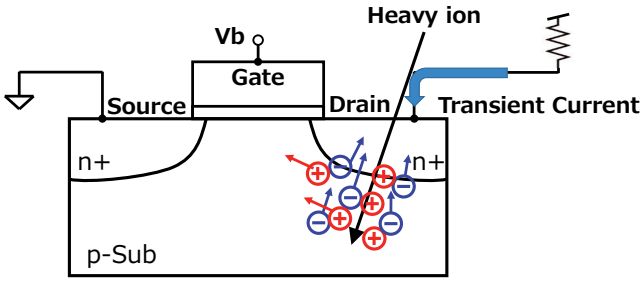



Figure 1: Carrier generation mechanism by heavy ion exposure

The transient current may cause latch-up and/or lead to voltage transient on bias voltage nodes of analog circuits in a semiconductor device. When latch-up occurs, internal circuits do not operate properly because a large direct current continuously flows between the power node (VDD) and the ground (VSS). On the other hand, the voltage transient on bias voltage nodes causes a period when the internal circuits do not work properly, so the data generated during the period by the circuits are likely to be abnormal and cause an error.

This paper describes Bit Error Rate (BER) prediction methodology for wireline data transmission of LVDS (Low Voltage Differential Signaling) topology [25-27] under irradiation environment. The LVDS is widely used for space application [28,29]. The BER was measured between the LVDS transmitter (TX) and receiver (RX) under a latch-up eliminated environment using a custom-designed LVDS transmitter (TX) for latch-up immunity enhancement [2]. In [2], nothing is stated about the BER estimation. In addition, the transient current is generated only by a mathematical formula, and there was a problem with accuracy.

In this paper, a relationship between transistor size and BER has been analyzed by focusing on Single Event Effect (SEE) as a cause of the bit error. The BER prediction methodology is based on error analysis by circuit simulation using the current source model for SPICE to emulate the transient current. The current source model is extracted through TCAD simulation to improve accuracy. Therefore, the methodology can be applicable at a circuit design stage and useful in proactively determining if the design circuit meets the BER criteria of the target system.

## 2. Transmitter Design and BER Measurement

### 2.1. *Circuit Design for Latch-up Immunity Enhancement*

BER should be measured under the latch-up eliminated condition in an irradiation environment. The radiation emission induces the transient current as shown in Fig.1 and it causes voltage drop through n-well and/or substrate resistance ($R_{nw}$, $R_{sub}$) in Fig.2. Due to the voltage drop, $V_{BE}$ of the parasitic BJTs ($Q_{PNP}$, $Q_{NPN}$) is positively biased and collector currents ($I_{C\_PNP}$, $I_{C\_NPN}$) flow between VDD and VSS. These corrector currents continue to flow as direct current until the power is turned off. Because thyristor structure of two BJTs ($Q_{PNP}$, $Q_{NPN}$) holds in a stable latching state, if the product of beta gains of these two BJTs can be kept greater than one. This state is called "latch-up".

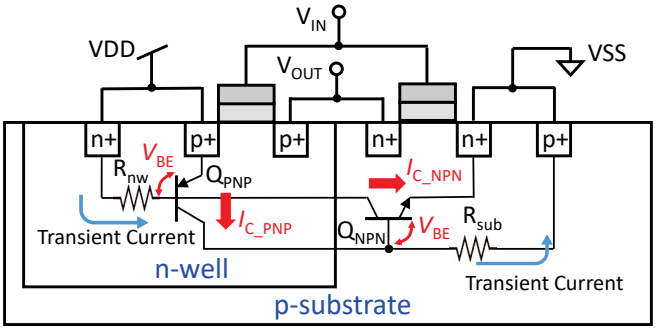



Figure 2: Cross Section of CMOS Inverter

Once the latch-up occurs, the internal circuits do not work properly due to the large and steady direct current between VDD and VSS. In the LVDS-TX where the latch-up has occurred, most of the transmitted data will result in an error, making detailed error analysis impossible. Therefore, an enhancement of latch-up immunity should be applied to the LVDS-TX for BER measurement with irradiation conditions. In this paper, it is assumed that radiation is applied only to TX as described later.

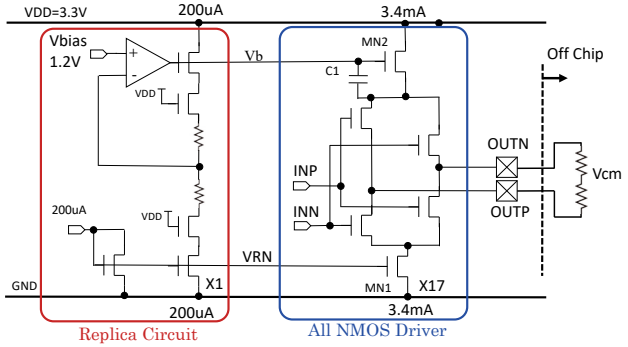
For radiation-hardened IC products with latch-up immunity enhancement, customized processes such as SOI, BiCMOS and deep trench isolation are generally used [17, 30, 31, 32]. In order to enhance

the latch-up immunity by design in the standard CMOS process, for example, redundant latches and power regulators are used [33, 34], but these are for digital circuits and are difficult to apply to analog circuits. For analog circuits, the most common way is to strengthen a guard ring on n-well and p-substrate for decreasing bulk resistances ($R_{nw}$, $R_{sub}$ in Fig.2) [35]. Normally, individual measures are taken for each analog circuit in consideration of individual circuit configurations [18-21], e.g. redundant circuit configuration [36]. In the custom-designed LVDS-TX, the following design measures of i) to iii) have been applied considering the circuit configuration as shown in Fig.3(a) and (b), which were described in [2].

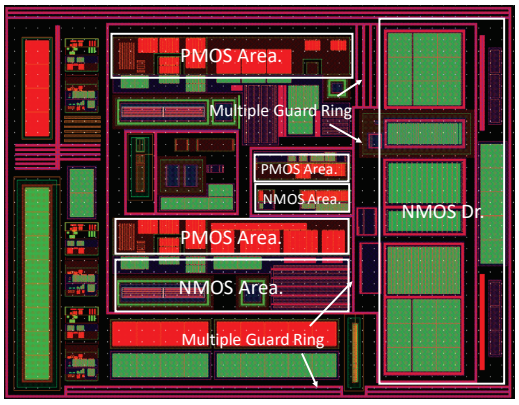
i) Off-chip Driver has large MOSFETs to feed transmitted data and large MOSFETs' region has the high beta gain of parasitic BJT. Therefore, the Driver was designed by NMOS only to avoid CMOS and thyristor structure.

ii) Feed-forward common voltage (Vcm) generation by replica circuit to avoid feedback loop via off-chip node (OUTP/OUTN)

iii) Multiple guard rings which applied on the bulk (p-substrate) between large n+ diffusion and n-well area, especially in the circuit area near the driver, to reduce n-well and substrate resistance ($R_{nw}$ and $R_{sub}$ in Fig.2)




(a) Circuit Schematic of Off-Chip Driver




(b) Layout of LVDS-TX

Figure 3: LVDS-TX Test Device

The TX test device was fabricated by Renesas SOTB 65nm Technology, which is a mixed process of SOI (Silicon On Insulator) and Bulk CMOS transistors. In the TX test device, only Bulk MOSFETs (3.3V applicable between source and drain nodes and 0.35µm technology equivalent) were used for the generated carrier in bulk to inject onto the drain node. Any SOI MOSFET was not used because the SOI structure is inherently resistant to latch-up and radiation.

### 2.2. *BER Measurement under Irradiated Environment*

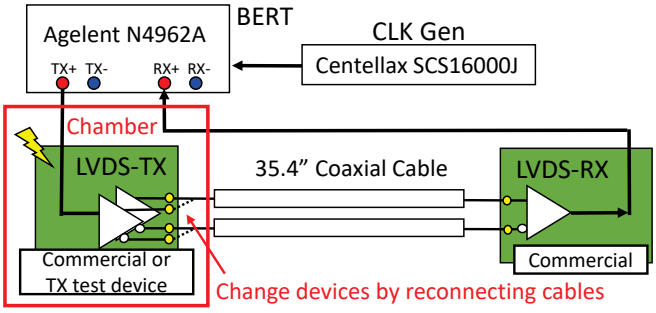
An experiment of data transmission between the LVDS-TX and RX was conducted in Cyclotron Radioisotope Center (CYRIC) at Tohoku University, Japan. As shown in Fig.4(a), a couple of evaluation boards were assigned to the transmitter (TX) and the receiver (RX) respectively, and only one board of the TX side was enclosed in a chamber for heavy-ion exposure. Fig.4(b) and (c) show the evaluation board and the chamber in the experiment. In the chamber, heavy-ion of $^{84}Kr^{17+}$ (LET: 40 MeV/cm$^2$/mg) of 322.0 MeV was irradiated at various flux condition from $1\times10^3$ to $5\times10^5$ count/cm$^2$/sec. As for the LVDS-TX device, the commercial device (DS90LV017A) and the TX test device were prepared as stated above, and the top surface of their package was exposed so that the heavy-ion could directly hit internal chips. As for the LVDS-RX device, a commercial device of DS90LV018A was used as shown in Fig.4(b).

Digital data was fed from Bit Error Rate Tester (BERT) of Agilent N4962A to either commercial or test device of LVDS-TX on an evaluation board in the chamber, and the digital data were converted to low voltage differential signal in the LVDS TX (Commercial or TX Test Device). As for the TX test device, design measures for the latch-up immunity enhancement have been applied to build the latch-up eliminated environment during BER measurement with irradiation conditions. The differential signal was sent out of the chamber through coaxial cables and transmitted to the commercial LVDS-RX on another evaluation board. The differential data was restored to full-swing digital data in the LVDS-RX, and the restored digital data was returned to the BERT for BER measurement.

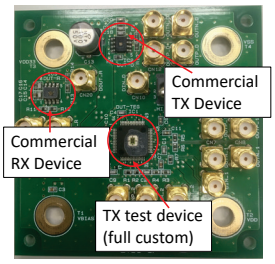
In the measurement, the heavy-ion was irradiated to the TX, not to the RX, because i) the custom-designed and latch-up eliminated device was only for the TX as stated, and ii) the RX device was a commercial

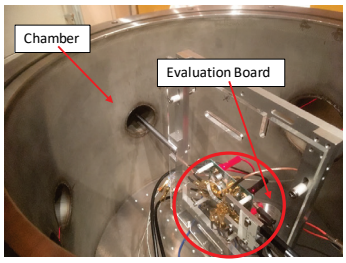
product and error analysis would be difficult due to non-disclosure of the internal circuits.

As for the LVDS-TX, one of the commercial and the TX test device could be connected to the LVDS-RX through coaxial cables by changing the cable connection as shown in Fig.4(a). Because BERT could not handle two series of data at the same time.




(a) Device Connection for Measurement




(b) Evaluation Board (c) Chamber

Figure 4: BER Measurement System

Fig.5 depicts the BER measurement results of the TX test device and the TX commercial device. The measurement was executed by the measurement system in Fig.4.

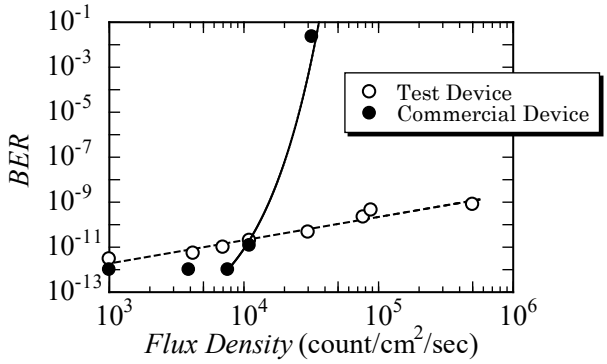



Figure 5: BER Measurement Results of the Commercial and Test Devises

As shown in the figure, bit error increases rapidly when the flux density is $10^4$ count/cm$^2$/sec or higher. The cause of this rapid increase for the bit error is seemed to be the latch-up in the commercial device. Because the operating current of the commercial device increased drastically after a drastic deterioration of BER, and the operation current did not decrease even if the operation was stopped. Also, when the power was turned on again after the power was turned off, it operated normally with reasonable operating current under non-irradiation conditions.

In contrast, the test device does not have a drastic increase in BER. It means the test device has a much higher latch-up tolerance thanks to above-mentioned design treatments.

However, in the test device experiment, BER worsened as the flux density increases according to Fig.5. Generally, in wireline communication, BER on the order of $10^{-12}$ bit/sec is required [37,38], therefore BER deterioration should be suppressed even in the irradiation condition. The cause of the BER deterioration seems to be a defect that occurs in the internal circuit of the test device due to the Single Event Effect (SEE). The reason is as follows. In the irradiation experiment, the BER was on the order of $10^{-9}$ even in the irradiation condition, and the operation was almost normal. When the irradiation was stopped, the bit error disappeared. That is, radiation caused a sporadic error in the circuits on the silicon chip, which was not permanent. From these facts, it was presumed that SEE was the cause of the bit error in the TX test device.

## 3. Bit Error Analysis by SPICE Simulation

### *3.1. Single-Event Current Source Model Setup*

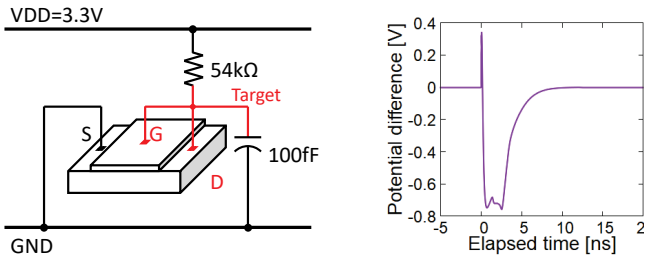
In order to analyze the bit error in the circuit simulation, it is necessary to reproduce the SEE under the irradiation situation of heavy ions on the SPICE simulation. For the reproduction of SEE, the single-event current source model should be built to express the transient current which is caused by radiation emission as shown in Fig.1.

To understand the carrier generation by radiation emission, a MOSFET model was constructed in TCAD of Synopsys Device Simulator. The MOSFET model was for an NMOS transistor of 5 μm width (W) and 4 μm length (L), and was operable at 3.3V VDD. In the TCAD simulation, the source node of the NMOS was tied to GND, then gate and drain nodes were connected and pulled up to VDD through a 54 kΩ resistor as shown in Fig.6(a).

The connected node of the gate and drain was the target node for the simulation. The target node had 100 fF capacitance considering gate capacitance of MOSFET in an analog bias circuit.

In the device simulation at a single stroke of a heavy-ion, its emission energy, depth and radios were set to 40.3 MeV/cm$^2$/mg, 2 μm and 0.0455 μm respectively assuming Krypton (Kr) ion emission.

Fig.6(b) is the results of the TCAD simulation for voltage transient at the target node with Kr ion emission onto the drain area.

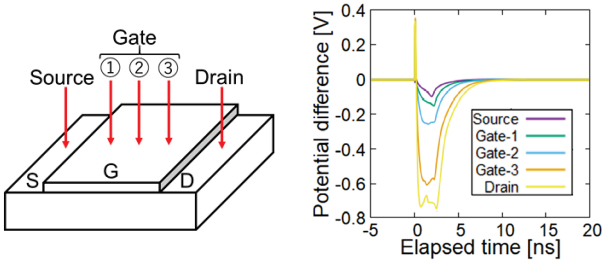



(a) Simulation model (b) Sim. Result

Figure 6: Device model and simulation result of TCAD environment

In the DC equilibrium state, the voltage of the target node is standardized to 0V. The voltage drop is caused by the transient current flowing through the 54 kΩ resistor after the emission. The transient current is caused by heavy ion emission as stated above.

Fig.7 shows the relationship between the irradiation position and the transient current for the model of Fig.6(a). A shown in the figure, the transient current is generated even if the irradiation position is the gate node instead of the drain node. Furthermore, the amount of transient current decreases as the irradiation position is closer to the source node.




(a) Irradiation Positions (b) Sim. Results

Figure 7: TCAD Simulation at various irradiation positions for the model of Fig.6(a)

### 3.2. *Configuration of Single-Event Current Source Model*

For verification of the analog circuit behavior, designers have to execute SPICE simulation for the circuit. In order to apply SPICE simulation assuming the irradiation condition, the transient current has to be expressed as a general current model on SPICE environment. For the current expression, the following equation (eq.1) was used to state the current on time domain [16]. Using the equation, curve fitting of time and current was tried by changing the time constant ($T$) and charge quantity ($Q$)

$$I(t) = \frac{2Q}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right) \qquad \text{(eq.1)}$$

The transient current was obtained through the calculation of eq.1 with setting $T$ and $Q$, and the current value was stored in a text file with specifying time value. Then, the time and current value were set to the general current source model of SPICE via the text file. Using the current source model, SPICE simulation model was executed with a circuit of Fig.8.

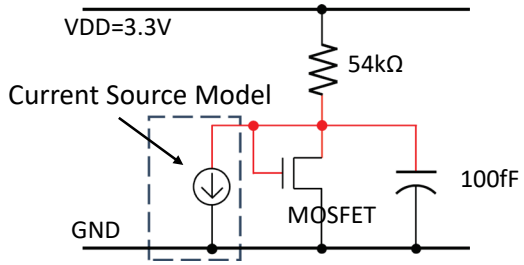



Figure 8: Circuit for SPICE simulation with the Current Source Model

For the curve fitting of the results between the circuit simulation of SPICEs using the current source model and the device simulation of TCAD, the transient current was adopted when the irradiation point was the drain node in this paper. By trial and error approach, $T$ and $Q$ were set to 200 ps and 144 fF respectively. The fitting result is shown in Fig.9. Time constant $T$ was seemed to be around 100 ps according to 0.35 μm technology of Fig.9 in [39], but the fitting result was better when $T$ was 200ps. The time constant $T$ is an effective vector and it can be extracted by fitting to measurement and/or simulation result [40]. Therefore, we decided to give priority to the simulation result.

For the fitting, starting time and voltage for the emission were set to 20ns and zero volt (0 V) respectively as shown in Fig.9.

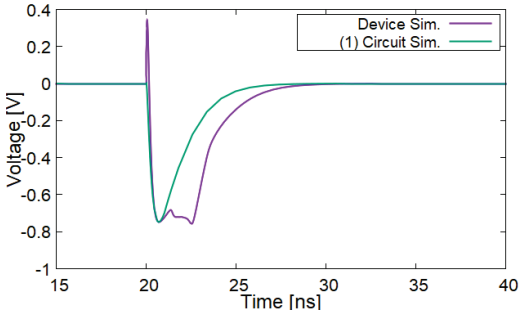



Figure 9: Comparison of device and circuit simulation results of eq.1

The figure denotes that the situation of stagnation at

peak value can not be expressed in the calculation model of eq.1. To express the stagnation, the equation has to be modified as follows according to the time range.

$$I(t) = \frac{2Q}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right) \quad \text{(eq.2a)}$$

($t$=$t_{star}$ to $t_{start}$+0.68ns)

$$I(t) = I_{peak} \quad \text{(eq.2b)}$$

($t$= $t_{start}$+0.68ns to $t_{start}$+2.48ns)

$$I(t) = \frac{2Q}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right) \quad \text{(eq.2c)}$$

($t$>$t_{start}$+2.48ns)

Calculation results of eq.2 (eq.2a, eq.2b and eq.2c) are shown as a series of graphs in Fig.10. In this calculation, $t_{start}$, $T$ and $Q$ were set to 20 ns, 200 ps and 144 fC respectively, which were the same as in Fig.9.

As seen from the comparison between Fig.9 and 10, the fitting of device and circuit simulation results has been significantly improved. Therefore, this single-event current source model can be applicable to SPICE simulation to simulate circuit behavior in an irradiation environment. This single-event current source expresses transient current at the drain node in the MOSFETs.

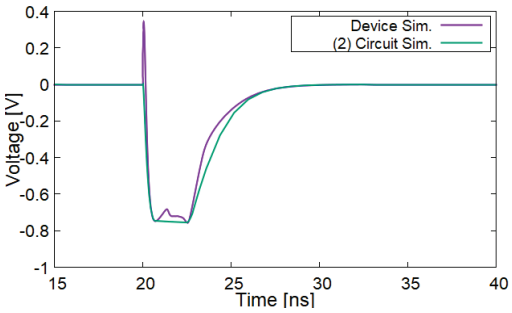



Figure 10: Comparison of device and circuit sim. of eq.2

### 3.3. *SPICE Simulation of the LVDS Transmitter*

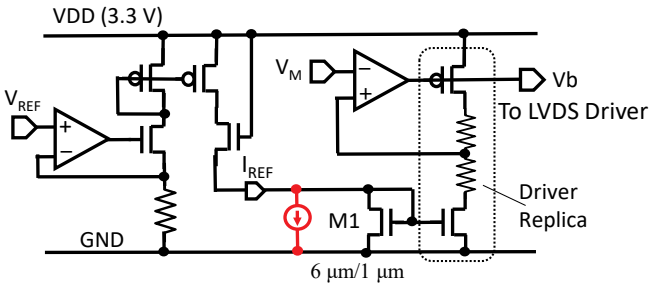
Applying the single-event current source model of Fig.10, a SPICE simulation using the current source model was performed in the LVDS-TX and RX. The current source model was connected to DC bias nodes of bias generator only in the LVDS-TX, then differential outputs of the LVDS-TX and the single output of the LVDS-RX are observed during the SPICE simulation. The RX circuit assumes a differential amplifier that converts incoming data from the differential to single. The current source connection was applied to the drain node of target MOSFETs.

Fig.11(a) illustrates a bias circuit in the LVDS-TX. The bias circuit is to generate a bias voltage (Vb) for LVDS driver to have pre-determined common-mode voltage (Vcm). The single-event current source was connected to drain node of M1 (L=1 µm, W=6 µm) as the target MOSFET

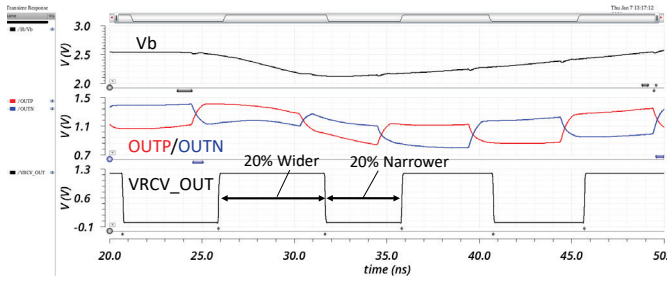
Fig.11(b) shows SPICE simulation results of the LVDS-TX and RX. The internal bias voltage (Vb) of Fig.11(a), differential outputs (OUTP/OUTN) of the TX and receiver output (VRCV_OUT) of the RX are depicted in the figure. The transient current flows at 20 ns from the current source in the simulation.

As shown in the figure, a bit width of received data (VRCV_OUT) has ±20% fluctuation due to bias voltage (Vb) distortion by current injection from the single-event current source model to drain node of specific MOSFETs, and the bit width fluctuation causes bit errors at BERT.

The bias circuit of Fig.11(a) is an example, and the LVDS-TX has a certain number of similar bias circuits. These bias circuits have a direct bias current on the order of microampere (µA), and the direct current is disturbed by the transient current of radiation emission. The current disturbance causes a problem with data transmission of the LVDS-TX in some cases.




(a) Bias Circuit of the LVDS TX




(b) Simulation Results

Figure 11: Circuit and SPICE Simulation Result with the Current Source Model

Table 1 lists channel width (W), length (L), parallel number (M), total drain area and total gate area for critical MOSFETs in the LVDS-TX, which have high sensitivity for radiation emission, e.g. M1 in Fig.11(a), enough to disturb the differential outputs of the LVDS-TX.

These critical MOSFETs have been found through one-by-one SPICE simulation with the current source for an entire circuit of the LVDS-TX.

Table 1: Critical MOSFETs and their parameters

| | *L* (μm) | *W* (μm) | M | Drain Area (μm²) | Gate Area (μm²) |
|---|---|---|---|---|---|
| M1 | 1 | 6 | 1 | 1.2 | 6 |
| M2 | 1 | 6 | 1 | 1.2 | 6 |
| M3 | 0.4 | 2 | 1 | 0.4 | 0.8 |
| M4 | 1 | 12 | 2 | 4.8 | 24 |
| M5 | 2 | 20 | 1 | 4 | 40 |
| M6 | 0.4 | 2 | 1 | 0.4 | 0.8 |
| *Sum* | | | | 12 | 77.6 |

## 4. Discussion

In this section, results of SPICE simulation and actual measurement are compared and discussed in view of BER as failure rate. By utilizing information of area (*S* as Sum) for critical MOSFETs in Table 1 and flux density (*F*) at measurement in Fig.5, BER can be calculated in given data rate (*DR*) in SPICE simulation via the following equation (eq.3) as shown in Fig.12. In eq.3, the calculated BER is expressed as *C_BER*.

$$C\_BER = \frac{S \times F}{DR} \qquad \text{(eq.3)}$$

This calculation is based on a probability that heavy ion particles will hit the critical MOSFETs.

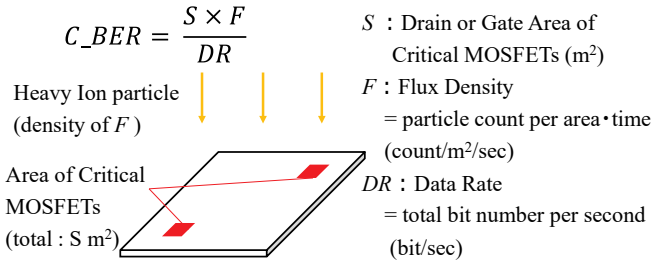



Figure 12: BER Calculation Methodology by flux density and the drain/gate area

In such failure rate calculation, drain area is usually used in error-induced MOSFETs because charge collection is related to the drain area [39-41]. In this paper, BER is calculated by eq.3 using the drain and gate area respectively considering TCAD simulation result of Fig.7. The calculation results are shown with measured BER in Fig.13.

According to this figure, BER calculation using the drain area is seemed to be underestimated when compared with the measured value. This cause is that the transient current has been induced at the drain node even if heavy-ion hits on the gate area as shown in Fig.7.

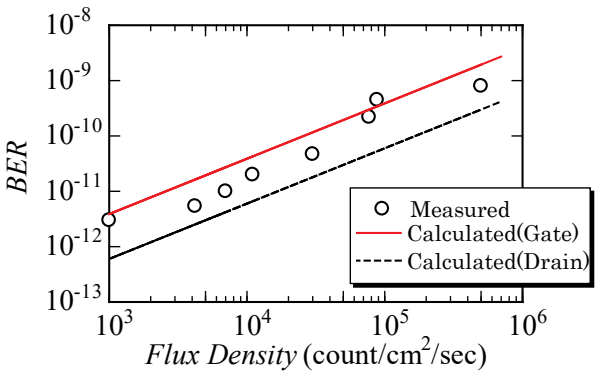



Figure 13: BER Calculation and Measurement in various Flux Density

Next, we verify which model parameter (drain or gate area) can better represent the actual failure rate of BER.

Table 2 shows measured BER (*M_BER*) and calculated BER (*C_BER*) of the drain and gate area basis on applied flux density (*F*) at the measurement.

Using these values and statistical methods [42], we quantify how well the calculation model for each parameter of the drain and gate area can reproduce the failure rate.

Table 2: BER at Applied Flux Density

| *i* | Flux Density (*F*) (count/cm2/s) | *M_BER* by Meas. (bit/s) | *C_BER* by Drain (bit/s) | *C_BER* by Gate (bit/s) |
|---|---|---|---|---|
| 1 | $1.0\times10^{3}$ | $3.0\times10^{-12}$ | $6.0\times10^{-13}$ | $3.9\times10^{-12}$ |
| 2 | $4.2\times10^{3}$ | $5.4\times10^{-12}$ | $2.5\times10^{-12}$ | $1.6\times10^{-11}$ |
| 3 | $7.0\times10^{3}$ | $1.0\times10^{-11}$ | $4.2\times10^{-12}$ | $2.7\times10^{-11}$ |
| 4 | $1.1\times10^{4}$ | $2.0\times10^{-11}$ | $6.6\times10^{-12}$ | $4.3\times10^{-11}$ |
| 5 | $3.0\times10^{4}$ | $4.7\times10^{-11}$ | $1.8\times10^{-11}$ | $1.2\times10^{-10}$ |
| 6 | $7.7\times10^{4}$ | $2.2\times10^{-10}$ | $4.6\times10^{-11}$ | $3.0\times10^{-10}$ |
| 7 | $8.8\times10^{4}$ | $4.5\times10^{-10}$ | $5.3\times10^{-11}$ | $3.4\times10^{-10}$ |
| 8 | $5.0\times10^{5}$ | $8.0\times10^{-10}$ | $3.0\times10^{-10}$ | $1.9\times10^{-9}$ |

For the analysis, we define the following parameters.

$$x_i = \log F_i \qquad \text{(eq.4)}$$

,where *Fi* is Flux Density of *i*

$$y_i = \log M\_BER_i \qquad \text{(eq.5)}$$

,where *M_BERi* is BER for measured results of *Fi*

$$\hat{y}_i = \log C\_BER_i \qquad \text{(eq.6)}$$

,where *C_BERi* is BER for calculation results of *Fi*

By mapping $(x_i, y_i)$ and $(x_i, \hat{y}_i)$ to x-y plane, a graph similar to Fig.13 will be produced. Therefore, statistical analysis of a double logarithmic graph can be applicable. Considering the coefficient of determination ($R^2$) in statistics, we define $Q^2$ as follows;

$$Q^2 = \frac{\sum_i^n (\hat{y}_i - \bar{y})^2}{\sum_i^n (y_i - \bar{y})^2} \quad \text{(eq.7)}$$

$$\bar{y} = \frac{\sum_{i=1}^n \hat{y}_i}{i} \quad \text{(eq.8)}$$

, which is average of $\hat{y}_i$

$\hat{y}_i$, $\bar{y}$ and $Q^2$ are derived for each drain and gate areas basis.

This $Q^2$ provides a measure of how well the actual failure rate (*M_BER*) is replicated by the calculation model, based on the percentage of the total variation of *M_BER* explained by the calculation model with referencing the point set ($\bar{y}$) in each calculation model.

Therefore, the closer the $Q^2$ is to 1, the better the calculation model represents the variation of measurement values (*M_BER*).

The $Q^2$ is similar to $R^2$ in statistics, but not exactly. This is because the calculation model does not come from a regression analysis from the measurement data, but from the hit rate of heavy-ion as explained in eq.3.

Through Table 2 and eq.4 to eq.8 at n=9, $Q^2$ of the drain and gate area are calculated as follows;

$$Q^2_{Drain}=0.63$$
$$Q^2_{Gate}=0.81$$

From these results, the calculation model of the gate area explains the failure rate about 29% better than one of the drain area.

## 5. Conclusion

The test result of BER measurement for the LVDS data transmission under the Krypton (Kr) irradiation condition shows that the error rate worsens as the flux density increases under the latch-up eliminated condition. The error rate increases in proportion to the flux density. This is caused by the Single Event Effect (SEE) of radiation emission and can be reproduced in SPICE simulation using the current source model, which represents SEE in time-domain analysis. The analysis can specify critical MOSFETs which have high sensitivity for radiation emission enough to cause the bit error.

This paper clarifies that the gate area of the critical MOSFETs is a more effective parameter for estimating the BER. By comparison with the actual measurement of BER and the original evaluation index ($Q^2$), the failure rate can be explained 29% better by using the gate area than the drain area. This estimation methodology is useful to judge design quality at the circuit design stage in case that any error rate criteria under the radiation environment are given to circuit designers.

## Data Availability

Data of the BER measurement are available within this article.

Simulation data that support the findings of this study are available, but restrictions apply to the availability of these data, which were used under license for this study. The data are available with the permission of Renesas Electronics Corporation from the corresponding author, Takefumi Yoshikawa, upon reasonable request.

## Conflicts of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.

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