Study of Design Methodology of ASIC and FPGA Considering Correlation between Process Variation and BTI-Induced Degradation

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Chapter 1

Introduction

1.1 Outline

We widely use LSIs (Large Scale Integrations) for many industrial products such as computers, mobile devices, automobiles, and medical instruments. LSIs are infrastructures for our current advanced information society. Hundreds of millions of transistors are integrated within a single chip through advances in the scaling. The progress of the scaling improves the economic development. LSIs play important roles in our society. LSIs must be reliable products[1, 2, 3, 4].

Reliability issues of MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), such as BTI (Bias Temperature Instability) and process variations become dominant at the highly-scaled process[5]. BTI is one of the most significant aging-degradations on LSIs. Threshold voltages V_{th} of transistors are shifted by BTI for the long-term period of use. They result in circuit delays and unstable performances because their effects are not negligible and avoidable.

In this study, the design methodology considering the correlation between process variations and BTI-induced degradations is proposed. The design margins of LSIs are reduced without threatening their reliability. The frequencies of ROs (ring oscillators) on ASICs and FPGAs are measured to analyze the reliability issues. The frequencies are varied by the process variations according to locations on the test chips. They follow the Gaussian distribution. The groups of the highest, average and lowest frequencies are focused on. The aging-degradations of the three groups are measured on the accelerated test. The correlation between process variations and BTI-induced degradations

are examined. The degradation at the highest frequency group is larger than one at the slowest frequency group. BTI has a large impact on the highest frequency group transistors. The appropriate design margins are defined according to this nature.

This chapter is organized as follows. Section 1.2 and section 1.3 show introductions of the BTI and the process variation, respectively. Section 1.4 shows the introduction of the correlation of the degradations. Section 1.5 shows related works of this study. Section 1.6 shows the purpose of this study. Section 1.7 shows the brief summary of this study.

1.2 BTI (Bias Temperature Instability)

This section introduces the effect, history, physical origin, and the impact on circuits of BTI.

There are two types of BTI. One is called NBTI (Negative BTI) that appears in PMOS transistors[6]. Because V_{th} of PMOS transistors increases with time when their gates are stressed by negative bias. NBTI is known as one of the dominant factors that determines life time of circuits after 65-nm process technology.

The other type of BTI is also called PBTI (Positive BTI) that appears in NMOS transistors[7]. PBTI emerges as a problem after 40-nm high-k metal gate process technology.

The BTI-induced degradation has a permanent part and a recoverable part. The recoverable part recovers within 1 ns-order when the stress is removed but the permanent part remains forever. BTI under continuous stress is called static BTI. BTI alternating between stress and no stress is called dynamic BTI. The dynamic BTI effect depends on the frequency and the duty cycle of the stress. Because the degradation heavily depends on the stress condition, it is difficult to measure the BTI-induced degradation for modeling.

BTI is a kind of random discrete-charge-induced variations[8]. It is time-dependent phenomenon. Behavior of a single charge in the channel is becoming a significant problem on highly-scaled LSIs. Characteristics of the MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are fluctuated by the charge behavior. It is called the RTN (Random Telegraph Noise)[9, 10, 11]. BTI is basically the same degradation as the

RTN. But it has the effect for the longer-term than RTN.

1.2.1 History of BTI

BTI was first reported in 1967[12]. The theories of the physical origin of BTI are still discussed. Conventionally, the R-D Model (Reaction-Diffusion Model) is one of the major theories[13, 14]. The physical origin of NBTI according to the R-D Model is explained as follows. Fig. 1.1 shows the bond model of the silicon (Si) crystal. Four bonds of a Si atom combine with other Si atoms. But a bond of a Si atom on the Si-SiO_2 surface combines with a Si, an oxygen (O) , or a hydrogen (H) . The atomic bonds with O and H are reactive. In the SiO_2 film, almost all Si atoms combine with O. But some Si atoms combine with H, because the SiO_2 film near the Si substrate is amorphous. Fig. 1.2 shows the liberations of atomic bonds of H and Si. They generate uncombined pairs of electrons, which are called the interface traps (ITs). Fig. 1.3 shows that the ITs capture the carriers of PMOS (holes). Then, the number of the carriers is decreased and then the channel current decreases. NBTI is based on this phenomenon. The model of the initial state is shown in Eq. (1.1).

$$\mathrm{Si_3} \equiv \mathrm{SiH} \tag{1.1}$$

There is no pair of electrons in Eq. (1.1). If the high electric field is applied, it becomes Eq. (1.2).

$$\mathrm{Si_3} \equiv \mathrm{SiH} \rightarrow \mathrm{Si_3} \equiv \mathrm{Si} \cdot + \mathrm{H} \tag{1.2}$$

Where, $\cdot$ is a shared pair of electrons.

After the R-D Model, the Atomistic Trap-Based Model (AT-B Model) is proposed[15]. The physical origin of BTI according to the model is introduced in the next subsection.

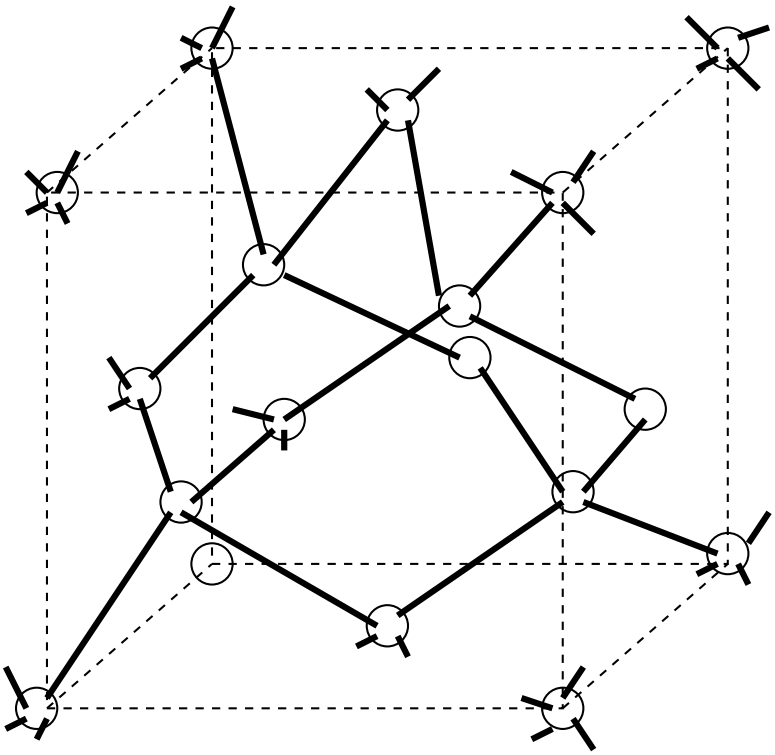

Figure 1.1: Crystal structure of Si.

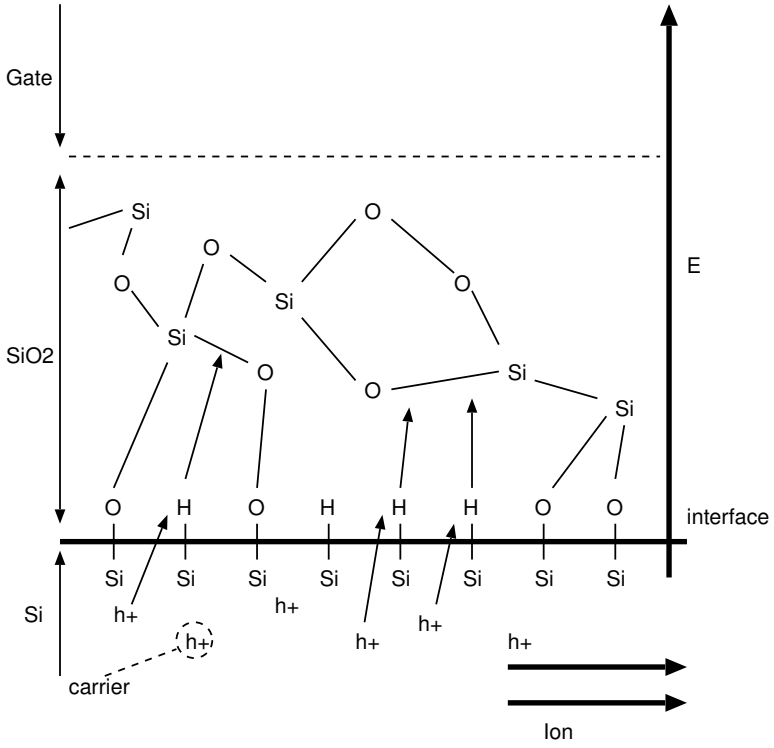

Figure 1.2: Liberation of H on Si-SiO_2 surface of PMOS.

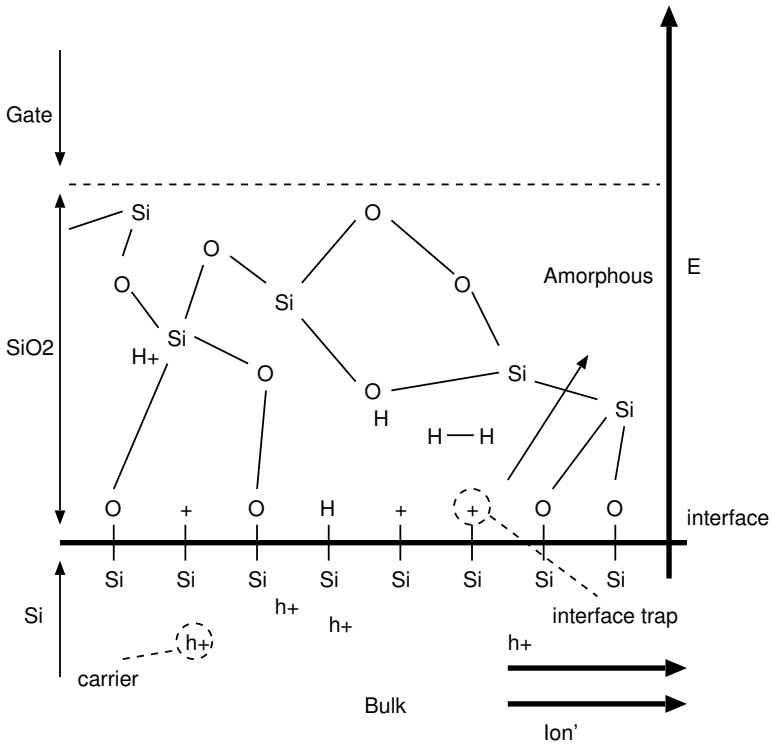

Figure 1.3: Hole captured by trap on Si-SiO_2 interface of PMOS.

1.2.2 Physics of BTI

The physical origin of BTI in the AT-B model is described as the defects in the gate dielectric which called oxide traps (OTs)[15]. Fig. 1.4 shows the defects. The channel current is fluctuated when the gate of transistors are applied by the stress bias. Because the defects trap and de-trap the carriers in the channel. When the defects are capturing the carriers, the channel current decreases. Then the V_{th} decreases, and vice versa.

The defects have time constants of trapping and de-trapping which are called the capture time (τ_{c}) and the emission time (τ_{e}), respectively. Those time constants are log-normally distributed from 10^{-9} s to 10^{9} s and depend on the voltage and the temperature[16, 17]. When the stress bias is applied to the gate, τ_{e} and τ_{c} become longer and shorter, respectively. Therefore, the V_{th} is easy to be degraded in the stress condition. When the defects which have long-term τ_{e} capture the carriers, the V_{th} is changed permanently in effect.

The V_{th} shift of BTI is explained by a combination of charge trapping/detrapping and a diffusion process in recent study[18, 19].

1.2.3 Impact on Circuits of BTI

The effects of BTI on the circuits are introduced. BTI-induced degradations become significant problems of the circuit performance[20, 21, 22, 23]. The performance is degraded for the long-term use by the BTI effect.

If logic circuits are degraded by the BTI effect, their delays increase. In the case of

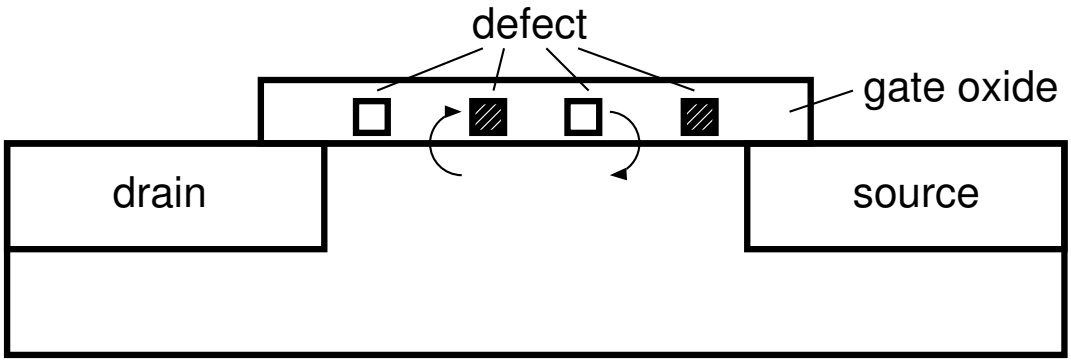

Figure 1.4: Physical origin of BTI.

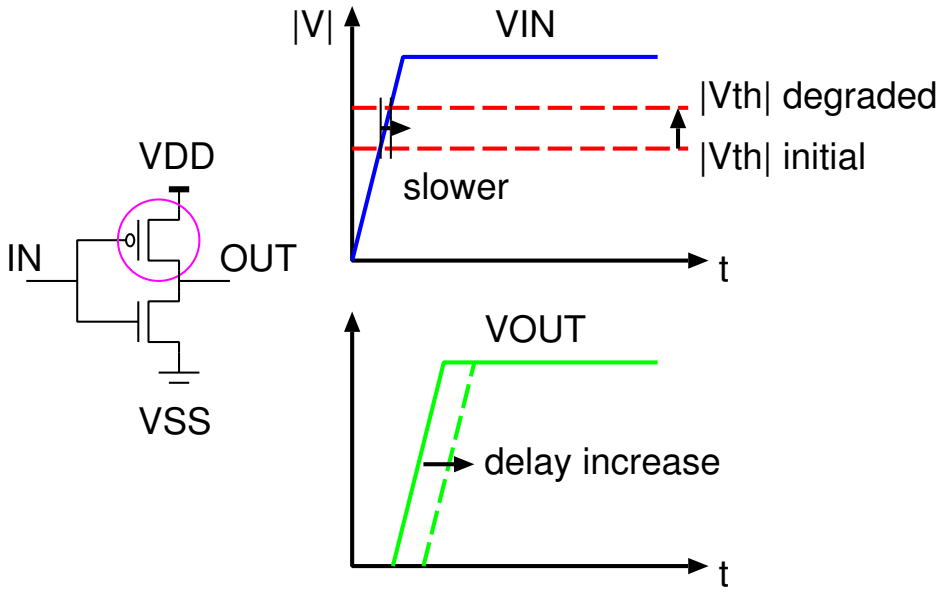

Figure 1.5: NBTI-induced degradation of circuit delay.

an inverter, either the NMOS or the PMOS is degraded in its operation. When the input signal is high, the NMOS is degraded by PBTI. When the input signal is low, the PMOS is degraded by NBTI. For example, Fig. 1.5 shows the illustration of the NBTI-induced degradation of circuit delays. When the V_{th} of the PMOS in the inverter increases, it becomes slower for the input voltage to exceed the V_{th}. Then the delay of the output voltage increases.

Memory circuits which degraded by BTI-induced degradations are threatened by bit errors[24]. Stability of SRAM is sensitive for the variability of characteristics of MOSFETs[25]. Therefore, SRAMs are weak in the degradations[26].

1.3 Process Variation

This section introduces process variations. Characteristics of MOSFET are fluctuated by various factors of the fabrication process. Process variations of LSIs are as follows.

- variation by fluctuations of the temperature and the gas flow of the fabrication process
- variation by the random dopant fluctuation

- variation by locations of the masks and the pattern densities of the lithography process

- variation of layouts by the optical proximity effect of the lithography and the mechanical strains of transistors

The yield ratio becomes worse when the process variations get larger. The yield ratio is an important factor that determines the cost of productions. If we want to keep the yield ratio high despite large process variations, we must estimate the performance which is the standard of the yield ratio low. But that means we undermine the value of the products. Therefore, it is important to evaluate and reduce the process variations.

The random dopant fluctuation (RDF) has the most significant effect on the variation in the 65 nm process[27]. In this case, the variations of gate depletions and gate oxide interface traps have the small effect. There is no correlation between the threshold voltages and physical parameters such as the gate length/width.

The process variations follow the Gauss distributions. We use the corner models to evaluate the process variations. In this model, the center condition μ, the high $V_{\rm th}$ condition $\mu + 3\sigma$, and the low $V_{\rm th}$ condition $\mu - 3\sigma$ are defined as typical, slow, and fast condition, respectively. The layout designers and the circuit designers consider process variations.

In 45 - 32 nm process, the line edge/width roughness, variation of body thickness, and optical proximity effect become the origin of process variations[28, 29, 30].

1.4 Correlation between Process Variation and BTI

This section introduces the physical origin of correlation between process variations and BTI. The circuit design considering the reliability is discussed.

Traditionally, the main source of the variations is the RDF (Random Dopant Fluctuation). It is location-dependent phenomenon. Now the main sources of the variations are random discrete-charge and RDF. The accurate prediction of the combination effects is necessary. Therefore, we should consider the reliability issues.

1.4.1 Physics of Correlation

The physical origin of the correlation between process variations and BTI-induced degradations is the amount of the interface traps and the oxide traps[31]. The flat band voltages V_{FB} of MOSFETs are determined by them and the difference of the work function between metal and semiconductor ϕ_{ms}.

The descriptions of the traps and charges are shown in Fig. 1.6. There are trapped charges in interface (surface level) Q_{it}, fixed charges Q_{f}, trapped charges in oxide Q_{ot}, and charges by movable ion Q_{m}. Charges Q_{ot} are the defects in SiO_2. They are the defects of the origins of the BTI. They are generated by the X-ray irradiation and the high energy electron irradiation. The traps are distributed in the oxide. Most of the charges Q_{ot} can be removed by low temperature anneal.

The relation among the traps, charges, and V_{FB} is shown in Eq. (1.3).

$$V_{\mathrm{FB}} = \phi_{\mathrm{ms}} - \frac{(Q_{\mathrm{f}} + Q_{\mathrm{m}} + Q_{\mathrm{ot}})}{C_{\mathrm{o}}} \tag{1.3}$$

Where, C_{o} is the capacitance of the oxide. The flat band voltages are shifted from ϕ_{ms} when the amount of the charges Q_{ot} are fluctuated. The process variations and the defects in oxide have the correlation because V_{th} of MOSFETs are the functions of the flat band voltages. The function is shown in Eq. (1.4).

$$V_{\mathrm{th}} \approx V_{\mathrm{FB}} + 2\Psi_{\mathrm{B}} + \frac{\sqrt{2\varepsilon_{\mathrm{s}} q N_{\mathrm{A}} (2\Psi_{\mathrm{B}} + V_{\mathrm{BS}})}}{C_{\mathrm{o}}} \tag{1.4}$$

According to the AT-B Model, the oxide defects capture the carriers which are electrons in NMOS transistors and holes in PMOS transistors. The charges of the defects Q_{ot} are holes (+) or electrons (−) in the case of NMOS or PMOS, respectively. When the number of defects and $|Q_{\mathrm{ot}}|$ become larger, $|V_{\mathrm{FB}}|$ and $|V_{\mathrm{th}}|$ become smaller. It means the MOSFETs which have large number of the oxide defects are the fast condition of the variations. The effect of BTI-induced degradation becomes larger if the MOSFET has large number of the defects. Therefore, the BTI has a large impact in the case of the fast condition.

Because the RDF has the most significant effect on the variation, the correlation between process variations and we assumed that BTI-induced degradations is weakly.

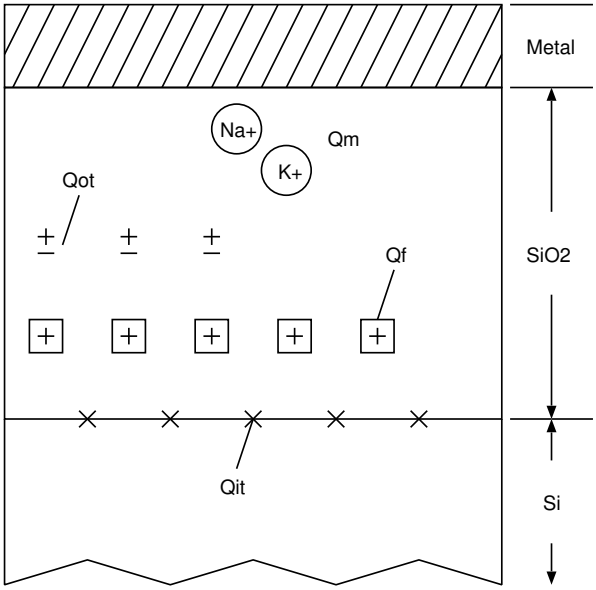

Figure 1.6: The descriptions of the traps and charges in the oxide.

1.4.2 Reliability-Aware Design Methodology

The design methodology considering process variations and BTI-induced degradations is introduced[32].

Delay calculations of the target logic circuit are the most important part of the timing analysis. There are two ways of the delay calculation, the back-end route which considers layout designs and the front-end route which does not consider layout designs. The points of analysis are as follows.

Critical path analysis verifying that the delay of the slowest critical path between FFs is shorter than the clock cycle.

Setup/hold time analysis checking the competition of clock signals and data signals.

Recovery/removal time analysis checking the competition of control signals of FFs (set/reset) and clock signals.

The methodology of the timing analysis are divided into dynamic and static.

Dynamic timing analysis running the delay simulations. The simulations require input patterns and output expectations. The violation paths and the critical path are detected as the malfunction of the circuit.

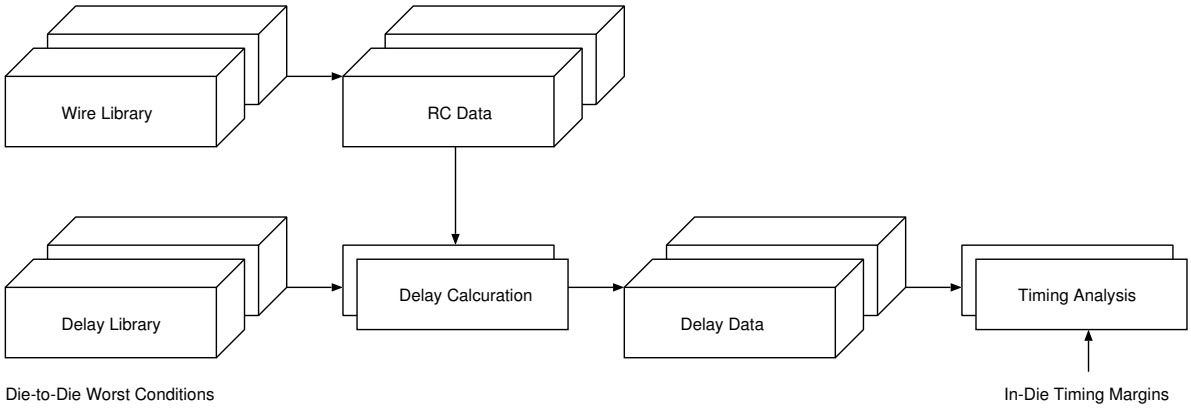

Figure 1.7: Timing analysis considering process variation[32].

Static timing analysis running the static path analyses. The analyses need accurate and particular timing constraints.

It is difficult for us to run the dynamic timing analysis of large scale integrations in terms of an amount of calculation and the completeness of the analysis. The static timing analysis is mainly used.

Process variations become problems with the cross talk and the IR drop in the timing analysis. Fig. 1.7 shows the methodology of the timing analysis considering process variations.

Within-die variation-aware analysis verifying with the libraries of the worst cases. Delays are calculated multiple times.

Die-to-die variation-aware analysis considering as timing margins. The margins are applied to both fast paths and slow paths.

Because the aging degradations, BTI and HCI (Hot Carrier Injection), are die-to-die variations, the correlation between process variations and BTI-induced degradations can be considered in the delay libraries.

1.5 Related Works

This section introduces related works.

BTI-induced degradations on ASICs are discussed in [15, 20, 33].

BTI-induced degradations on FPGAs are discussed in [34, 35, 36]. In [34], performance degradations on circuit elements of FPGAs induced by NBTI has been discussed. They propose Relaxing Bitstream Technique to gain back lost stability. Their proposed technique recovers an average of 53.2% of the lost Static Noise Margin (SNM) of SRAM cells and improves the failure in time rate by 2.48% for commercial FPGA devices. The impact of NBTI is mitigated by flipping the configuration bits. Ref. [37] is a survey paper about the reliability of FPGAs. It explains various faults of FPGAs and the detection/repair methods.

The correlation between process variations and BTI-induced degradations is discussed in [5, 38]. The analytical BTI model is proposed in [5]. In this model, the degradations of BTI are different among the conditions of process variations. It shows the degradation characteristics of ring oscillators with different initial frequencies. The differences are decreased by the degradations. This work did not discuss the physics of the correlation. In [38], BTI characteristics of 28 nm FDSOI process are shown. There is no correlation between process variations and BTI-indeuced degradations in this process. Because the channel is not doped in this process.

1.6 Purpose of This Study

In this study, the design methodology on ASICs and FPGAs considering the correlation between process variations and BTI-induced degradations is proposed. The purpose is the optimization of the design margins, which consider the reliability problems.

1.7 Brief Summary

Chapter 2 shows the results of simulation analyses of process variations and BTI-induced degradations. The analytical models of the degradations and the simulation methodology are discussed. The accurate predictions of the degradations are required by the circuit designers.

Chapter 3 shows the measurement methodologies and measurement results of process variations and BTI-induced degradations on FPGAs and ASICs. The results are discussed with the analytical models.

Chapter 4 introduces the design methodology considering correlation between process variations and BTI-induced degradations. The BTI-induced degradations on the circuits are predicted with the proposed methodology.

Chapter 5 concludes this study.

Chapter 2

Simulation Analysis of BTI

This chapter shows the analytical models of the reliability issues, the simulation methodologies, and the simulation results of BTI-induced degradations.

2.1 Outline

Simulation analyses are widely used for circuit designs. Circuit simulations of BTI-induced degradations are discussed in this chapter. It is important to predict the effect of BTI-induced degradation of circuits, because the lifetimes of circuits are limited by the degradations.

This chapter is organized as follows. Section 2.2 shows the analytical models of BTI-induced degradations. Section 2.3 shows the simulation methodology and the simulation results of BTI-induced degradations. Section 2.4 introduces the methodology of the simulation analysis of FPGAs. Section 2.5 summarizes this chapter.

2.2 BTI Modeling

There are many models which describe how the V_{th} (threshold voltage) is changed by the BTI-induced degradation. Several measurement methodologies are proposed in [39, 40, 41]. Some predictive BTI models are suggested in [5, 17, 42, 43]. The accurate model is still discussed, because the BTI-induced degradation critically depends on the stress condition and the process methodology.

This section introduces two analytical models of BTI, the R-D Model and AT-B Model.

2.2.1 Reaction-Diffusion Model

The R-D Model is proposed in [5, 42, 43]. Eqs. (2.1) (2.2) show the threshold voltage shifts of static and dynamic conditions.

$$\Delta V_{\mathrm{th,Static}} = A\left((1+\delta)t_{\mathrm{ox}} + \sqrt{Ct}\right)^{2n} \tag{2.1}$$

$$\Delta V_{\mathrm{th,Dynamic}} = \left(\sqrt{\frac{K_{\mathrm{v}}^2 \alpha T_{\mathrm{clk}}}{1-\beta_{\mathrm{t}}^{1/2n}}}\right)^{2n} \tag{2.2}$$

Eqs. (2.1) (2.2) express ΔV_{th} on static BTI and dynamic BTI, respectively. The parameters are determined as follows. The degradation factors, A and K_{v}, have dependence on the electrical field and the temperature. The parameter δ is a fitting parameter, t_{ox} is the oxide thickness. The parameter C has temperature (T) dependence as $C = T_{\mathrm{o}}^{-1} \exp\left(-E_{\mathrm{a}}/kT\right)$. The parameter E_{a} is the activation energy of hydrogen species, k is the Boltzmann constant, and T_{o} is constant with the value of 10^{-8} s·nm^{-2}. The time exponent parameter n is 1/6 for H_2 diffusions. If they are H diffusions, n becomes 1/4 instead. The parameter α is duty cycle, T_{clk} is the time period of one stress-recovery cycle, and β_{t} is fraction parameter of the recovery.

V_{th} is assumed to be degraded by 55% on continuous DC stress under the following condition. The supply voltage (V_{dd}) is 1.2 V and T = 100 °C. Device parameters are based on 65-nm process typical PMOS devices. The degradation time is 10 years ($= 3.1536 \times 10^8$s). Under the condition, V_{th} is degraded by 10% on stress-recovery cycle which is $\alpha = 0.5$ and $T_{\mathrm{clk}} = 0.01$ s. The degradation amount is consulted by [5]. Fig. 2.1 shows V_{th} degradations of static and dynamic NBTI under the above condition. Those parameters are also described in Table 2.1.

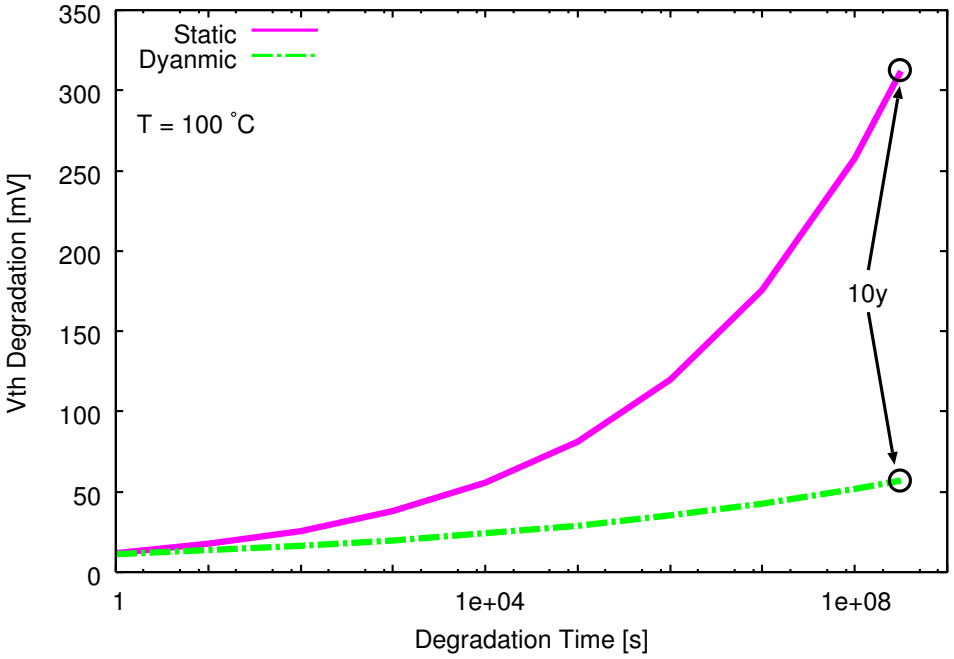

Figure 2.1: V_{th} degradation prediction under static/dynamic NBTI based on the R-D model.

Table 2.1: Parameter descriptions.

P.	Description	Value
A	Degradation Factor (Static)	-
K_{v}	Degradation Factor (Dynamic)	-
δ	Fitting Parameter	-
t_{ox}	Oxide Thickness	-
C	$= T_{\text{o}}^{-1} \exp\left(-E_{\text{a}}/kT\right)$	-
T	Temperature	100°C
k	Boltzmann Constant	1.38×10^{-23}J/K
E_{a}	Activation Energy of Hydrogen Species	0.49eV
T_{o}	Constant	10^{-8}s/nm^2
n	Time Exponent Parameter	1/6
α	Duty Cycle	0.5
V_{dd}	Supply Voltage	1.2V
T_{clk}	Time Period of Stress-Recovery Cycle	0.01s
β_{t}	Fraction Parameter of the Recovery	-

2.2.2 Atomistic Trap-Based Model

The shift of $V_{\rm th}$ ($\Delta V_{\rm th}$) is determined by characteristics and states of the defects in the gate dielectric in the AT-B Model[17]. If a defect captures carriers, $V_{\rm th}$ of the device increases. When the MOSFET has n defects, the degradation $\Delta V_{\rm th}$ at degradation time t can be calculated by Eq. (2.3).

$$\Delta V_{\rm th}(t) = \sum_{j=1}^{n} k_j(t) \cdot \mu_j \tag{2.3}$$

Where, j is the index of defects (1-n), and k_j is the state of the jth defect. When the jth defect captures carriers, $k_j = 1$. When the carrier is emitted, $k_j = 0$. They are determined by the capture probability $P_{\rm C}$ which is a function of the capture and emission time constants, $\tau_{\rm c}$ and $\tau_{\rm e}$, respectively. The number of defects n follows the Poisson distribution. Threshold voltage shifts of each defect μ_j are exponentially-distributed.

PMF (Probability Mass Function) f_n and CDF (Cumulative Distribution Function) F_n of n are shown in Eqs. (2.4) and (2.5).

$$f_n = \frac{N^n}{n!} \cdot e^{-N} \tag{2.4}$$

$$F_n = e^{-N} \sum_{i=0}^{n} \frac{N^i}{i!} \tag{2.5}$$

Where, N is the expected value of n and is explained as Eq. (2.6).

$$N = LWD_{\rm N} \tag{2.6}$$

Where, L and W are the length and width of the channel,respectively, and $D_{\rm N}$ is the density of the defect in gate oxide.

PDF (Probability Density Function) f_μ and CDF F_μ of μ are shown in Eqs. (2.7) and (2.8).

$$f_\mu = \frac{1}{\eta} \exp\left(-\mu/\eta\right) \tag{2.7}$$

$$F_\mu = 1 - \exp\left(-\mu/\eta\right) \tag{2.8}$$

Where, η is the expected value of μ and is explained as Eq. (2.9)[**?**].

$$\eta = \frac{s}{LW} \tag{2.9}$$

Where, s is the coefficient of η.

Long-term P_{C} is shown in Eq. (2.10)[44].

$$P_{\mathrm{C}}(t) = \frac{\tau_{\mathrm{e}}^*}{\tau_{\mathrm{c}}^* + \tau_{\mathrm{e}}^*}\left[1 - \exp\left\{-\left(\frac{1}{\tau_{\mathrm{e}}^*} + \frac{1}{\tau_{\mathrm{c}}^*}\right)t\right\}\right] \tag{2.10}$$

$$\frac{1}{\tau_{\mathrm{c}}^*} = \frac{DF}{\tau_{\mathrm{ch}}} + \frac{1-DF}{\tau_{\mathrm{cl}}} \tag{2.11}$$

$$\frac{1}{\tau_{\mathrm{e}}^*} = \frac{DF}{\tau_{\mathrm{eh}}} + \frac{1-DF}{\tau_{\mathrm{el}}} \tag{2.12}$$

Where, DF, τ_{e}^*, and τ_{c}^* are the duty factor, the effective capture time constants, and the effective emission time constants, respectively. Duty Factor (DF) becomes 1 if the gate terminal of MOSFETs is applied by some amount of DC bias to turn on. Then Time constants τ_{e} and τ_{c} are τ_{eh} and τ_{ch} respectively. If the gate terminal of MOSFETs has no DC bias, Time constants τ_{e} and τ_{c} are τ_{el} and τ_{cl} respectively. Time constant τ_{el} is assumed log-normally distributed from 10^{-9} s to 10^{9} s[45, 16]. The relations between τ_{el} and the other time constants are as follows: $\tau_{\mathrm{ch}} \simeq 0.01\tau_{\mathrm{el}}$, $\tau_{\mathrm{eh}} \simeq 100\tau_{\mathrm{el}}$, $\tau_{\mathrm{cl}} \simeq 100\tau_{\mathrm{el}}$[46]. Those characteristics are based on the result of 45 nm process, nevertheless the circuits of 65 nm process are simulated in the later part. The characteristics are assumed different at a process node. Because there are few reports which show the characteristics of the time constants of 65 nm process, the characteristics of 45 nm process are consulted.

The specific calculation methodology of V_{th} degradation is as follows.

1. set the length and width of the channel of the device L and W
2. set the number of the defects n
3. set characteristics of the defects, μ, τ_{eh}, τ_{ch}, τ_{el}, and τ_{cl}
4. calculate P_{C} at t and determine k of each defect
5. calculate ΔV_{th} at t

Fig. 2.2 shows the flow chart of this methodology. Here, the maximum of t is 10 years (3.1536×10^8 s). The time step size of t is 1 s during 1-10 s, 10 s during 10-100 s, 100 s during 100-1000 s, and exponentially increased. In Fig. 2.2, Pc<rand ? means comparing

P_{C} with random number (0-1) because k is determined by the stochastic distribution. The characteristics of the defects are also determined by the same way.

Fig. 2.3 shows the calculation result of ΔV_{th} under the conditions $N = 800$, $V_{\mathrm{th}} = 500$ mV, and $DF = 50$ %. The X axis is logarithmic scale and indicates the degradation time, the Y axis indicates ΔV_{th}. Those results have changed in each calculation even though the conditions are the same. Because the random numbers are used in those calculations. Fig. 2.4 shows the average of the calculation results of 100 times and its fitting function. It follows the logarithmic function. The defects in gate oxide capture/emit the carriers with the time constants which distribute log-normally. It is well known that ΔV_{th} follows the logarithmic function[19]. The results are saturated near 10^8 s because the constants τ_{el} are distributed at the maximum 10^9 s.

The theory that BTI-induced degradations are based on both the AT-B Model and R-D Model is proposed in [18]. The experimental results fit well with the combination model[19]. In this study, experimental results follow the AT-B Model because the DUTs are measured repeatedly.

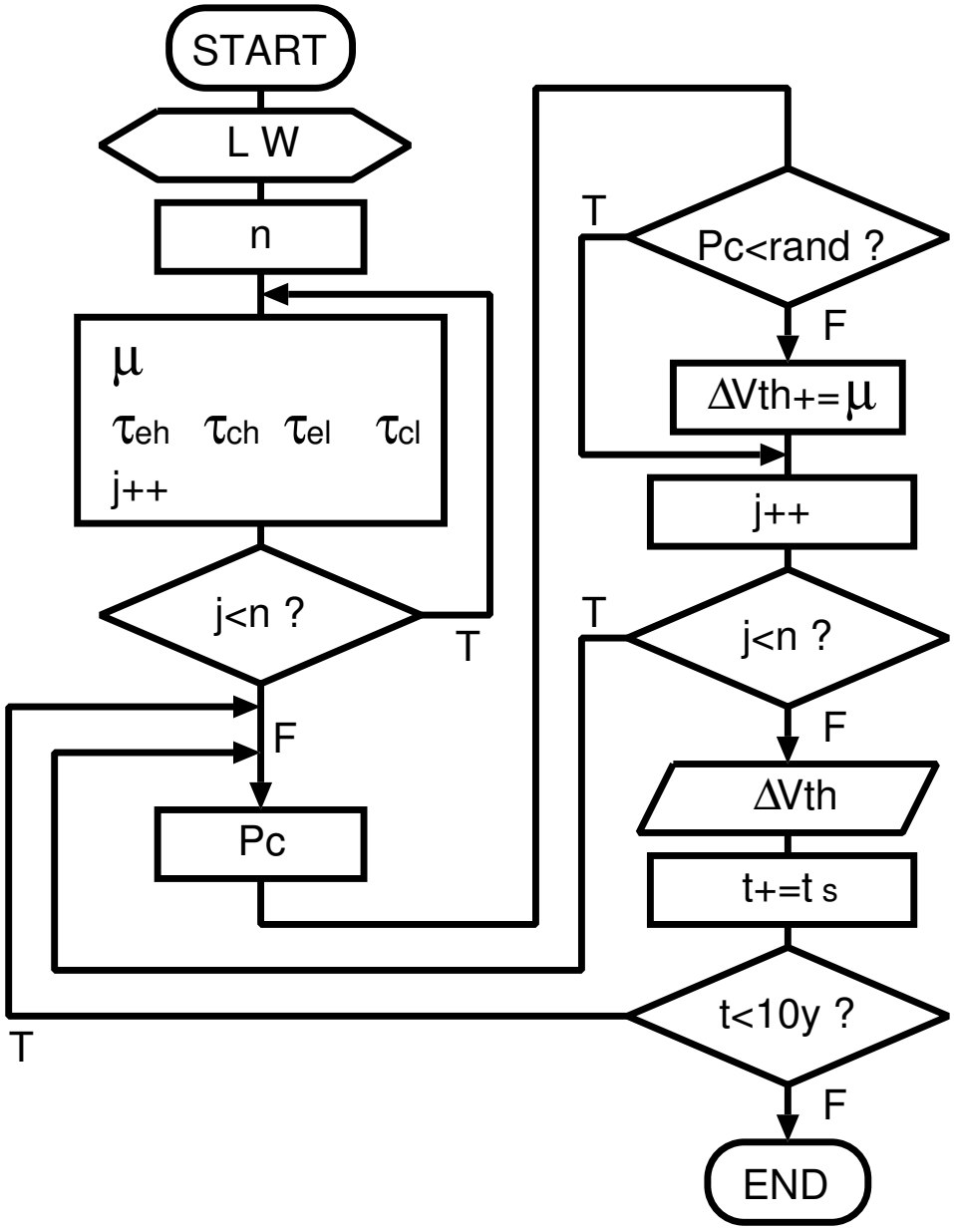

Figure 2.2: Flow chart of calculation of threshold voltage degradation using Atomistic Trap-Based Model.

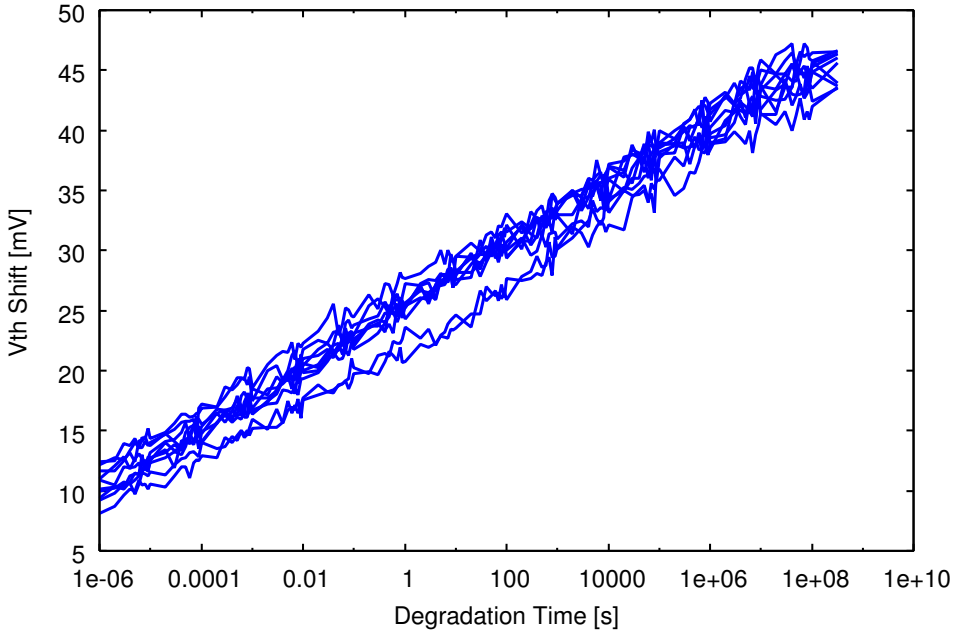

Figure 2.3: Calculation result of threshold voltage degradation, condition $N = 800$, $V_{\mathrm{th}} = 500$ mV, $DF = 50$ % (10 times).

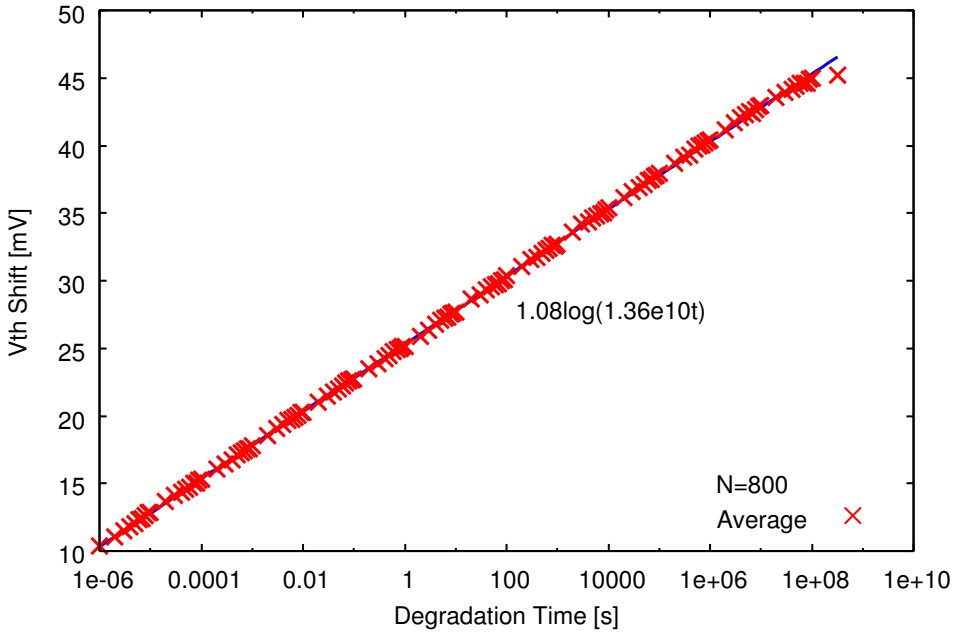

Figure 2.4: Calculation result of threshold voltage degradation, condition $N = 800$, $V_{\mathrm{th}} = 500$ mV, $DF = 50$ % (average of 100 times, fitting function $\Delta V_{\mathrm{th}} = 1.08\log(1.36\times10^{10}t)$).

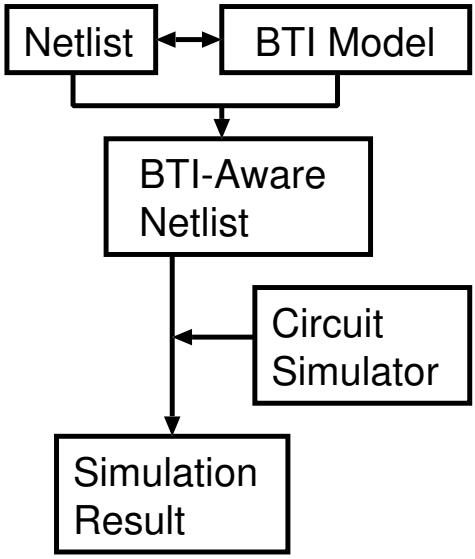

Figure 2.5: BTI-aware circuit simulation methodology.

2.3 Simulation Analysis of BTI-Induced Degradation

This section introduces the simulation methodology considering the reliability issues and shows the results of the simulation analyses.

2.3.1 BTI-Aware Simulation Methodology

The BTI-aware netlist are used to analyze the characteristics of the BTI-induced degradation of circuits. Here, the simulation methodology using the BTI-aware netlist is introduced. For each time t, predicted values of the V_{th} degradation are applied for each MOSFET in the netlists. Fig. 2.5 shows the BTI-aware netlist created from the original netlist and the BTI model for the simulation analysis.

Fig. 2.6 shows an example of the BTI-aware netlist using BSIM4 for HSPICE simulations[47]. In case of BSIM4, the parameter of threshold voltage VTH0 of each MOSFET can be controlled by the parameter DELVTO. V_{th} of the MOSFET is shifted to the amount of DELVTO. Parameters dvthn and dvthp are configured for an NMOSFET and a PMOSFET in this example.

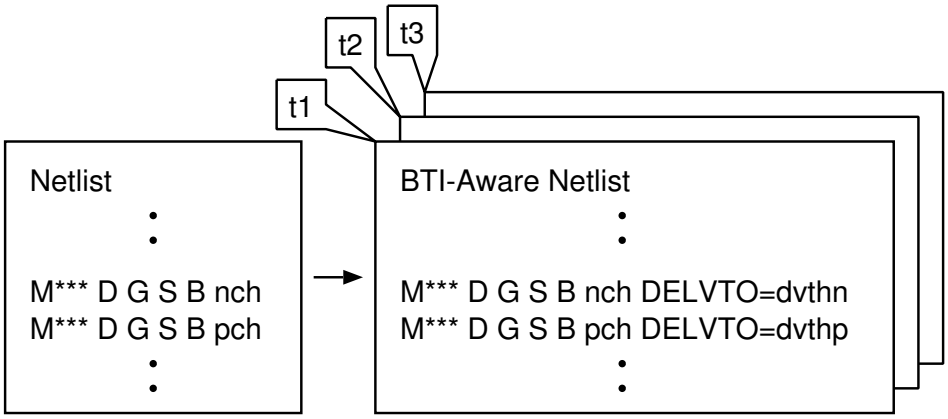

Figure 2.6: Example of BTI-aware netlist.

2.3.2 Simulation Results of Delay Characteristics on FPGA and ASIC

The degradations of two types of ROs are simulated. Simulation conditions are as follows: the process node is 65 nm bulk process, the variation condition is typical, the supply voltage is 1.2 V, and the temperature is 80°C. BTI-aware netlists are used in this simulation. Degradations of threshold voltage are calculated by the AT-B Model. The degradation time is 10 years (3.1536×10^8 s).

One of the simulation circuit is shown in Fig. 2.7. It is a 17-stage RO with NAND enable. The initial frequency is 1.232 GHz.

The other circuit is shown in Fig. 2.8. It is an oscillation circuit which consists of 4-stage CMOS multiplexers. It represents a logic element chain of the FPGA. The schematics of internal circuits of FPGAs are not disclosed. This circuit is analyzed instead. Furthermore, Sec. 2.4 shows simulation analysis of FPGAs. The oscillation path is A and the enable is B. The initial frequency is 3.736 GHz.

The results are shown in Fig. 2.9 and 2.10. Note that the X axis is a log-scale. The degradations follow a logarithmic function. Because the V_{th} shifts of BTI-induced degradations follow the model of the logarithmic function.

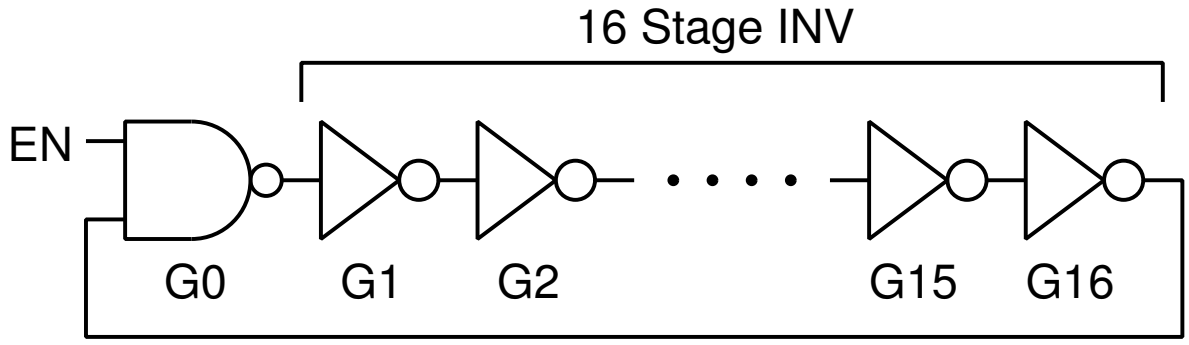

Figure 2.7: Simulation circuit, 17-stage ring oscillator.

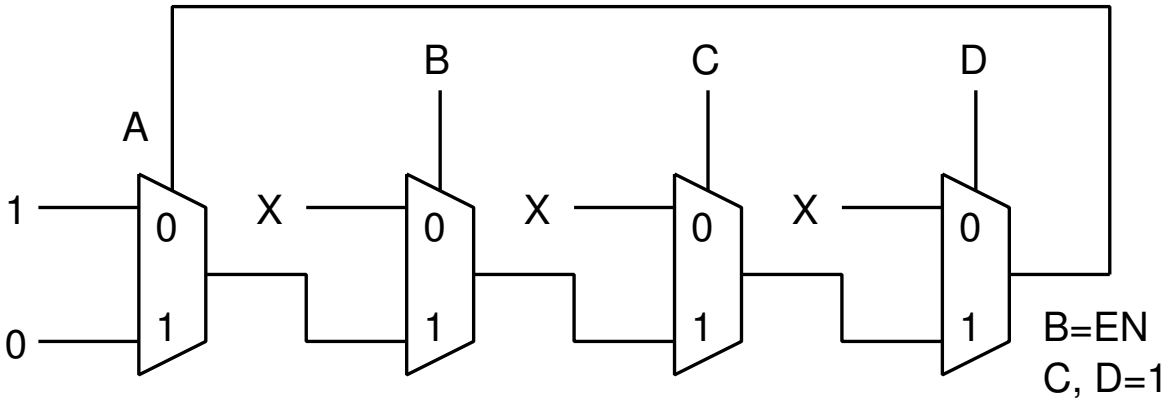

Figure 2.8: Simulation circuit, 4-stage MUX chain.

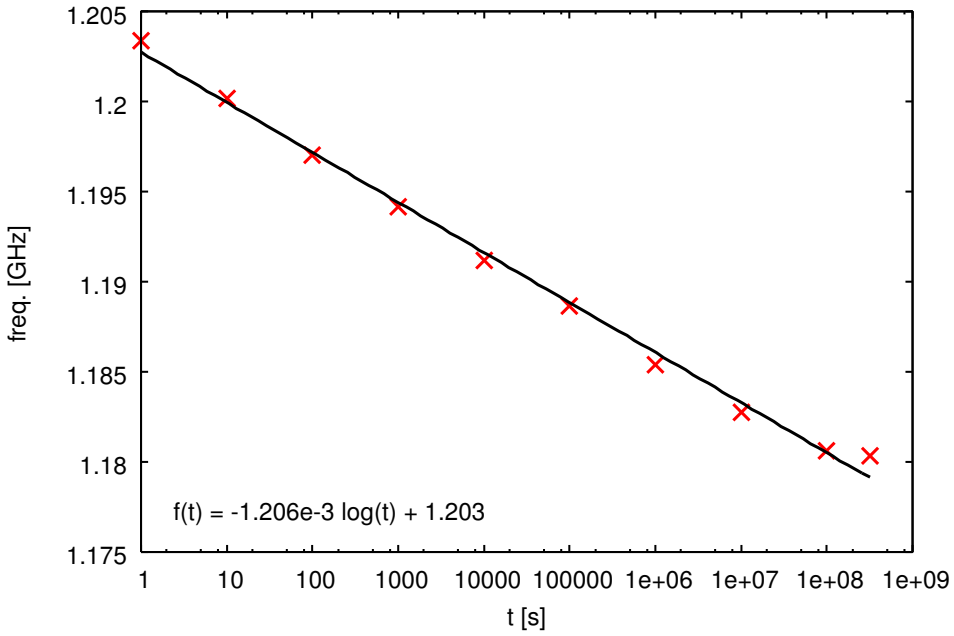

Figure 2.9: Simulation result of 17-stage ring oscillator.

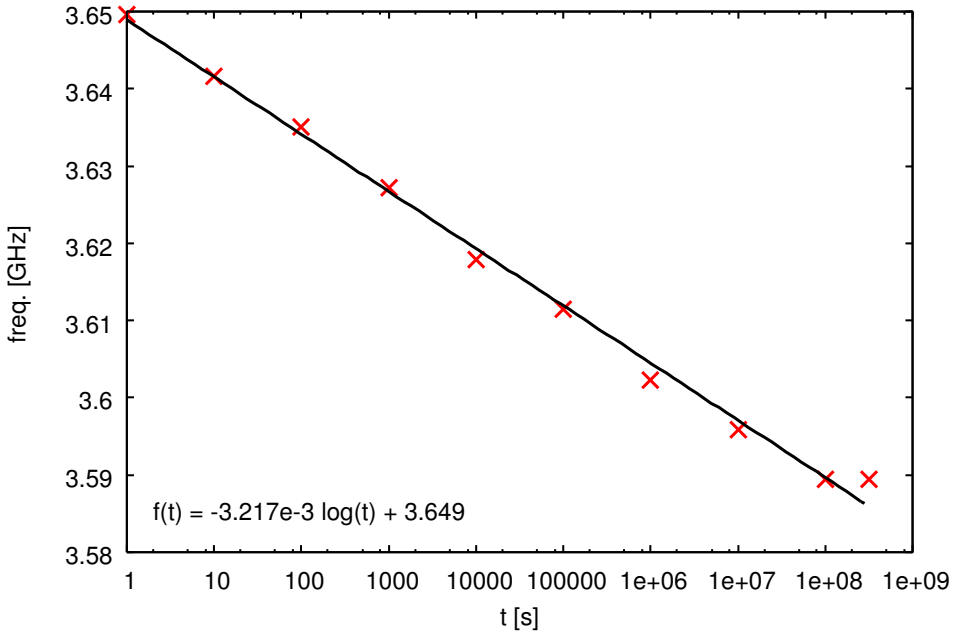

Figure 2.10: Simulation result of 4-stage MUX chain.

2.3.3 Simulation Result of Duty Factor Characteristics on Inverter

Delay degradations caused by both BTIs of an inverter (Fig. 2.11) is evaluated. The simulation conditions are as follows. Rectangle pulses with 1 ns rise and 1 ns fall time are applied to the circuits via two inverters. The output nodes of the circuits are connected to fan-out of 4 inverters. Threshold voltage V_{th} degradations with the AT-B Model are calculated[17]. The transistor size is the 65 nm process standard size and the temperature is 25°C. BTI-aware netlists are used in this simulation. The degradation time is 10 years (3.1536×10^8 s).

When the input signals are low, PMOS transistors are stressed and degraded by NBTI. When they are high, NMOS transistors are stressed and degraded by PBTI. Relationship between duty factor of the stress bias on PMOS transistors (DF_{p}) and that on NMOS transistors (DF_{n}) is expressed as $DF_{\mathrm{p}} = 1 - DF_{\mathrm{n}}$. The degradations of the condition $DF_{\mathrm{p}}/DF_{\mathrm{n}} = 0.0/1.0$ to $DF_{\mathrm{p}}/DF_{\mathrm{n}} = 1.0/0.0$ are evaluated. The degradation rates of NBTI and PBTI are assumed equivalent.

The results of delay degradation analyses under both BTIs of an inverter are shown in Fig. 2.12 and Fig. 2.13. The results show the rise time delays (T_{dr}) or the fall time delays (T_{df}) increase with the degradation time and are degraded by 15 % after 10 years in the condition of $DF_{\mathrm{p}} = 1.0$ or $DF_{\mathrm{n}} = 1.0$. In the condition of $DF_{\mathrm{p}} = 0.0$ or $DF_{\mathrm{n}} = 0.0$, the degradations affect a little on T_{dr} or T_{df}.

The delays, T_{dr} and T_{df}, increase due to the degradations. Because they become slower for the gate voltage to exceed V_{th} than the initial condition when V_{th} increases. Those effect result in T_{dr} and T_{df} increases. In the condition of only the NBTI effect ($DF_{\mathrm{p}}/DF_{\mathrm{n}} = 1.0/0.0$), T_{dr} increases and T_{df} slightly decreases. It shows the degradation of PMOS transistors has a large impact on T_{dr} but a small impact on T_{df} because V_{th} of PMOS transistors is only related to T_{dr}. The result of the condition of only the PBTI effect ($DF_{\mathrm{p}}/DF_{\mathrm{n}} = 0.0/1.0$) can be explained in a similar way.

The duty factor characteristic are shown in Fig. 2.14. The results show T_{dr} increases with DF_{p} and T_{df} increase with DF_{n}. NBTI becomes dominant in the condition $DF_{\mathrm{p}} \geq 0.5$ and PBTI becomes dominant in the condition $DF_{\mathrm{n}} \geq 0.5$. Those can be explained in the same way as the preceding paragraph.

The average delay times of T_{dr} and T_{df} are shown in Fig. 2.15. The average delay times at a certain degradation time are almost constant as long as the circuits are caused by both BTIs. For example, the delay times are between 17.4 ps and 17.6 ps after 10 years. The average delay time degradations are bigger when both BTIs are effective ($0.1/0.9 < DF_{\mathrm{p}}/DF_{\mathrm{n}} < 0.9/0.1$) than when only NBTI or PBTI is effective ($DF_{\mathrm{p}}/DF_{\mathrm{n}} = 0.0/1.0$ or $1.0/0.0$).

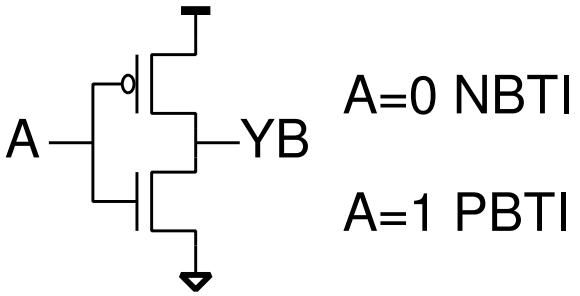

Figure 2.11: NBTI and PBTI of a inverter circuit.

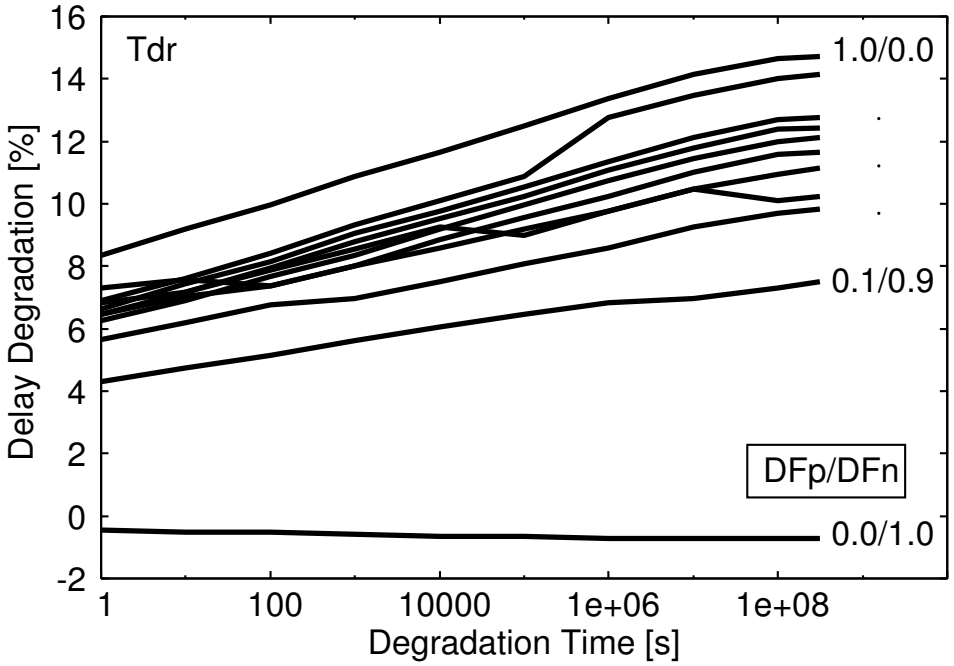

Figure 2.12: Rise time delay degradation of CMOS inverters caused by both BTIs.

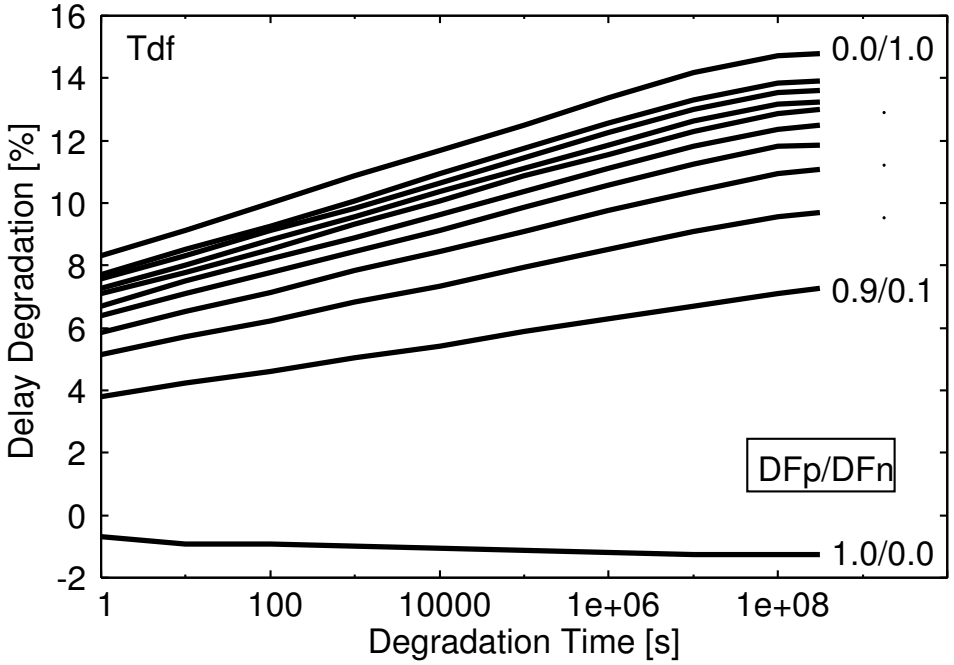

Figure 2.13: Fall time delay degradation of CMOS inverters caused by both BTIs.

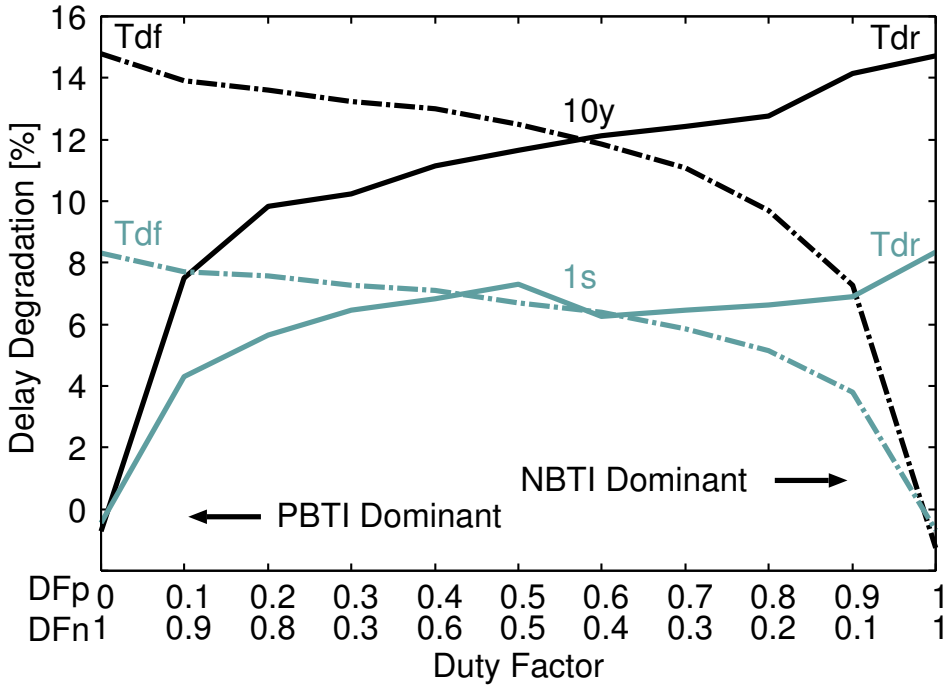

Figure 2.14: Duty factor characteristic of rise and fall time delay degradation of CMOS inverters caused by both BTIs.

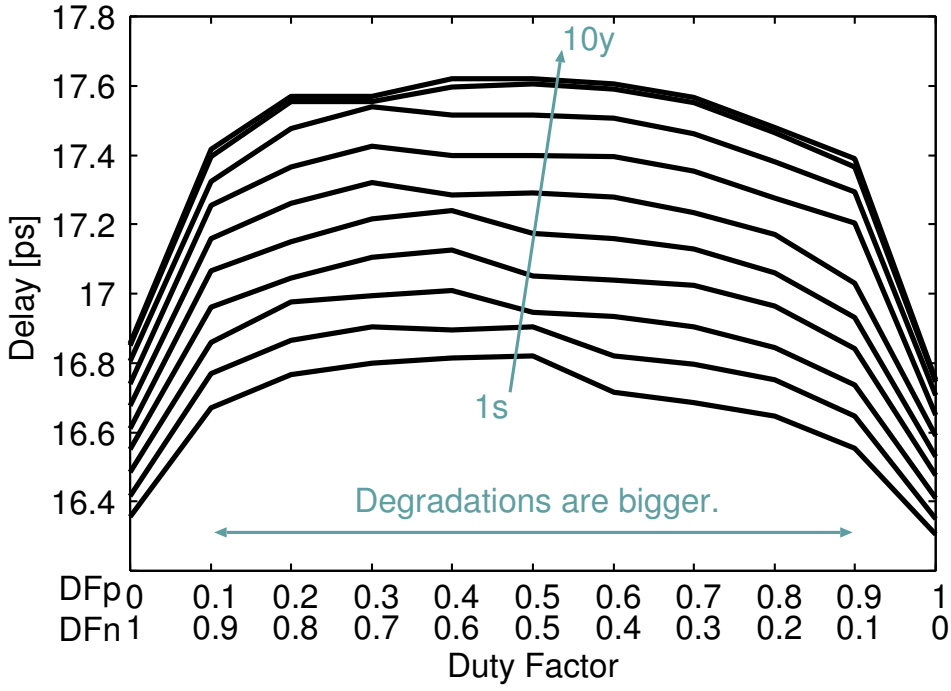

Figure 2.15: Duty factor characteristic of average delay time degradation of CMOS inverters caused by both BTIs. The degradation times are from 1s to 10 years.

2.4 Simulation of FPGA Routing Structure

This section shows characterization of NBTI-induced delay degradations on routing resources in FPGAs.

2.4.1 Simulation Circuit of Routing Structure

FPGAs consist of logic parts and connection parts. The logic parts are able to configured to any logic by users. The connection parts establish connection between the logic blocks by using reconfigurable switch matrices. The connection parts have a unique circuit structure which includes an NMOS switch transistor and a weak-keeper PMOS transistor called a level restorer or a half latch. The level restorers restore the voltage level lowered by the NMOS switch. The half latches are used to fix inputs of the logic blocks to a constant value and are used for multiplexers which select a path on routing structures of FPGAs to prevent the input node of the logic blocks from floating. The BTI-induced degradation of the delay time on the routing structures is a dominant design concern on FPGAs because the delay time of the routing structures determines the circuit performance. FPGAs have an ability to reconfigure to tackle such a degradation effect.

An FPGA device consists of programmable logic blocks (PLBs) and programmable interconnects (PIs). Fig. 2.16 shows a structure of an island-style FPGA. PLBs include several logic elements consisting of look up tables (LUTs), flip-flops and configuration memories. Users can configure it to any logic they want. PIs include a lot of switch matrices, wires and routing switches. The BTI degradations of the routing switch shown in Fig. 2.17 are focused on, which is commonly used in FPGAs [48, 49]. There are two inverters (INV0 and INV1), an NMOS transistor to be used for a switch, a pull-up PMOS transistor and a configuration bit determining ON/OFF of the switch. If the configuration bit stores 1, the switch is ON. If 0 is stored, the switch is OFF and the input node of INV1 floats without pull-up PMOS transistors. The PMOS transistor is called a level restorer or a half latch to restore the voltage level lowered by the NMOS or to prevent INV1 from floating. Fig. 2.18 is an illustration of what half latches are at the circuit level [50]. When one of the NMOS switches is on, the pull-up PMOS transistor will be driven by the incoming signals from the routing network. The half latch circuit can be used to produce a fixed output value of 0 or 1, as needed by the

user's design. Note that its performance is not degraded by NBTI because the output value is constant.

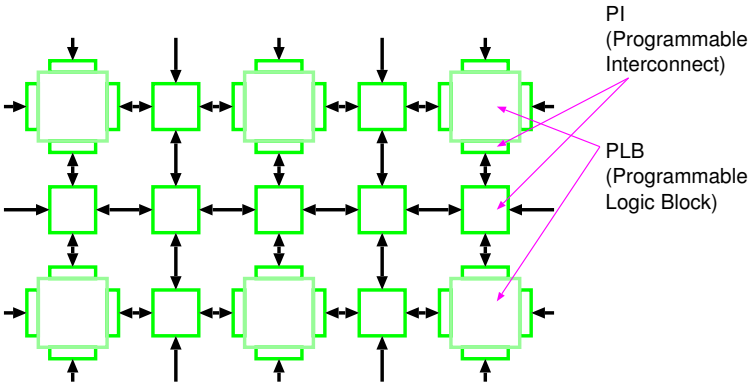

Figure 2.16: FPGA architecture.

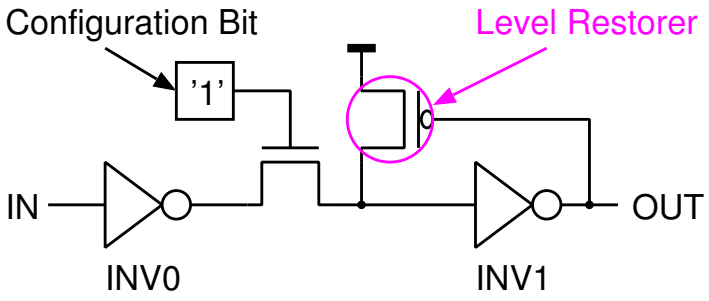

Figure 2.17: Routing switch with level restorer.

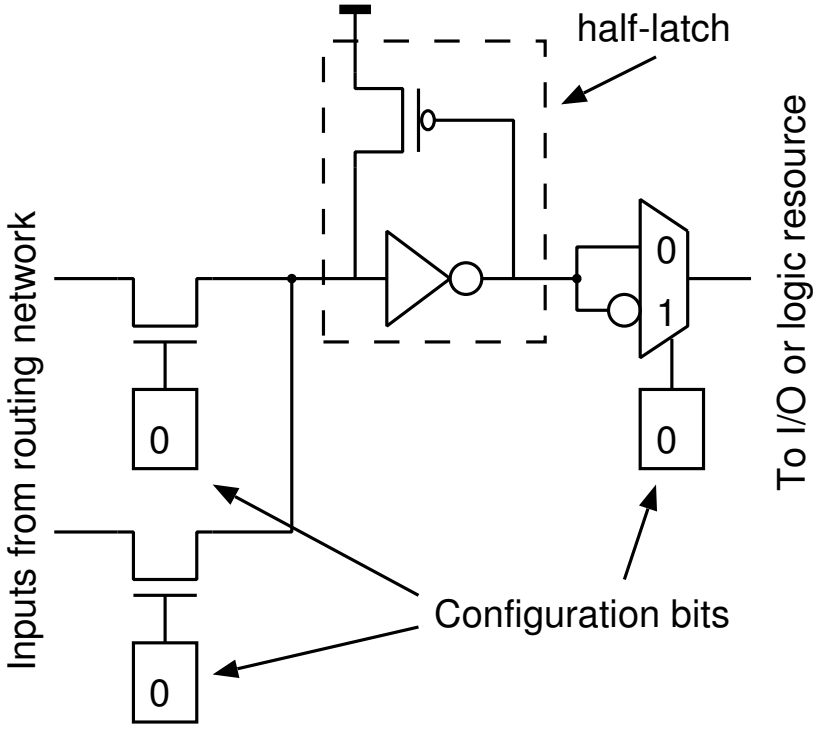

Figure 2.18: Half latch circuit in FPGA.

2.4.2 Simulation Analysis of NBTI-Induced Degradation on Routing Structure

The NBTI degradation on two structures, the routing switch with and without a level restorer are evaluated and compared by circuit simulations. The delay degradations under the NBTI effect are analyzed. The transistor size is the 65 nm process standard size and the temperature is 25 °C. BTI-aware netlists are used in this simulation. Degradations of threshold voltage are calculated by the R-D Model. The degradation time is 10 years (3.1536×10^8 s).

Fig. 2.19 shows the routing switch without any level restorer. Fig. 2.20 shows the routing switch with the multiple inverters and cascaded level restorers. The rise and fall delays of Fig. 2.20 are close to those of Fig. 2.19 in the initial condition by duplicating inverters (M=2) and cascading level restorers. In order to compare the degradation of these circuits under equal conditions, the delay difference at the initial state is within 0.8%. The size of the level restorer transistor should be smaller than the other transistors [51]. The level restorer can be weak to stack PMOS transistors without increasing load capacitance. The purpose of comparing those two circuits is to evaluate difference of FPGAs over general ASICs.

The results of delay degradation analysis are shown in Fig. 2.21 and Fig. 2.22. The word LR in those figures is the abbreviation of level restorer. The left side of Fig. 2.21 shows degradations near $t = 0$. Note that the initial degradations are both 0 % regardless of level restorer. Degradations at $t = 0$ are 0 % in all the graphs showing time dependent degradations hereafter. The rise time delay (T_{dr}) is increasing when the circuits are degraded by NBTI. Delay increase of the circuit without any level restorer is 1.9 times larger than that of the circuit with level restorers. The fall time delay (T_{df}) is decreasing when the circuits are degraded by NBTI as shown in Fig. 2.22. Delay decrease of the circuit with level restorers is 2.4 times larger than that of the circuit without any level restorer.

The PMOS transistor in INV1 is the most sensitive to NBTI degradation from sensitivity analysis, because output of INV1 is connected to FO4 inverters. If its V_{th} increases, it becomes harder for V_{gs} to exceed V_{th} than the initial condition. The effect results in T_{dr} increase. If its V_{th} decreases, it becomes easy for V_{gs} to exceed V_{th} and the effect

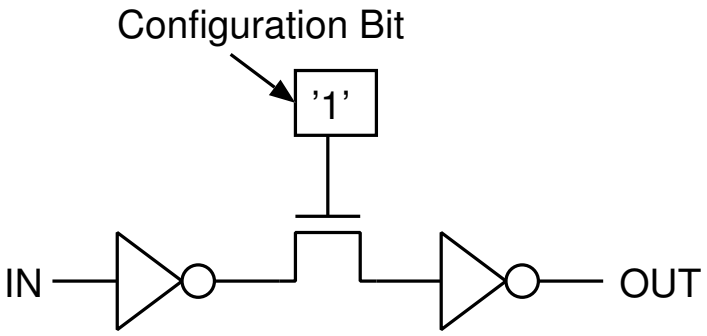

Figure 2.19: Routing switch without level restorer.

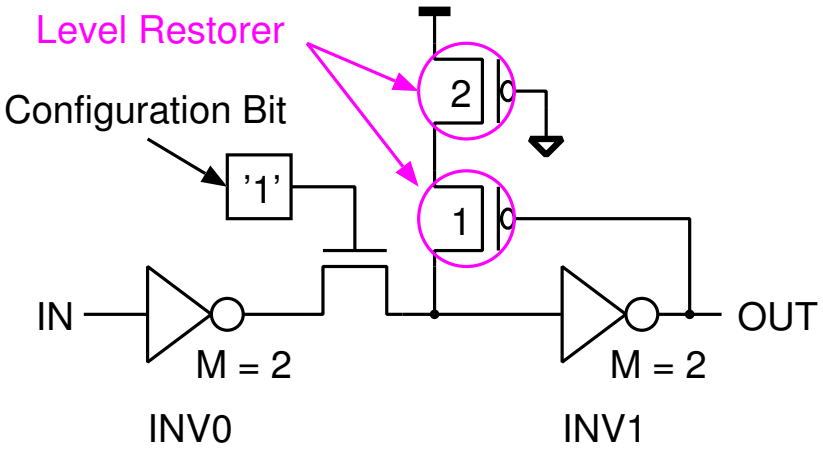

Figure 2.20: Routing switch with cascaded level restorers.

results in T_{df} decrease. Those two effects are caused by sensitivity of INV1. The level restorer PMOS easily becomes OFF by the degradation. It becomes ON when OUT falls, and becomes OFF when OUT rises. The level restorer helps OUT to fall under the degradation condition, while it interferes with OUT from rising.

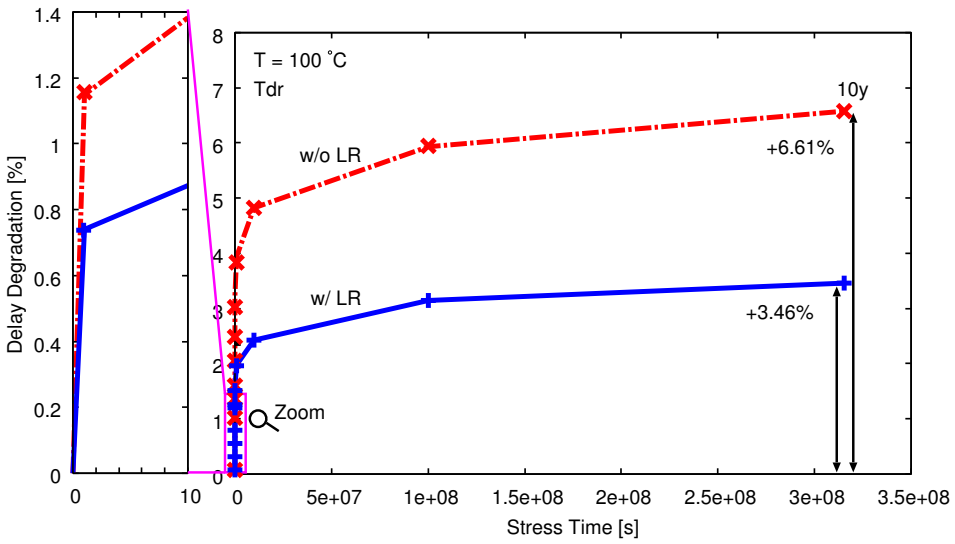

Figure 2.21: T_{dr} degradation under accelerated NBTI condition at 100°C.

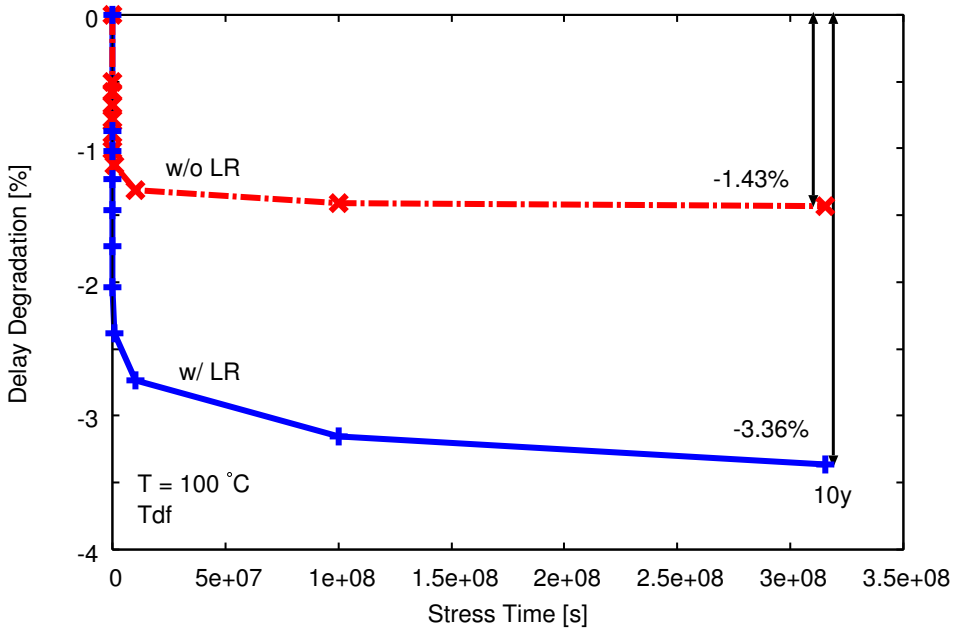

Figure 2.22: T_{df} degradation under accelerated NBTI condition at 100°C.

2.5 Summary

The circuit simulation methodologies of BTI-induced degradations and their results are introduced in this chapter.

The analytical models of the BTI-induced degradations are introduced. The physical origin of the R-D model is the interface traps between the gate oxide and the channel. Threshold voltage shifts follow the power-law of the degradation time. The physical origin of the AT-B model is the oxide trap. Threshold voltage shifts follow the logarithmic function of the degradation time.

The BTI-aware simulation methodology is introduced. The BTI-aware netlists which consider the threshold voltage shifts of BTI-induced degradations are used. The accurate predictions of BTI-induced degradations are achieved by simulations using the BTI-aware netlists.

The NBTI and PBTI-induced delay degradations on CMOS inverters are analyzed. The rise time delay or the fall time delay increase 15 % after 10 years in the case that duty factor is 1. If the input signal is often low, NBTI becomes dominant on the delay degradation. If it is often high, PBTI becomes dominant on the delay degradation. The average of delay time degradations is almost constant except in the condition that the input signal is always high or low. In the condition, the delay degradation is smaller.

The NBTI-induced frequency degradations on ring oscillators are analyzed. The frequency degradations follow a logarithmic function. Because the V_{th} shifts of BTI-induced degradations follow the model of the logarithmic function.

The NBTI-induced delay degradations on FPGA routing paths are analyzed. In the case of an independent routing switch, the rise delay time increases by 3.46 % and the fall delay time decreases by 3.36 % on the 10 years degradation at 100 °C. Threshold voltage degradation on the pull-up PMOS (level restorer/half latch) is the main cause of the NBTI-induced delay degradation.

Chapter 3

Measurement of Process Variation and BTI

This chapter shows the measurement results of process variations and BTI-induced degradations on the FPGA and ASICs.

3.1 Outline

Ring oscillators (ROs) on the FPGA and ASICs are measured to analyze their characteristics of process variations and BTI-induced degradations. The initial frequencies of ROs are assumed to be varied by the process variations according to the locations on the test chips. The groups of the highest, average and lowest frequencies are focused on. The aging degradations of the three groups are measured on the accelerated test. The degradation at the highest frequency group is larger than one at the slowest frequency group, because there should be the correlation between process variations and BTI-induced degradations.

This chapter is organized as follows. Section 3.2 and 3.3 show the measurement setups, the circuits, and the results on the FPGA and ASICs, respectively. Section 3.4 summarize this chapter.

3.2 Measurement of Process Variation and BTI on FPGA

This section introduces the measurement setup for the FPGA. The ROs are measured to analyze process variations and BTI-induced degradations.

3.2.1 Measurement Setup

The measurement setup is shown in Fig. 3.1. An engineering LSI tester is used to measure the circuits. A Cyclone IV FPGA contains 1,347 ROs which is fabricated in a 65-nm process. 837 ROs of them are measured. The details of the configurations are shown in the latter part. The cyclone FPGA is mounted on the DE0 NANO FPGA board which has 72 GPIO pins, a USB mini-AB port, two DC 5 V pins, and etc. The FPGA board and the DUT board on the tester are connected by the DSUB 50 pin cable. Power supply voltage is 1.2 V, which is limited by the specification of the FPGA board. Therefore, the voltage condition is not accelerated.

The temperature conditions are 80 °C. Numbers of oscillations are detected by on-chip counters. It is important to minimize the control signal delays when measuring BTI. Because the degradation amount is changing in very short time. To achieve accurate measurement results, the LSI tester is used. Frequencies of all ring oscillators are measured to analyze the process variations. BTI-induced degradations can be detected by measuring the frequencies of the ROs through the degradation time. The measurement time is 300 μs. When the oscillations stop, the ROs degrade over time. The frequencies of the ROs of the fast, typical and slow conditions are measured, periodically. The ROs repeat the degradation intervals and oscillations/measurements. The total degradation time is 5,000 s. It is enough longer than the total measurement time.

3.2.2 Measurement Circuit

The ROs and the on-chip counters are implemented on the the FPGA. The structure of the Cyclone IV FPGA is shown in Fig. 3.2. They consist of logic array blocks which can configure any logic circuits. Each logic array block has 16 logic elements which are the basic units of the FPGA. Fig. 3.3 shows the measurement circuit on the FPGA. It contains a ring oscillator (RO), a four-stage divider (DIVx4) and a 16-bit counter

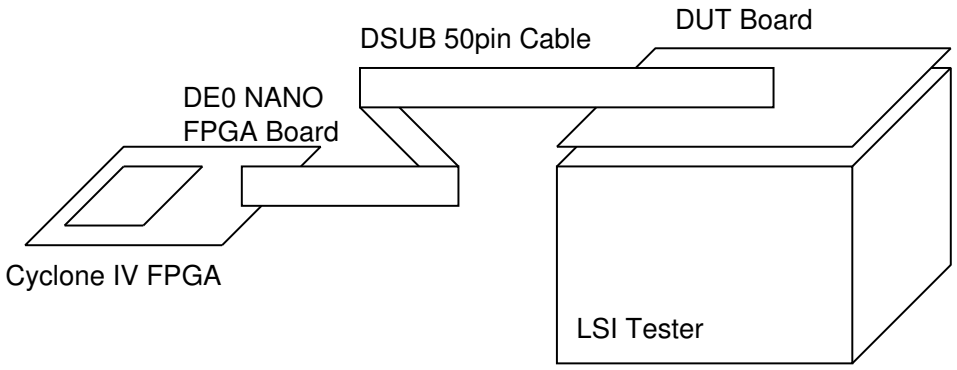

Figure 3.1: Measurement equipment.

(DIVx16).

The configurations of the test circuit are synthesized from the structured Verilog descriptions. To analyze the process variations, the configurations should cover whole logic array blocks of the FPGA. The circuit can be put in any location on the FPGA by using a corresponding configuration.

3.2.3 Results of Process Variation on FPGA

Fig. 3.4 shows the distributions of frequencies of the ROs on the FPGA. The frequencies follow the Gaussian distribution. The 1,347 ROs which have the configurations of each location are measured. But the automatic optimization of the design tool rewrites some configurations. Fig. 3.4 includes only the frequencies of the original configuration ROs. The 10 of the highest frequency group, the 10 of the average group, and the 10 of the lowest group are described as the “fast” condition, the “typical” condition, and the “slow” condition, respectively. Note that the descriptions of the variation conditions are different from that of ASICs.

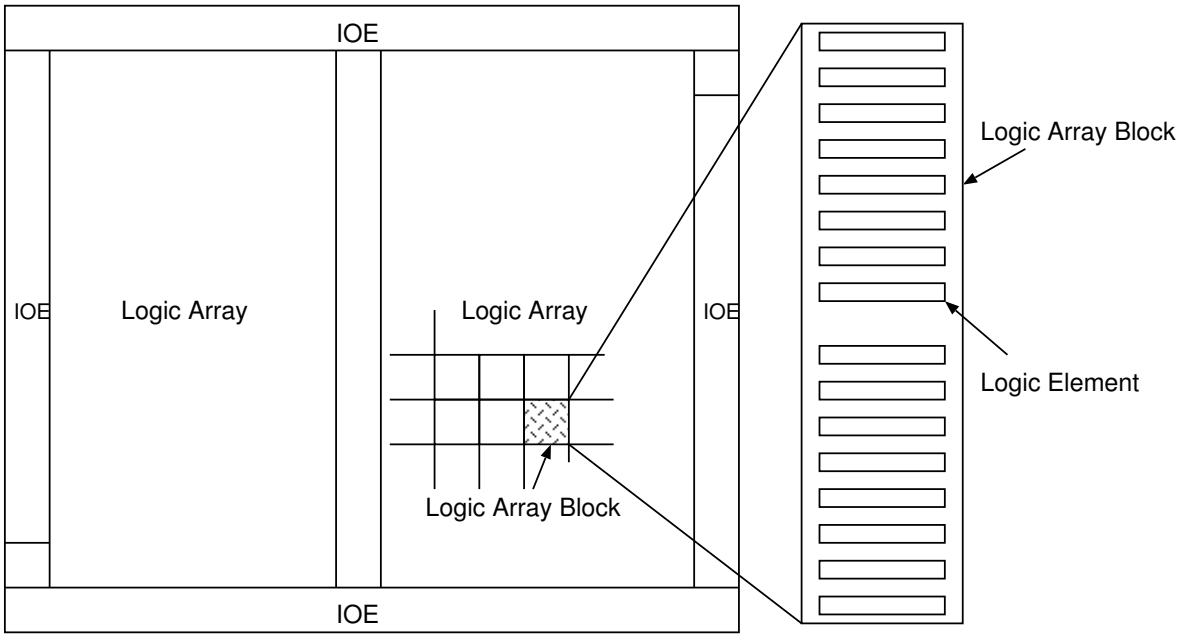

Figure 3.2: Structure of the Cyclone IV FPGA.

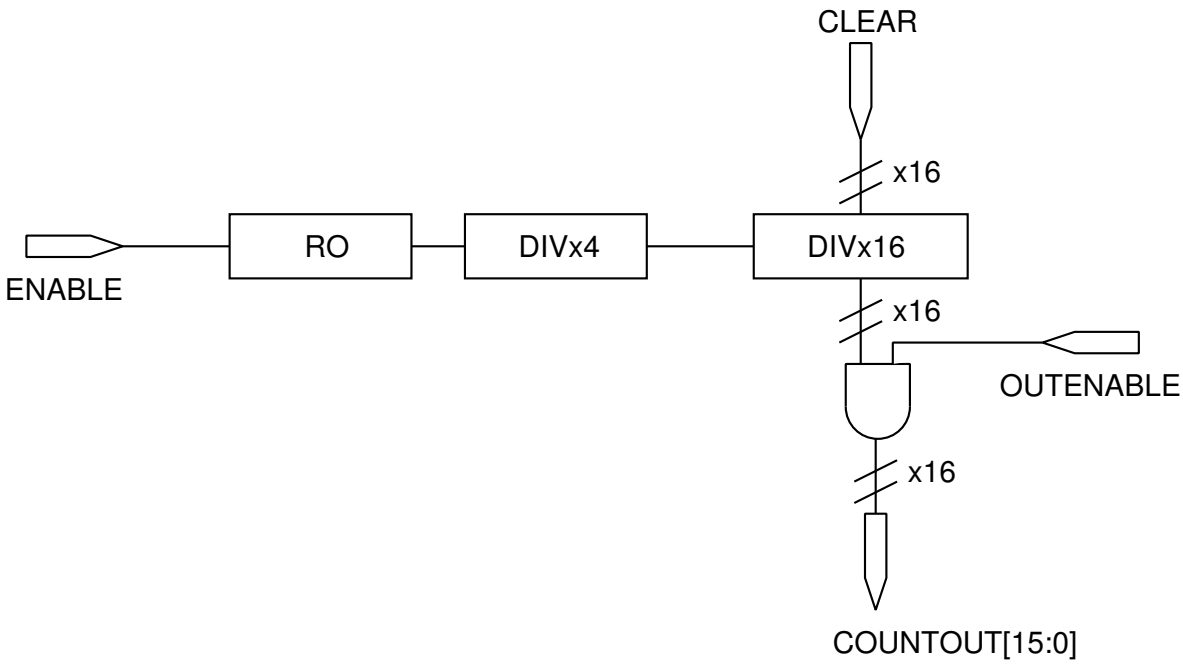

Figure 3.3: Measurement circuit consists of a RO and a 16-bit counter on the FPGA.

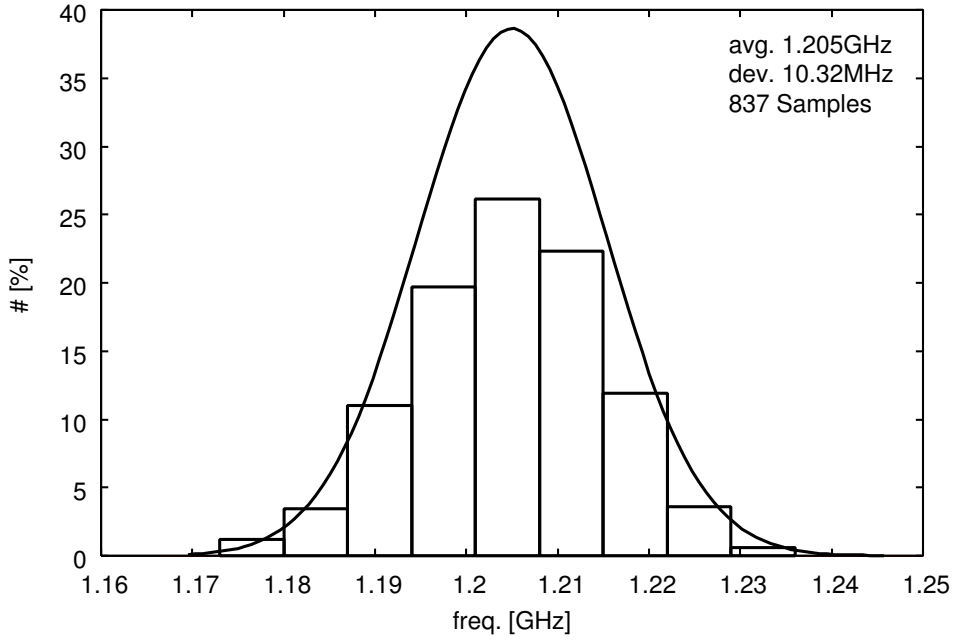

Figure 3.4: Frequency distribution of ROs on the FPGA, $V_{\mathrm{dd}} = 1.2\mathrm{V}$, $T = 80°\mathrm{C}$.

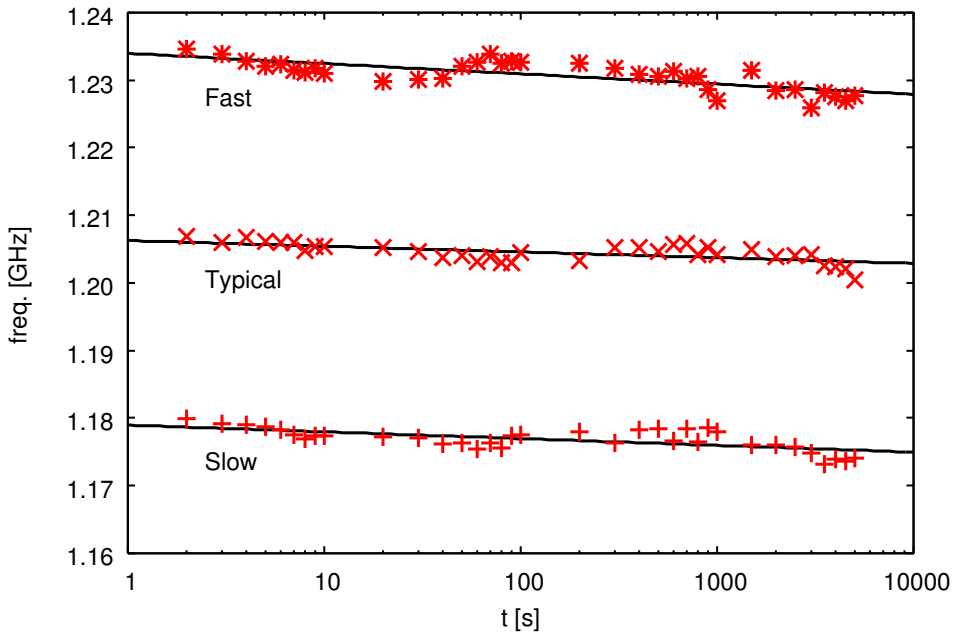

Figure 3.5: Frequency degradations of fast, typical and slow conditions on the FPGA, $V_{\mathrm{dd}} = 1.2\mathrm{V}$, $T = 80°\mathrm{C}$.

3.2.4 Results of BTI on FPGA

The degradations of frequencies of the three conditions on the FPGA are shown in Fig. 3.5. Note that the x axis is a log-scale. The frequencies are the frequency of single RO of three conditions. The degradations also follow logarithmic function which shown in Eq. (3.1).

$$f(t) = -a \times \log(t) + b \tag{3.1}$$

3.3 Measurement of Process Variation and BTI on ASIC

This section introduces the measurement setup for ASICs. The ROs are measured to analyze process variations and BTI-induced degradations.

3.3.1 Measurement Setup

The measurement setup is as follows. The engineering LSI tester is used to measure the circuits. A 65-nm process test chip contains 1,764 ROs. Those ROs are divided into 18 types. These 98 ROs have different structures such as stages and wiring capacitance/resistance. Therefore, the measurement results of ring oscillators of the same type are considered in the analysis. They are measured at the accelerated condition at which the power supply voltage is 2.0 V. Nominal power supply voltage is 1.2 V.

The temperature conditions are 80 °C. Numbers of oscillation are also detected by the on-chip counters.

3.3.2 Results of Process Variation on ASIC

Fig. 3.6 shows the distributions of frequencies of 98 ROs of the same type of the structure on the ASIC. The frequencies do not follow the Gaussian distribution. The reason is that the samples are 98. 10 samples (10%) of the highest frequency group, 10 samples (10%) of the average group, and 10 samples (10%) of the lowest group are described as the “fast” condition, the “typical” condition, and the “slow” condition.

3.3.3 Results of BTI on ASIC

The degradations of frequencies of the three conditions on the ASIC are shown in Fig. 3.7. Note that the x axis is a log-scale. The frequencies are averages of each variation condition. The degradations follow logarithmic function which shown in Eq. (3.1). The variable a is the degradation factor. The degradation trend is increased with a. The variable b is the frequency factor.

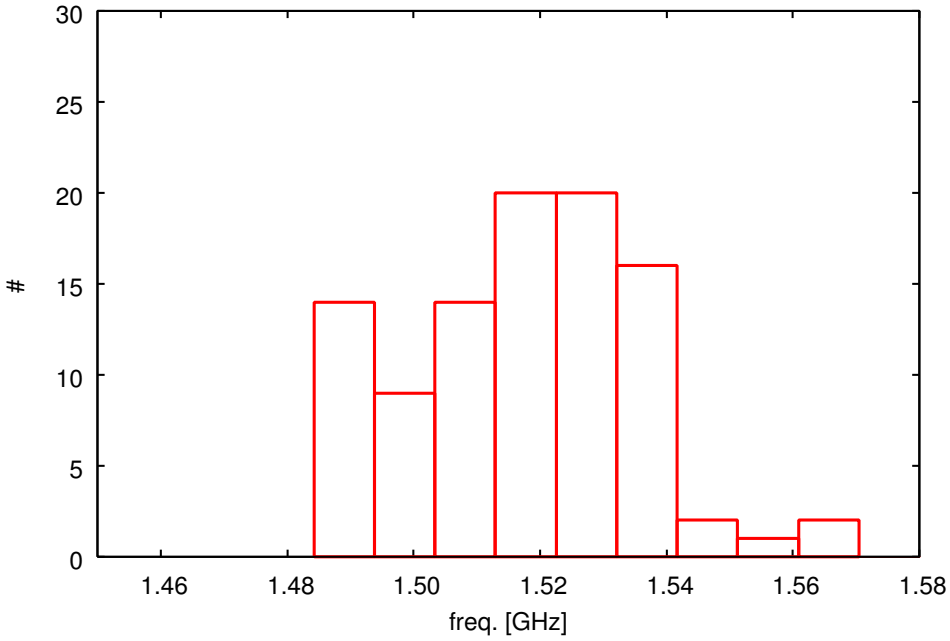

Figure 3.6: Frequency distribution of 98 ROs on the ASIC, $V_{\mathrm{dd}} = 2.0\mathrm{V}$, $T = 80°\mathrm{C}$.

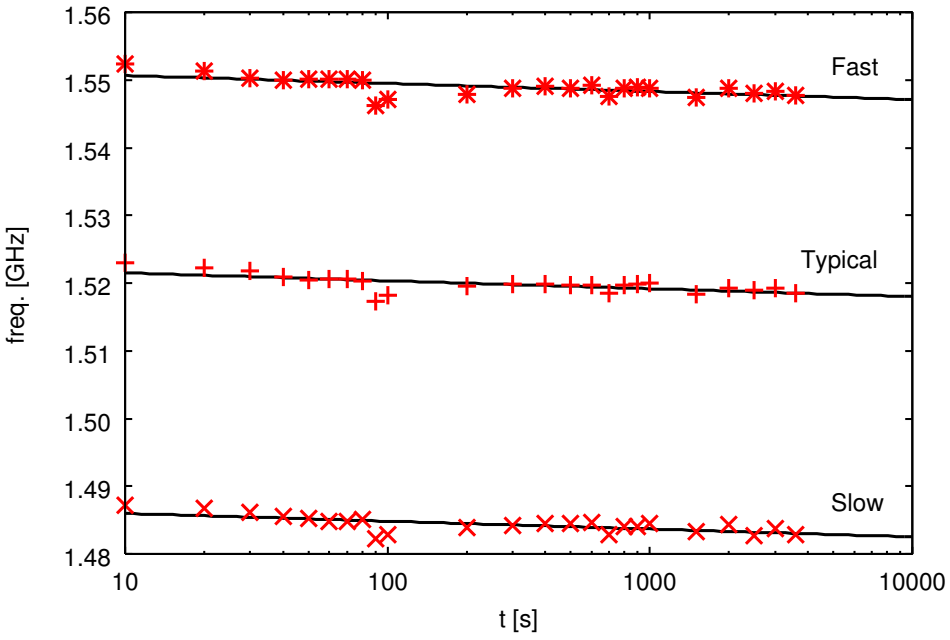

Figure 3.7: Frequency degradations of fast, typical and slow conditions on the ASIC, $V_{\mathrm{dd}} = 2.0\mathrm{V}$, $T = 80°\mathrm{C}$.

3.4 Summary

In this chapter, process variations and BTI-induced degradations are measured on the FPGA and ASICs. Those degradations are analyzed by the frequencies of the ROs. The measurement circuits consist of the ROs and counters (shift registers). The measurements of the BTI-induced degradations are accelerated by the temperature conditions.

The 1347 ROs configured in the logic elements are measured to analyze the process variations and BTI-induced degradations on the FPGA. The initial frequencies of the FPGA follow the Gaussian distribution. The frequencies of the FPGA decrease with time because of BTI-induced degradations. The degradations follow the logarithmic functions.

The process variations and BTI-induced degradations on the ASICs are measured. The initial frequencies of the ASICs are distributed from slow to fast conditions. The frequencies of the ASICs decrease with time because of BTI-induced degradations. The degradations follow the logarithmic functions.

According to the Atomistic Trap-Based Model, the prediction model of the BTI-induced degradations follows the logarithmic function. Therefore, the measurement results and the physical models are coincident.

Chapter 4

Design Methodology Considering Correlation between Process Variation and BTI-Induced Degradation

This chapter introduces the design methodology of ASICs and FPGAs considering the correlation between process variations and BTI-induced degradations. The measurement results that indicate the correlation are shown.

4.1 Outline

The design methodology considering process variations and BTI-induced degradations is proposed. In the conventional methodologies, the process variations are considered in the timing analysis. Delays are verified with the libraries of the worst case and calculated multiple times according to the libraries. BTI-induced degradations are considered as timing margins in the delay libraries. Those reliability issues are considered separately. However, the correlation between process variations and BTI-induced degradations is not considered in the conventional methodology. In the proposed methodology, the timing margins of BTI-induced degradations are configured by the conditions of the process variations. The different timing margins are applied to the timing analysis in the case of the fast, typical, and slow conditions. The accurate and efficient results of the timing analysis are achieved by the proposed methodology.

This chapter is organized as follows. Section 4.2 shows the correlation between

process variations and BTI-induced degradations. Section 4.3 shows the degradation-aware design methodology. Section 4.5 summarize this chapter.

4.2 Correlation between Process Variation and BTI-Induced Degradation

The correlation between process variations and BTI-induced degradations is examined in this section. To compare the trends of the degradations, the variables a of the degradation functions which shown in Eq. (3.1) are focused on. If a is larger, it means the degradation has a larger impact on BTI-induced degradations.

Fig. 4.1 shows a of the 98 ROs of the same type on the ASIC. The x axis is initial frequencies of the ROs. The correlation coefficient r of the frequencies f and a is calculated by Eq. (4.1).

$$r = \frac{\sum_{i=0}^{n}(f_i - \overline{f})(a_i - \overline{a})}{\sqrt{\sum_{i=0}^{n}(f_i - \overline{f})^2}\sqrt{\sum_{i=0}^{n}(a_i - \overline{a})^2}} = 0.338 \tag{4.1}$$

Variables $\overline{f}$ and $\overline{a}$ are averages of f and a respectively. The Pearson product-moment correlation coefficient is calculated by Eq. (4.1). The coefficient r is a real number (-1 to 1). If the absolute value of r come close 1, the correlation becomes larger. The relation between correlation coefficients and strengths of the correlation is shown in Table 4.1. In this case, $r = 0.338$ means the weak correlation. Degradation factors a show an increasing trend with the initial frequencies f.

The significance test of the correlation coefficient is required to confirm the correlation. The variable t which calculated by Eq. (4.2) and the probability p of the Student's t distribution are used for the test.

$$t = \frac{|r|\sqrt{n-2}}{\sqrt{1-r^2}} \tag{4.2}$$

Eq. (4.3) is the probability density function of the t distribution.

$$f(t) = \frac{\Gamma(\frac{\nu+1}{2})}{\sqrt{\nu\pi}\Gamma(\frac{\nu}{2})}\left(1 + \frac{t^2}{\nu}\right)^{-(\frac{\nu+1}{2})} = 0.0646 \tag{4.3}$$

Where, Γ is a gamma function and $\nu = n - 1$ is a degree of freedom. In the case of $n = 98$ and $r = 0.338$, the calculation result is $p = f(t) = 6.46\%$. It means the result achieves statistical significance of 10% of level of significance.

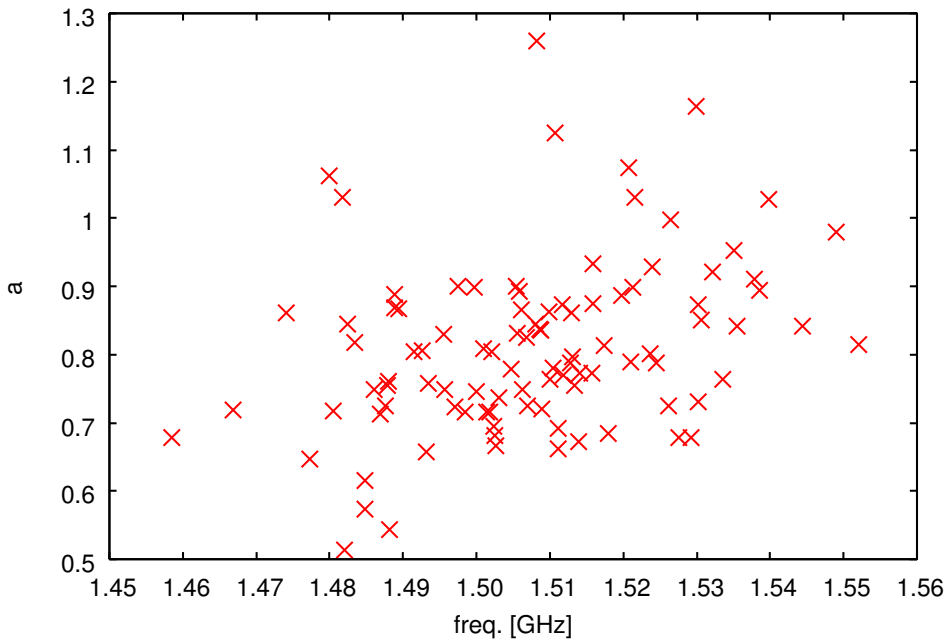

Figure 4.1: Variable a of same type ROs on the ASIC.

Table 4.1: Relation between correlation coefficient and strength of correlation.

correlation coefficient	strength of correlation
0.7 >	strong
0.4-0.7	medium
0.2-0.4	weak
0.2 <	not correlated

Figs. 4.2-4.4 show the degradations of the frequencies of the fast, typical and slow conditions on the FPGA respectively. They are the averages of the variation conditions. The variables a and b are shown in Table 4.2. It shows that a of the fast condition is the largest of all conditions.

Those results show there is the correlation between process variations and BTI-induced degradations.

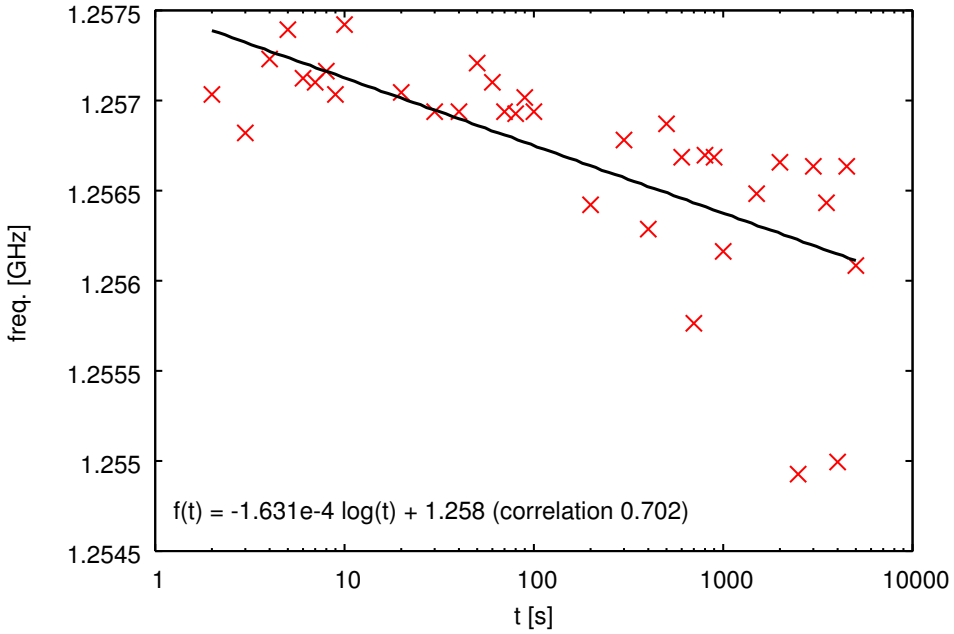

Figure 4.2: Frequency degradation of the average of the fast condition on the FPGA.

Table 4.2: Variable a and b of three conditions on the FPGA.

	fast	typical	slow
a	16.31×10^{-5}	9.873×10^{-5}	5.267×10^{-5}
b	1.258	1.211	1.175

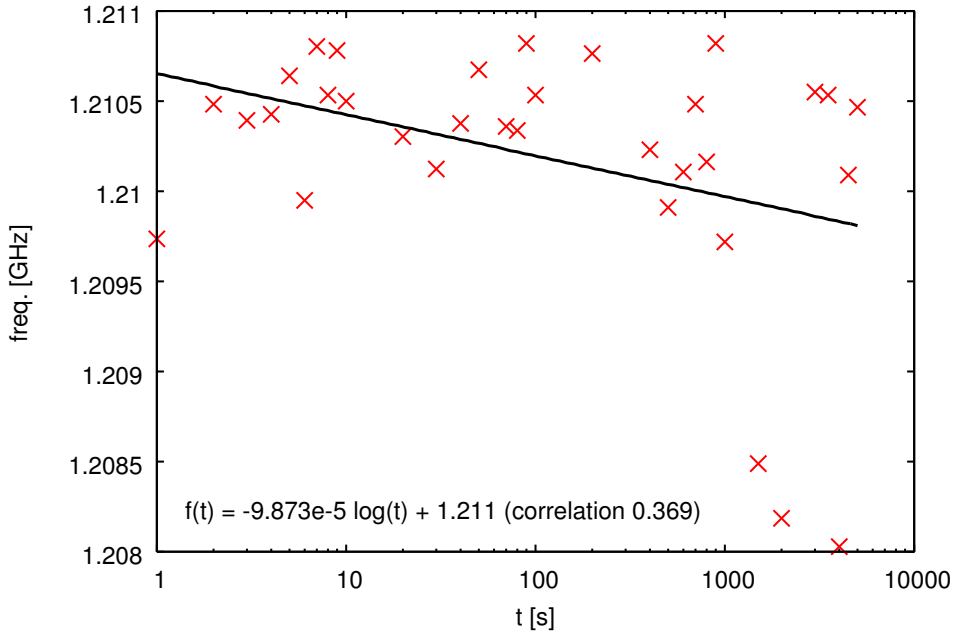

Figure 4.3: Frequency degradation of the average of the typical condition on the FPGA.

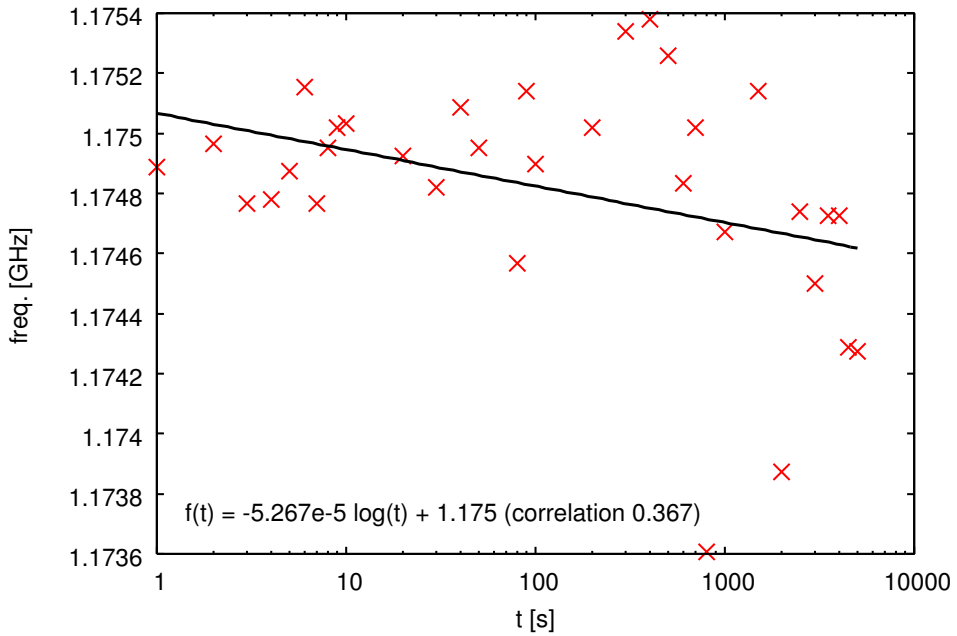

Figure 4.4: Frequency degradation of the average of the slow condition on the FPGA.

4.3 Degradation-Aware Design Methodology

The design methodology considering process variations and BTI-induced degradations is proposed in Fig. 4.5. In the proposed methodology, the timing margins of BTI-induced degradations in Delay Library are configured by the three conditions of the process variations, fast, typical, and slow. The appropriate timing margins are applied to Timing Analysis in the case of the three variation conditions.

Fig. 4.6 shows the timing margins considering the correlation between the reliability issues. The BTI-induced degradation at the fast condition has a significant effect. The timing margin of the fast condition is the largest among the three variation conditions. The timing margin of the slow condition is the smallest because the degradation at the slow condition is not significant. In this case, the timing margins for BTI-induced degradations can be reduced because the degradation at the slow condition is smaller than the others.

BTI-induced degradations have discrete characteristics because of the mechanism of trapping/detrapping carriers. The discussion based on the average of the degradations can not cover the worst case. The degradations are estimated corresponding to the variation conditions in the proposed methodology. If threshold voltage shifts of the degradations are larger than those of process variations, the worst values have been chosen and not the average. Nevertheless, the effect of the variations are 3 times larger than that of the degradations in 65 nm process. It is enough to discuss based on the average.

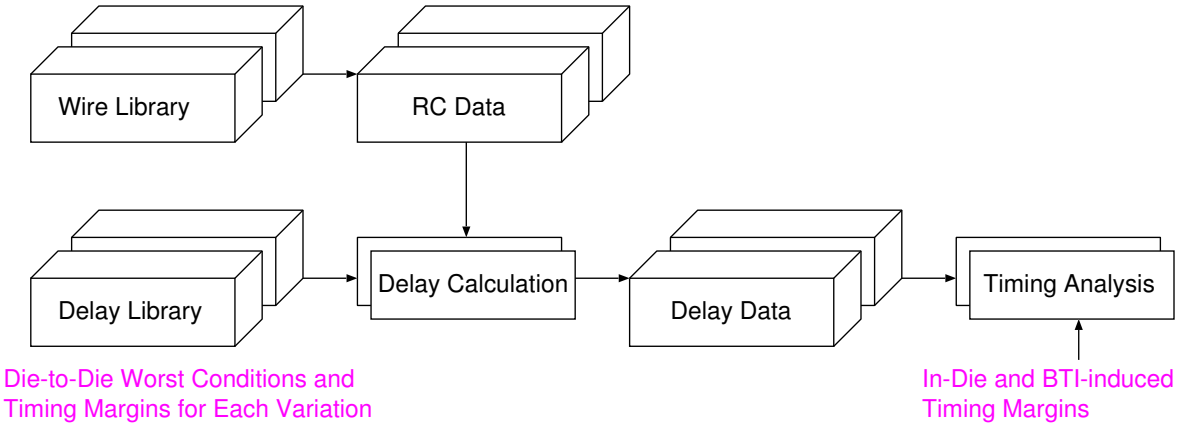

Figure 4.5: Timing analysis considering correlation between process variation and BTI-induced degradation.

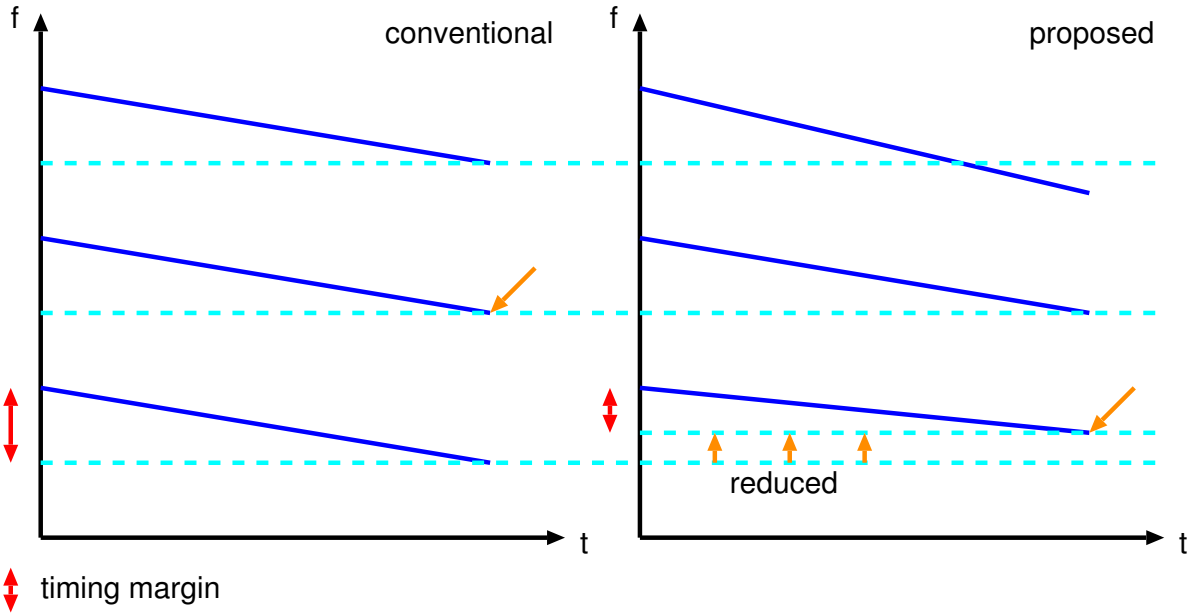

Figure 4.6: Timing margin considering correlation.

4.4 Degradation Prediction with Proposed Design Methodology

The degradation predictions of both the proposed and the conventional methodologies are analyzed with circuit simulations.

4.4.1 Prediction of Frequency Degradation of Ring Oscillator

The BTI-induced degradations of frequencies of ring oscillators with the proposed methodology are predicted. If the predictions of frequency degradations with the proposed methodology are smaller than those of conventional methodologies, timing margins of whole circuit are reduced.

The degradation predictions with the proposed methodology are introduced. Fig. 4.7 shows the distribution of measurement data which introduced in Sec. 3.3 and its approximate function with the least-square approach. The function is shown in Eq. (4.4).

$$a = g(f) = 2.31f - 2.66 \tag{4.4}$$

The initial frequencies f follow the Gaussian distribution of $\mu = 1.51$ GHz, $\sigma = 18.4$ MHz ($\sigma/\mu = 1.22\%$). Because the degradation factors a and the initial frequencies f are correlated, a of each variation condition is achieved by substitution of f of the fast, typical, or slow condition. The frequency degradations are predicted by Eq. (3.1) with a of each variation condition. Degradation factors a of all variation conditions are same in conventional methodologies.

The predictions with conventional and the proposed methodologies are shown in Table 4.3. Table 4.3 shows f, a, and the degradation ratios of frequency after 10^8 s Δf of the conditions of $\pm 3\sigma$. Where, $\Delta f = (f - f_{\mathrm{t}=10^8})/f \times 100$. In the proposed methodology, the degradation factors a of $\pm 3\sigma$ increase and decrease 15.4% from the typical condition, Δf becomes larger in the fast condition and smaller in the slow condition. In the conventional methodology, the degradations are predicted small in the fast condition and large in the slow condition. In this case, the reliability is threatened and excess timing margins are required. The predictions of the slow condition are reduced in the proposed methodology according to nature of the correlation. Therefore, the timing margins are reduced in the proposed methodology.

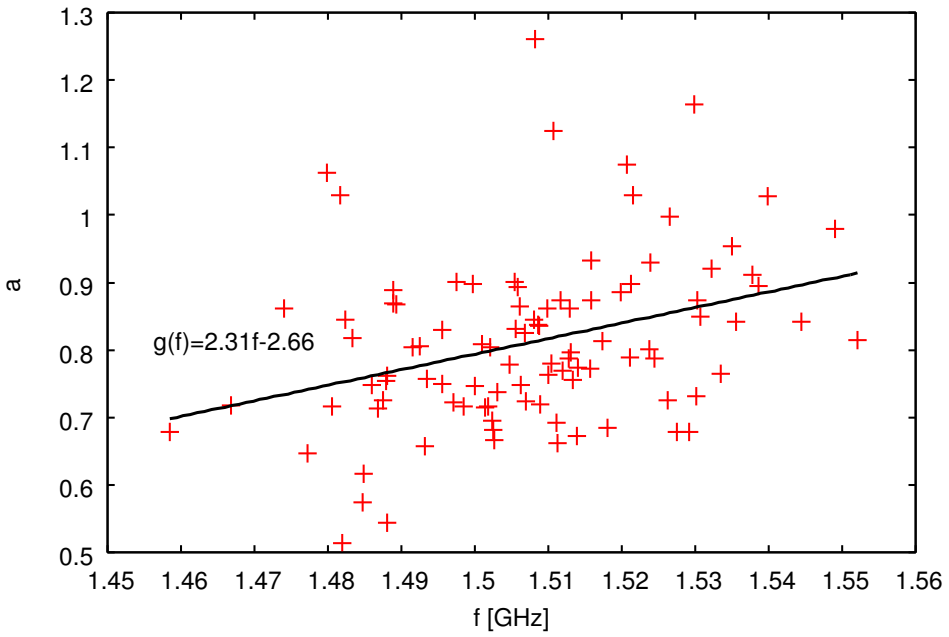

Figure 4.7: Distribution of degradation factors and initial frequencies, its approximate function of the least-square approach.

4.4.2 Degradation Analysis of Frequency of Ring Oscillator

The degradation analysis with the BTI-aware netlist are shown and conventional methodologies and the proposed methodology are compared. The simulation circuits are as same as the circuits in Sec. 2.3.2. Simulation conditions are as follows: the process node is a 65 nm bulk process, the supply voltage is 1.2 V, and the temperature is 80°C. Device parameters of the fast, typical, slow conditions are provided by the library. BTI-aware netlists are used in this simulation[52]. Degradations of threshold voltage are calculated by the AT-B Model. The degradation time is 10 years (3.1536×10^8 s). Degradation ratios of threshold voltage of PMOS are assumed 10% after 10 years of each variation condition. Note that the correlation is not considered in this setup.

Fig. 4.8 and Fig. 4.9 show the simulation results. Fig. 4.8 is the results of fast, typical, and slow conditions of 17-stage RO. Fig. 4.9 is the results of fast, typical, and slow conditions of 4-stage MUX. All results of frequency degradations follow the logarithmic function which shown in Eq. (3.1). Results a and $\Delta f = (f - f_{\mathrm{t=10y}})/f \times 100$ are summarized in Table 4.4. The degradation ratios Δf are different among each variation condition.

Table 4.3: Degradation factors a and predictions of frequency degradation ratios after 10^8 s Δf of $\pm 3\sigma$ with conventional (conv.) and proposed (prop.) methodologies.

			conv.		prop.	
cond.	σ	f [GHz]	a	Δf [%]	a	Δf [%]
fast	+3	1.57	0.828	0.971	0.956	1.12
	+2	1.55		0.984	0.913	1.09
	+1	1.53		0.997	0.871	1.05
typ.	±0	1.51		1.01	0.828	1.01
slow	−1	1.49		1.024	0.786	0.970
	−2	1.47		1.038	0.743	0.929
	−3	1.45		1.052	0.701	0.887

Table 4.4: Summary of results of simulation analysis of frequency degradations of 17-stage RO and 4-stage MUX with conventional methodology.

	17RO		4MUX	
condition	a	Δf [%]	a	Δf [%]
fast	1.21×10^{-3}	3.04	4.71×10^{-3}	3.62
typical	1.21×10^{-3}	4.20	3.22×10^{-3}	3.91
slow	1.04×10^{-3}	5.33	3.22×10^{-3}	5.79

Degradation predictions of the frequencies Δf with a calculated by the proposed methodology are shown in Table 4.5. Those results are considered the correlation as follows: Degradation factors a of $\pm 3\sigma$ increase and decrease 15.4% from that of the typical condition. The frequencies $f_{\mathrm{t=10y}}$ are calculated by Eq. (3.1) with those a.

In comparison with the results of Table 4.4, the degradation predictions of the slow condition are smaller in Table 4.5. In particular, 10% reduction is shown in the result of 4-stage MUX. Therefore, the timing margins of slow condition are reduced by the proposed methodology.

4.4.3 Degradation Analysis of Setup/Hold Time of Flip Flop

Setup/hold time of the flip flop (FF) are analyzed by the circuit simulations. The simulation circuit is shown in Fig. 4.10. Fig. 4.11 shows the operation check of the circuit under the condition that the clock signal (CLK) and the input signal (IN) are 1 GHz and 500 MHz respectively. The simulation conditions are as follows: the process

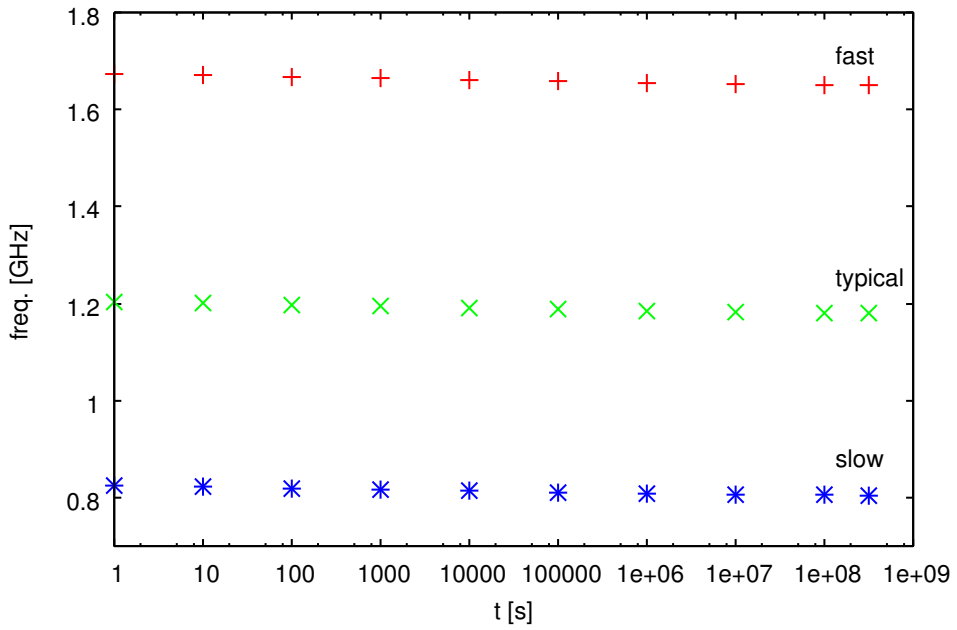

Figure 4.8: Results of simulation analysis of frequency degradations of 17-stage RO of each variation condition.

Table 4.5: Summary of degradation predictions of frequency of 17-stage RO and 4-stage MUX with proposed methodology.

	17RO		4MUX	
condition	a	Δf [%]	a	Δf [%]
fast	1.40×10^{-3}	3.55	3.72×10^{-3}	3.35
typical	1.21×10^{-3}	4.20	3.22×10^{-3}	3.91
slow	1.02×10^{-3}	5.29	2.72×10^{-3}	5.32

node is a 65 nm bulk process, the supply voltage is 1.2 V, and the temperature is 25 °C. IN and CLK are connected to the circuit through the inverters (INV). The output signal (OUT) is connected to the output load, fanout 4 INV. The setup/hold time are analyzed by measure time analysis which triggered by 0.6 V of IN and CLK. Setup/hold times are the minimum time requirements of stabilizations of the input signals for the forward/backward of the transitions of clock signals respectively.

IN are sweeped by 1 ps to analyze the setup time. CLK is 1 GHz. If the OUT malfunctions, it means the setup time failure. OUT malfunctions when setup times are 37 ps and 33 ps of rise and fall of IN on the typical condition. The results of setup

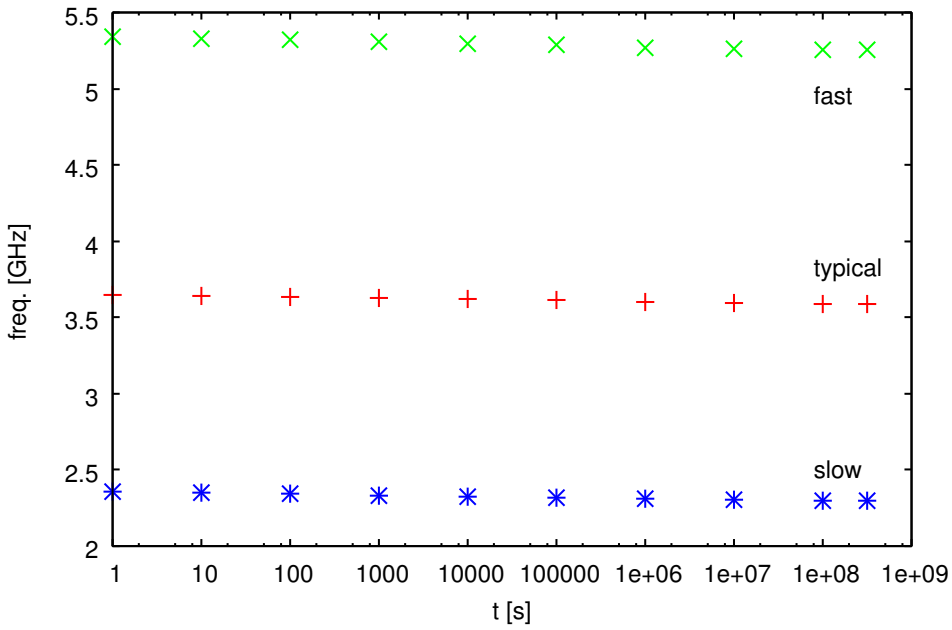

Figure 4.9: Results of simulation analysis of frequency degradations of 4-stage MUX of each variation condition.

time analysis of fast, typical, and slow conditions are summarized in Table 4.6. Setup times of fall of IN are shorter than those of rise. Hereafter, setup times of rise of IN are focused because setup times are defined by the minimum requirements. The setup time of fast condition is shorter than the other conditions.

Fig. 4.12 shows the short pulse of IN to analyze the hold time. The pulse rises at no violation timing for setup and falls after the transition of CLK. The pulse width are shorten by 1 ps until OUT malfunctions. The simulation circuit operates normally in fast, typical, and slow conditions, if the pulse falls within 1 ps of the transition of CLK. The pulse shown in Fig. 4.13 is analyzed, there are no malfunction of OUT. Therefore, hold times of all variation conditions are less than 1 ps.

BTI-induced degradations of setup/hold time are analyzed by circuit simulations with the BTI-aware netlist. Simulation conditions other than the degradations are the same as simulation described above. Threshold voltages of all PMOS transistors are increased 10% as the BTI-induced degradations.

The results of setup time analysis are 29 ps, 40 ps, and 58 ps on the fast, typical, and slow condition respectively. The setup times become longer than the initial conditions.

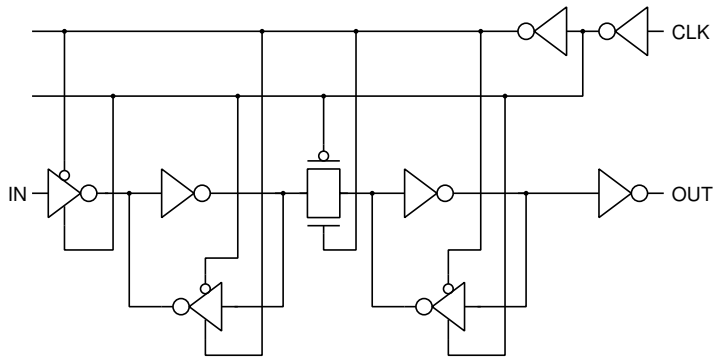

Figure 4.10: Simulation circuit, flip flop.

Table 4.6: Simulation result of setup time of rise/fall of IN signal.

condition	rise [ps]	fall [ps]
fast	28	25
typical	37	33
slow	55	47

The results of hold time analysis are less than 1 ps on all variation conditions. Those results mean that the restrictions of setup/hold time do not become strict if the circuits are degraded by BTI effects.

It is important for circuit designers to observe the setup time restriction of fast condition. The proposed methodology evaluates the statistics of the circuits as same as the conventional methodologies.

4.5 Summary

In this chapter, the correlation between BTI-induced degradations and process variations is analyzed with the measurement results.

The correlation coefficient of the degradation factors and the initial frequencies is 0.338 on the ASICs. It achieves the statistical significance of 10% of level of significance. The degradation factor at the fast condition is the largest among all conditions on the FPGA. They suggest that the BTI-induced degradation at the fast condition has a significant effect. In this case, the timing margins for BTI-induced degradations are reduced because the degradation at the slow condition is smaller. The design methodologies

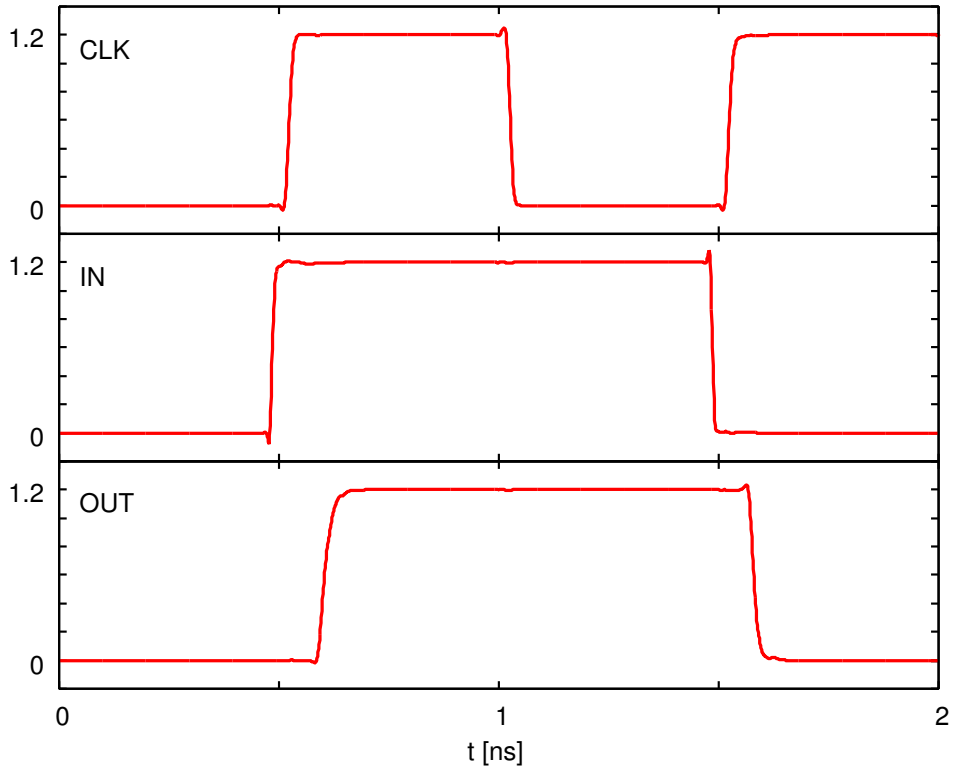

Figure 4.11: Operation check for simulated flip flop, CLK 1 GHz.

considering the correlation between process variations and BTI-induced degradations is proposed. In the proposed methodology, the timing margins are configured by the conditions of the process variations.

The degradation predictions with the proposed methodology are analyzed. The degradations of frequencies of the ROs are reduced by 10% with the predictions. The degradation predictions of setup times of the FFs are the same between the proposed and the conventional methodologies. Therefore, the reliability of the circuit is clearly not threatening with the proposed methodology.

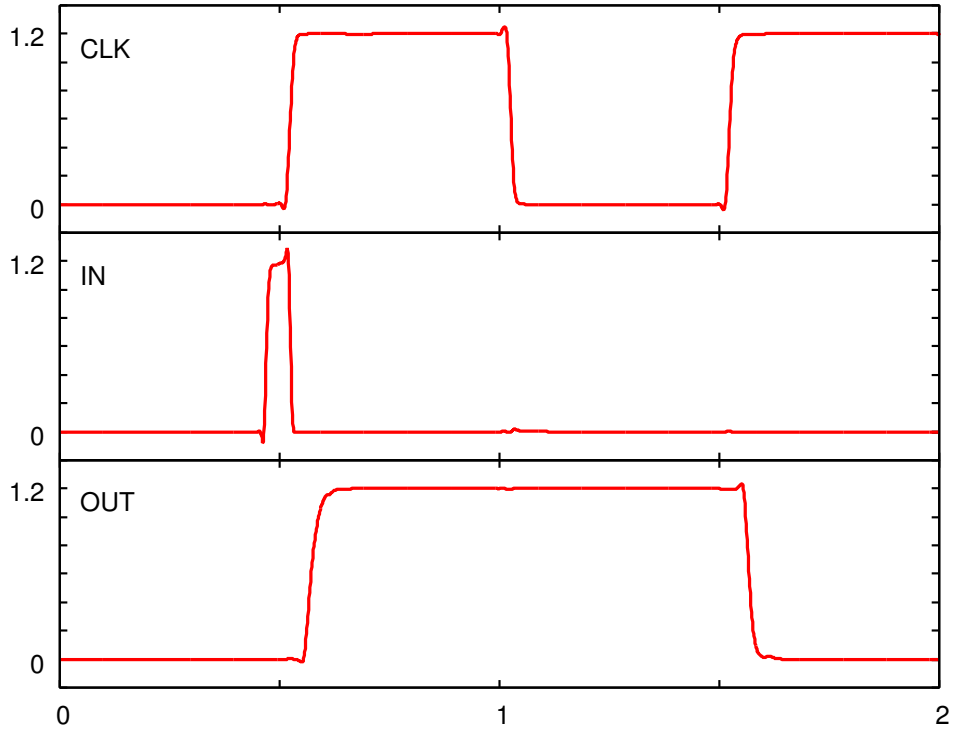

Figure 4.12: Hold time analysis of fall of IN signal.

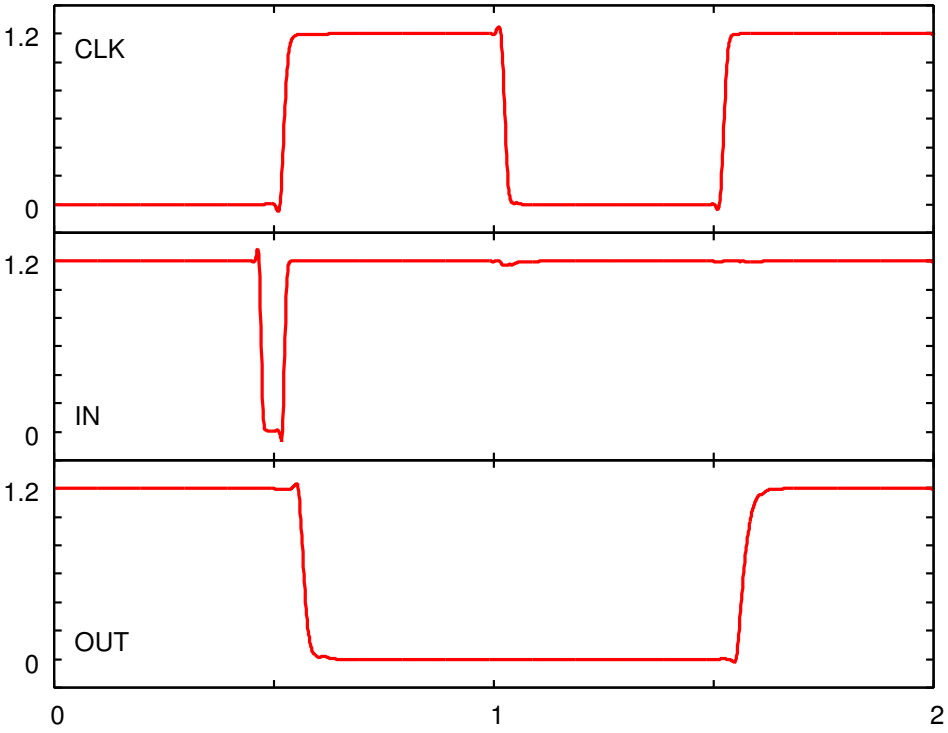

Figure 4.13: Hold time analysis of rise of IN signal.

Chapter 5

Conclusion

In this study, the design methodology considering the correlation between process variations and BTI-induced degradations is proposed.

Chapter 2 introduces the circuit simulation methodologies of BTI-induced degradations and their results. The analytical models of the BTI-induced degradations are introduced. The physical origin of the R-D model is the interface traps between the gate oxide and the channel. Threshold voltage shifts follow the power-law of the degradation time. The physical origin of the AT-B model is the oxide trap. Threshold voltage shifts follow the logarithmic function of the degradation time. The BTI-aware simulation methodology is introduced. The BTI-aware netlists which consider the threshold voltage shifts of BTI-induced degradations are used. The accurate predictions of BTI-induced degradations are achieved by simulations using the BTI-aware netlists. The NBTI and PBTI-induced delay degradations on CMOS inverters are analyzed. The rise time delay or the fall time delay increase 15 % after 10 years in the case that duty factor is 1. If the input signal is often low, NBTI becomes dominant on the delay degradation. If it is often high, PBTI becomes dominant on the delay degradation. The average of delay time degradations is almost constant except in the condition that the input signal is always high or low. In the condition, the delay degradation is smaller. The NBTI-induced frequency degradations on ring oscillators are analyzed. The frequency degradations follow a logarithmic function. Because the V_{th} shifts of BTI-induced degradations follow the model of the logarithmic function. The NBTI-induced delay degradations on FPGA routing paths are analyzed. In the case of an independent routing switch, the rise delay time increases by 3.46 % and the fall delay time decreases by 3.36 % on the

10 years degradation at 100 °C. Threshold voltage degradation on the pull-up PMOS (level restorer/half latch) is the main cause of the NBTI-induced delay degradation.

In chapter 3, process variations and BTI-induced degradations are measured on the FPGA and ASICs. Those degradations are analyzed by the frequencies of the ROs. The measurement circuits consist of the ROs and counters (shift registers). The measurements of the BTI-induced degradations are accelerated by the temperature conditions. The 1347 ROs configured in the logic elements are measured to analyze the process variations and BTI-induced degradations on the FPGA. The initial frequencies of the FPGA follow the Gaussian distribution. The frequencies of the FPGA decrease with time because of BTI-induced degradations. The degradations follow the logarithmic functions. The process variations and BTI-induced degradations on the ASICs are measured. The initial frequencies of the ASICs are distributed from slow to fast conditions. The frequencies of the ASICs decrease with time because of BTI-induced degradations. The degradations follow the logarithmic functions. According to the Atomistic Trap-Based Model, the prediction model of the BTI-induced degradations follows the logarithmic function. Therefore, the measurement results and the physical models are coincident.

In chapter 4, the correlation between BTI-induced degradations and process variations is analyzed with the measurement results. The correlation coefficient of the degradation factors and the initial frequencies is 0.338 on the ASICs. It achieves the statistical significance of 10% of level of significance. The degradation factor at the fast condition is the largest among all conditions on the FPGA. They suggest that the BTI-induced degradation at the fast condition has a significant effect. In this case, the timing margins for BTI-induced degradations are reduced because the degradation at the slow condition is smaller. The design methodologies considering the correlation between process variations and BTI-induced degradations is proposed. In the proposed methodology, the timing margins are configured by the conditions of the process variations. The degradation predictions with the proposed methodology are analyzed. The degradations of frequencies of the ROs are reduced by 10% with the predictions. The degradation predictions of setup times of the FFs are the same between the proposed and the conventional methodologies. Therefore, the reliability of the circuit is clearly not threatening with the proposed methodology.

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Bibliography

[1] S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation", *IEEE Micro*, Vol. 25, No. 6, pp. 10–16, (2005).

[2] Hidetoshi Onodera, "Variability modeling and impact on design", *IEEE IEDM*, (2008), pp. 1–4.

[3] M.A. Alam, K. Roy, and C. Augustine, "Reliability- and Process-variation aware design of integrated circuits - A broader perspective", *IEEE IRPS*, (2011), pp. 4A.1.1–4A.1.11.

[4] G.F. Taylor, "Where are we going? Product scaling in the system on chip era", *IEEE IEDM*, (2013), pp. 17.1.1–17.1.3.

[5] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, and Y. Cao, "The Impact of NBTI Effect on Combinational Circuit: Modeling, Simulation, and Analysis", *IEEE Trans. on VLSI Systems*, Vol. 18, No. 2, pp. 173–183, (2010).

[6] M. Alam, "A critical examination of the mechanics of dynamic NBTI for PMOSFETs", *IEEE IEDM*, pp. 14.4.1–14.4.4, (2003).

[7] K. Zhao, J.H. Stathis, B.P. Linder, E. Cartier, and A. Kerber, "PBTI under dynamic stress: From a single defect point of view", *IEEE IRPS*, (2011), pp. 4A.3.1–4A.3.9.

[8] Tibor Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities", *Microelectronics Reliability*, Vol. 52, No. 1, pp. 39–70, (2012).

[9] Kyosuke Ito, Takashi Matsumoto, Shinichi Nishizawa, Hiroki Sunagawa, Kazutoshi Kobayashi, and Hidetoshi Onodera, "Modeling of Random Telegraph Noise under Circuit Operation - Simulation and Measurement of RTN-induced delay fluctuation", *ISQED*, (2011), pp. 22–27.

[10] T. Matsumoto, K. Kobayashi, and H. Onodera, "Impact of random telegraph noise on CMOS logic circuit reliability", *IEEE CICC*, (2014), pp. 1–8.

[11] Jeffrey Hicks, Daniel Bergstrom, Mike Hattendorf, Jason Jopling, Jose Maiz, Sangwoo Pae, Chetan Prasad, and Jami Wiedemer, "45nm Transistor Reliability.", *Intel Technology Journal*, Vol. 12, No. 2, (2008).

[12] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the Surface-State Charge (Q) of Thermally Oxidized Silicon", *Journal of the Electrochemical Society*, Vol. 114, p. 266, (1967).

[13] C. Shen, M.-F. Li, C. E. Foo, T. Yang, D. M. Huang, A. Yap, G. S. Samudra, and Y.-C. Yeo, "Characterization and Physical Origin of Fast Vth Transient in NBTI of pMOSFETs with SiON Dielectric", *IEEE IEDM.*, (2006), pp. 1–4.

[14] V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, and C. Ouvrard, "New characterization and modeling approach for NBTI degradation from transistor to product level", *IEEE IEDM.*, (2007), pp. 797–800.

[15] B. Kaczer, T. Grasser, J. Martin-Martinez, E. Simoen, M. Aoulaiche, P.J. Roussel, and G. Groeseneken, "NBTI from the perspective of defect states with widely distributed time scales", *IEEE IRPS.*, (2009), pp. 55–60.

[16] H. Reisinger, T. Grasser, W. Gustin, and C. Schlunder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress", *IEEE IRPS.*, (2010), pp. 7 – 15.

[17] B. Kaczer, S. Mahato, V. Valduga de Almeida Camargo, M. Toledano-Luque, Ph. J. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, and G. Groeseneken, "Atomistic approach to variability of bias-temperature instability in circuit simulation", *IEEE IRPS*, (2011), pp. XT.3.1–XT.3.5.

[18] S. Deora, V.D. Maheta, and S. Mahapatra, "NBTI lifetime prediction in SiON p-MOSFETs by H/H2 Reaction-Diffusion(RD) and dispersive hole trapping model", *IEEE IRPS*, (2010), pp. 1105–1114.

[19] K. Sutaria, A. Ramkumar, Rongjun Zhu, R. Rajveev, Yao Ma, and Yu Cao, "BTI-induced aging under random stress waveforms: Modeling, simulation and silicon validation", *ACM/EDAC/IEEE DAC.*, (2014), pp. 1–6.

[20] W. Wang, S. Yang, S. Bhardwaj, R. Vattikonda, S. Vrudhula, F. Liu, and Y. Cao, "The impact of NBTI on the performance of combinational and sequential circuits", *DAC.*, ACM, (2007), pp. 364–369.

[21] K. Kang, K. Kim, A.E. Islam, M.A. Alam, and K. Roy, "Characterization and estimation of circuit reliability degradation under NBTI using on-line I DDQ measurement", *DAC.*, ACM, (2007), pp. 363–368.

[22] Hong Luo, Xiaoming Chen, Jyothi Velamala, Yu Wang, Yu Cao, Vikas Chandra, Yuchun Ma, and Huazhong Yang, "Circuit-level delay modeling considering both TDDB and NBTI", *ISQED*, (2011), pp. 14–21.

[23] B. Kaczer, C. Chen, P. Weckx, P.J. Roussel, M. Toledano-Luque, J. Franco, M. Cho, J. Watt, K. Chanda, G. Groeseneken, and T. Grasser, "Maximizing reliable performance of advanced CMOS circuits—A case study", *IEEE IRPS*, (2014), pp. 2D.4.1–2D.4.6.

[24] Yuji Kunitake, Toshinori Sato, and Hirota Yasuura, "Guideline Considering the NBTI degradation Locality for Mitigating the Degradation on Memory Circuits", *Review Paper*, pp. 1 – 10, (2010).

[25] Ik Joon Chang, Kunhyuk Kang, S. Mukhopadhyay, C.H. Kim, and K. Roy, "Fast and accurate estimation of nano-scaled SRAM read failure probability using critical point sampling", *IEEE CICC.*, pp. 439–442, (2005).

[26] A. Kerber and P. Srinivasan, "Impact of Stress Mode on Stochastic BTI in Scaled MG/HK CMOS Devices", *IEEE Electron Device Letters*, Vol. 35, No. 4, pp. 431–433, (2014).

[27] T. Tsunomura, A. Nishida, and T. Hiramoto, "Analysis of NMOS and PMOS Difference in VT Variation With Large-Scale DMA-TEG", *IEEE Trans. on Electron Devices*, Vol. 56, No. 9, pp. 2073–2080, (2009).

[28] K. Bernstein, D.J. Frank, A.E. Gattiker, W. Haensch, B.L. Ji, S.R. Nassif, E.J. Nowak, D.J. Pearson, and N.J. Rohrer, "High-performance CMOS variability in the 65-nm regime and beyond", *IBM Journal of Research and Development*, Vol. 50, No. 4.5, pp. 433–449, (2006).

[29] Asen Asenov and Khairulmizam Samsudin, "Variability in nanoscale UTB SOI devices and its impact on circuits and systems", *Nanoscaled Semiconductor-on-Insulator Structures and Devices*, Springer, (2007), pp. 259–302.

[30] Kelin Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Weikai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, and Keith Zawadzki, "Managing Process Variation in Intel's 45nm CMOS Technology.", *Intel Technology Journal*, Vol. 12, No. 2, (2008).

[31] S. M. Sze, *"Semiconductor Devices Physics and Technology"*, John Wiley and Sons, Inc., 2nd edition, (2002).

[32] T. Saito, "Chapter B7 Timing Analysis", *STARC 2010 LSI Design*, (2010).

[33] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer, "BTI reliability of 45 nm high-K + metal-gate process technology", *IEEE IRPS.*, (2008), pp. 352–357.

[34] K. Ramakrishnan, S. Suresh, N. Vijaykrishnan, and MJ Irwin, "Impact of NBTI on FPGAs", *VLSI Design.*, (2007), pp. 717–722.

[35] E. Stott and P. Y. K. Cheung, "Improving FPGA Reliability with Wear-Levelling", *ICFPL*, (2011), pp. 323–328.

[36] A. Amouri and M. Tahoori, "High-level aging estimation for FPGA-mapped designs", *ICFPL*, (2012), pp. 284–291.

[37] E. Stott, P. Sedcole, and P. Cheung, "Fault tolerant methods for reliability in FPGAs", *ICFPL.*, (2008), pp. 415–420.

[38] D. Angot, V. Huard, L. Rahhal, A. Cros, X. Federspiel, A. Bajolet, Y. Carminati, M. Saliva, E. Pion, F. Cacho, and A. Bravaix, "BTI variability fundamental understandings and impact on digital logic by the use of extensive dataset", *IEEE IEDM*, (2013), pp. 15.4.1–15.4.4.

[39] B. Kaczer, V. Arkbipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin, "Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification", *IEEE IRPS.*, (2005), pp. 381–387.

[40] M. Denais, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, A. Bravaix, V. Huard, and F. Perrier, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's", *IEEE IEDM.*, (2004), pp. 109–112.

[41] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast VT-Measurements", *IEEE IRPS.*, (2006), pp. 448–453.

[42] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive Modeling of the NBTI Effect for Reliable Design", *IEEE CICC.*, (2006), pp. 189–192.

[43] A.E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, and M.A. Alam, "On the differences between ultra-fast NBTI measurements and Reaction-Diffusion theory", *IEEE IEDM.*, pp. 1–4, (2009).

[44] M. Toledano-Luque, B. Kaczer, Ph.J. Roussel, T. Grasser, G.I. Wirth, J. Franco, C. Vrancken, N. Horiguchi, and G. Groeseneken, "Response of a single trap to AC negative Bias Temperature stress", *IEEE IRPS.*, (2011), pp. 4A.2.1–4A.2.8.

[45] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability", *IEEE IRPS.*, (2010), pp. 16–25.

[46] H. Miki, M. Yamaoka, N. Tega, Z. Ren, M. Kobayashi, C. P. D'Emis, Y. Zhu, D. J. Frank, M. A. Guillorn, D.-G. Park, W. Haensch, and K. Torii, "Understanding

short-term BTI behavior through comprehensive observation of gate-voltage dependence of RTN in highly scaled high-k/metal-gate pFETs", *VLSIT*, (2011), pp. 148–149.

[47] X. Xi, M. Dunga, J. He, W. Liu, K.M. Cao, X. Jin, J.J. Ou, M. Chan, A.M. Niknejad, and C. Hu, "BSIM4. 3.0 MOSFET Model User; s Manual", *University of California, Berkeley*, (2003).

[48] H. Quinn, G.R. Allen, G.M. Swift, Chen Wei Tseng, P.S. Graham, K.S. Morgan, and P. Ostler, "SEU-Susceptibility of Logical Constants in Xilinx FPGA Designs", *IEEE Trans. on Nuclear Science.*, Vol. 56, No. 6, pp. 3527–3533, (2009).

[49] Carl Carmichael, *"Triple Module Redundancy Design Techniques for Virtex FPGAs"*, Vol. 1.0.1, Xilinx, Inc., (2006).

[50] P. Graham, M. Caffrey, D.E. Johnson, N. Rollins, and M. Wirthlin, "SEU mitigation for half-latches in Xilinx Virtex FPGAs", *IEEE Trans. on Nuclear Science.*, Vol. 50, No. 6, pp. 2139–2146, (2003).

[51] Neil H.E Weste and David Harris, *"CMOS VLSI DESIGN A circuit and systems Perspective Third Edition"*, Addison Wesley, (2004).

[52] Michitarou Yabuuchi and Kobayashi Kazutoshi, "Circuit Characteristic Analysis Considering NBTI and PBTI-Induced Delay Degradation", *IEEE IMFEDK*, (2012), pp. 72–73.

Publication list

Journal Publications

[1] M. Yabuuchi, R. Kishida, and K. Kobayashi, "Correlations between BTI-Induced Degradations and Process Variations on ASICs and FPGAs," *IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences Special Section on VLSI Design and CAD Algorithms*, vol. E97-A, no. 12, Dec. 2014.

[2] M. Yabuuchi and K. Kobayashi, "NBTI-Induced Delay Degradation Analysis of FPGA Routing Structures," *IPSJ Transactions on System LSI Design Methodology*, vol. 5, pp. 143–149, Aug. 2012.

Proceedings

[1] M. Yabuuchi, R. Kishida, and K. Kobayashi, "Correlation between BTI-Induced Degradations and Process Variations by Measuring Frequency of ROs," in *IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK)*, 2014, pp. 128–129.

[2] M. Yabuuchi and K. Kobayashi, "Circuit characteristic analysis considering nbti and pbti-induced delay degradation," in *IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK)*, 2012, pp. 72–73.

[3] M. Yabuuchi and K. Kobayashi, "Evaluation of FPGA design guardband caused by inhomogeneous NBTI degradation considering process variations," in *International Conference on Field-Programmable Technology (FPT)*, 2010, pp. 417–420.

[4] M. Yabuuchi and K. Kobayashi, "Circuit Performance Degradation on FPGAs Considering NBTI and Process Variations," in *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, 2010, pp. 126–129.

Proceedings in Japanese

[1] M. Yabuuchi and K. Kobayashi, "Design Margin for BTI-Induced Degradation by Considering Process Variation," in *IEICE Engineering Sciences Society Conference*, 2014, pp. A–3–7.

[2] M. Yabuuchi, R. Kishida, A. Oshima, and K. Kobayashi, "Evaluation of Correlation Between BTI-Induced Degradation and Process Variation on Ring Oscillator," in *DA Symposium*, 2014, pp. 49–54.

[3] M. Yabuuchi and K. Kobayashi, "Prediction Model for Process Variation and BTI-Induced Degradation by Measurement Data on FPGA," in *IEICE Technical Report (VLSI Design Technologies)*, 2014, pp. 161–166.

[4] M. Yabuuchi and K. Kobayashi, "DF Characteristics Analysis of BTI-Induced Delay Degradation with Trap and De-Trap Model," in *DA Symposium*, 2012, pp. 145–150.

[5] M. Yabuuchi and K. Kobayashi, "Analytical Approach for NBTI-Induced Degradation with RTN Model," in *IEICE Engineering Sciences Society Conference*, 2011, pp. A–3–9.

[6] M. Yabuuchi and K. Kobayashi, "Analytical Approach for NBTI-Induced Delay with RTN Model on FPGA Routing Architecture," in *DA Symposium*, 2011, pp. 189–194.

[7] M. Yabuuchi and K. Kobayashi, "Circuit Performance Degradation on FPGAs Considering NBTI and Process Variations," in *DA Symposium*, 2010, pp. 135–140.