A Study to Evaluate and Project Soft Error Tolerance in Radiation-hardened Circuits Using Device and Physical Level Simulations

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Dec. 25 2015

Contents

Abstract

My thesis focuses on projection and evaluation for soft error tolerance in the radiation-hardened circuit by device and physics level simulations. The SERs of various circuit, layout and device structures are discussed. A high accurate Monte-Carlo based simulation methodology is also proposed in this thesis.

Firstly, the device and physical level simulations methodology for soft error are described in Chapter 2. In my thesis, the charge generation and collection mechanisms by direct ionization are simulated by TCAD simulator SENTAURUS, and the mechanisms by indirect ionization are simulated by Monte-Carlo based physical-level simulator PHITS. After that in Chapter 3, the parasitic bipolar effects are investigated to suppress MCUs on radiation-hardened dual-modular flip-flops in a 65-nm process. Device simulations reveal that a simultaneous flip of redundant latches is suppressed by storing opposite values instead of storing the same value due to its asymmetrical structure. Then, in Chapter 4, the contributions of layout structures to suppress MCU are analyzed by device-level simulations and neutron-beam tests. Device simulation and experimental results reveal that the ratio of MCU to SEU decreases by increasing the distance between 65-nm process redundant latches. MCU is suppressed effectively by increasing the density of well contacts. Furthermore, in Chapter 5, the SERs (Soft Error Rates) of FD-SOI processes depending on BOX (Buried OXide) regions and body bias are estimated by alpha, neutron-beam tests and a proposed Monte-Carlo based simulations. The simulated results are consistent with the alpha and neutron irradiation experimental results. Simulated results reveal that the SERs are decreased by increasing the thickness of BOX layer. By applying the reverse body bias the tolerance for soft error becomes stronger in SOTB while that in UTBB becomes weaker. Finally, Chapter 6 summarizes the contribution of my thesis.

Chapter 1

Introduction

It becomes importance to increase the reliability of very large scale integration (VLSI) circuits. Recently, in the deep submicron structures, the tolerance of VLSI circuits for noise has significantly decreased, because of theprocess scaling, lowering supply voltages, and high operating frequencies.Moreover, several new factors such as process variations and aging reduces VLSI ciruict reliabilities. Therefore, the design of high tolerant VLSI circuits has become very challenging. There are many types of noise in VLSI circuits, such as power and ground noise, capacitive coupling noise, single event effects (SEEs), etc.

As technology downscaling, The memory devices in VLSI circuits have become very sensitive to radiation particle hits[1, 2, 3, 4, 5, 6, 7]. Radiation particles can result in functional errors. Those are often referred to as soft errors. Almost 8% increase in soft error rate (SER) per logic gate bit for each technology downscaling[6, 7]. The number of logic gate bits on a chip doubles per technology downscaling. It makes VLSI became more sensitive to radiation particles. It is expected that the SERs in the 16-nm technology will be almost 100x of the SERs in the 180nm technology[6, 7]. It is necessary to improve the tolerance to radiations. Thus, mitigation and projection on the soft error tolerance in the scaled circuit and future structures such as SOI (silicon on insulator) become much more important.

This chapter describe the background of SEEs and objectives of this thesis. This thesis focuses on the projection of tolerance for soft error in radiation-hardened circuits by device and physics level simulations. Firstly, the background and history of SEEs will be described in Sect. 1.1. Secondly, the mechanisms of charge generation and charge

collection will be explained in Sect. 1.2. After that, the main cause of MCU are explained in Sect. 1.4. Finally, the objective of this thesis is presented in Sect. 1.5.

1.1 Single Event Effect

SEEs are caused when radiation particles such as protons, neutrons, alpha particles, or heavy ions hit sensitive areas in semiconductor. These radiation particles hits can deposit charge, resulting in a voltage pulse or glitch at the output of sensitive areas. The radiation-induced pulse cause a soft error.

Radiation particles are very problematic for memories (latches, SRAMs, and DRAMs) since they can directly flip the stored state of a memory element, causing a single event upset (SEU)[1, 2]. Although radiation-induced errors in sequential elements will continue to be problematic for high performance microprocessors, it is expected that soft errors in combinational logic will dominate in future technologies[4, 8, 9]. Radiation particle hits on combinational circuits are referred to as single event transients (SETs). An SET pulse due to a radiation particle hits can propagate to a storage cell such as a Flip-flop (FF), which can result in an incorrect value, hence resulting in single bit upsets (SEU).

There are three masking factors decide whether an incorrect value by a radiation particle hit propagates to the outputs of combinational circuits and results in failures. These masking factors are as follows[4, 9]:

Electrical masking occurs when a SET pulse at a circuit node induced by a radiation particle hit weaken as it propagates through the circuit to the output nodes. Electrical masking can reduce the SET to a value which cannot cause any soft errors.

Logical masking occurs when there is no functionally sensitized path from the node in the circuit where a radiation particle hits, to any output node. Logical masking properties of a logic gate can be estimated using logic information alone.

Temporal masking occurs if a SET pluse reaches the outputs of a circuit besides the latching window of the sequential elements of the circuit. Temporal masking only depends on the frequency of operation of the circuit. It equally influences all

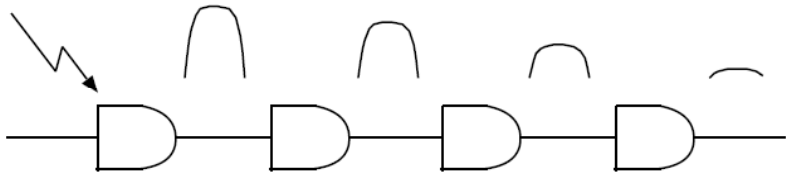


Figure 1.1: Electrical masking.

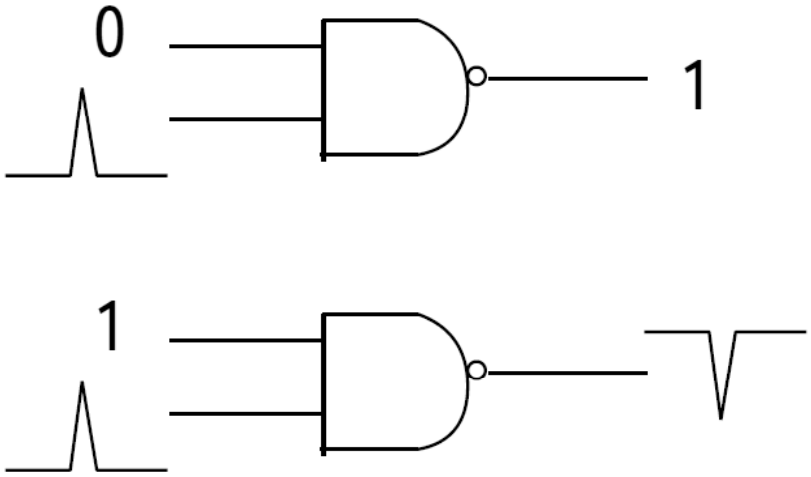


Figure 1.2: logical masking.

logic gates in the circuit. Therefore, reducing operation frequency increases the tolerance of circuit for soft errors.

Note that all these masking factors reduce the severity of a radiation particle hit in combinational circuits. In other words, if a logic gate in a circuit is masked to a large extent by any of these masking factors, then the output of that gate will unlikely have any effect on the primary outputs of the circuit by a particle hits. Only those sensitive gates in combinational circuit contribute significantly to soft errors. Only those gates in a combinational circuit that exhibit a low degree of masking due to these three factors. They are contribute significantly to the failure of the circuit due to soft errors.

Radiation particle hits were considered troublesome only for military and air space use. It is mainly due to the large number of radiation particles in the operating environment of such systems. The first radiation-induced error in air space was reported in 1975[10]. However, soft errors were also observed in microelectronics on the ground

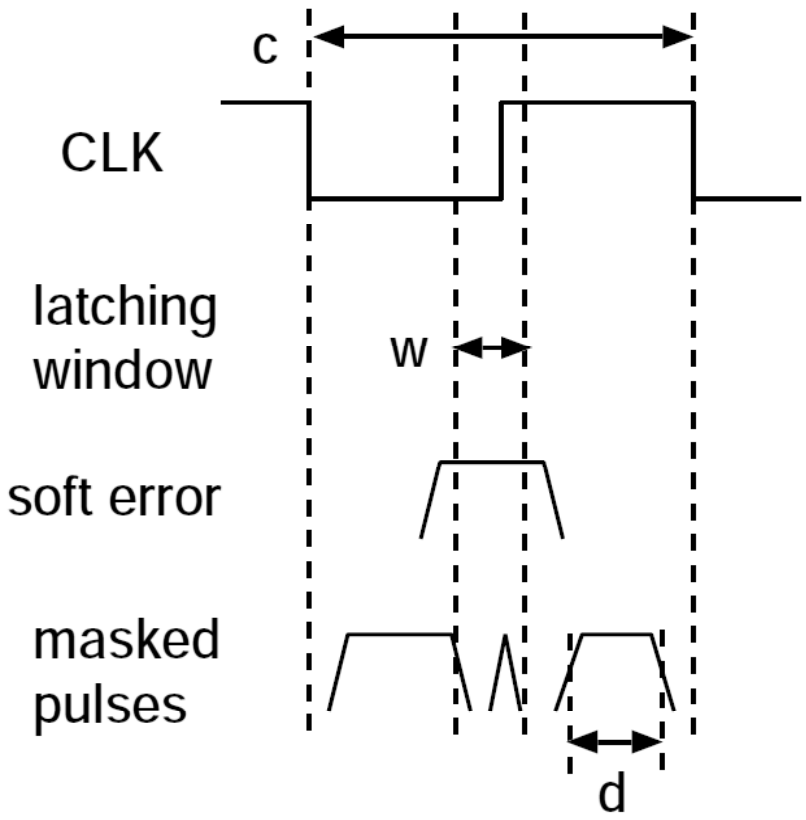


Figure 1.3: Temporal masking.

level in 1979[1]. After then, with technology downscaling, several cases of soft errors have been discovered in both air space as well as on the ground level[8]. Therefore, for applications such as air space, military, and electronics for higher reliability, it is important to use radiation tolerant circuits.

To efficiently design highly tolerant circuits against soft error, it is important to understand the mechanism of radiation particle hits on VLSI. This section contributes to discuss how these particles hit affect in current transients and the impact of technology downscaling on the sensitivity of VLSI to radiation particles.

1.1.1 Physical Origin of Particles for Soft Errors

In air space, cosmic rays enter the solar system from the galatic. These are some high-energy charged particles composed of protons, electrons, and heavy ions[11]. These particles cause soft errors in electronics used in outer space[8]. From those cosmic rays,

there are protons trapped in the radiation belts in the earth's atmosphere. These are also factors of SEEs. Alpha particles may also be deposit from radioactive contamination in IC packages and bording vires[8]. The first soft error reported was due to alpha-particles generated from IC packaging materials.

Recently, as the technology downscaling, VLSIs are sensitive to alpha particles, flip-chip packages have been identified as a source of radiation particles[8]. Also at the surface of the earth, neutrons induced soft errors have been very problematic. Several studies show that neutrons are a significant source of soft errors for memory systems at the ground level[8]. However, the flux of neutrons varies a lot by altitude or locations. a large number of neutron-induced soft errors were observed in DRAMs at 10,000 feet, while no upsets were observed when the DRAM was placed 200m underground in a salt mine[8].

1.2 Charge Generation and Collection Mechanisms

Each radiation particle such as protons, neutrons, alpha-particles, and heavy ions has different charge generation and collection mechanism. The mechanisms of charge deposition and collection are explained in this section.

1.2.1 Charge Generation

Direct Ionization Fig. 1.4 shows a radiation particle passes through a NMOSFET. Electron-hole pairs are generated along the particle. In this process, the radiation particle deposit its energy. It stops after losing all energy. The deposited energy from the radiation particle is described by its linear energy transfer (LET) value. LET is defined as the energy deposited from the radiation particle per unit length, normalized by the density of silicon. The unit of LET is usually MeV-cm^2/mg. The LET of a radiation particle also converts to the charge deposited per unit length. Heavy ions and alpha-particles deposit charge in a semiconductor by direct ionization. However, the particles such as protons and neutrons do not deposit charge by direct ionization.

Indirect Ionization Protons and neutrons deposit charge by indirect ionization, which can result in large numbers of soft errors[8, 4, 12]. When a high-energy light

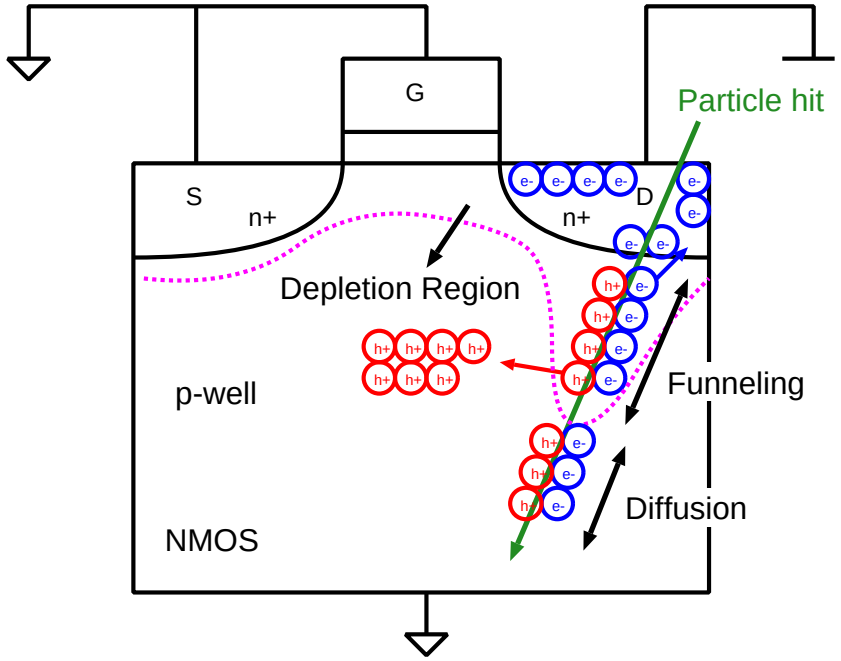


Figure 1.4: A radiation particle hits NMOS transistor. The charge generation and collection mechanisms occur.

radiation particle (such as a proton or a neutron) passes through a silicon device, it can result in nuclear reactions. These nuclear reactions may produce secondary particles such as alpha-particles or heavy ions. Then these secondary particles deposit charge by direction ionization. Moreover, if the charge is deposited at multiple positions in a chip then multiple soft errors may occur[8, 12]. Thus, the deposited charge by a light particle mainly depends on locations and angles of the particle-hit.

1.2.2 Charge Collection

Drift and diffusion Fig. 1.4 shows a cross section of an NMOS transisitor. The source, gate, and substrate node of the NMOS transistor are connected to the ground (GND). The drain node is connected to the power supply (VDD). The drain-substrate junction is reverse-biased, hence there is a strong electric field in the depletion region of this junction. When the electron-hole pairs are generated by radiation particle, the electrons are collected at the drain node and the holes are left in substrate by the electric field in the depletion region of the drain-substrate

junction. The reverse-biased electric field is the main factor of the charge collection into the drain. Therefore, the reverse biased junctions are most sensitive to a radiation particle.

As shown in Fig. 1.4, electron-hole pairs are deposited when a radiation particle hits the drain-substrate junction. After the particle hits, the width of depletion region is reduced due to the separation of the generated electrons and holes by drift process in the depletion region. This process resulting in the potential drop across the depletion region decreases. As the voltage between the drain and the substrate node is VDD, the decrease in the potential across the depletion region causes a voltage drop in the substrate region. This causes the drain-substrate junction electric field to penetrate into the substrate region, beyond the initial depletion region. This process is referred to as funneling as shown in Fig. 1.4. The funneling process increases the depth of the region with a strong electric field beyond the initial depletion region. It increases the amount of collected charge by the drift[13, 14, 15].

After funneling, the depletion region regains its initial width, the electrons that were not collected by the drift and diffuse toward the depletion region, then collected into drain region. Thus the charge is also collected by diffusion. It was reported in[14], that in a lightly-doping substrate, most of charge is collected through drift only. However in more heavily-doped substrates charge is collected due to both the drift and the diffusion processes[13, 14, 15, 16].

Parasitic Bipolar Effect (PBE) Electrons generated by a radiation particle can be collected at the drain. However, the radiation-induced holes are left in the p-well, which increases the potential of the p-well. As a result, the source injects electrons into the channel which can be collected into the drain. It increases the amount of the charge collected and reduces the tolerance of the transistor to a radiation particle hit. This effect is called the parasitic bipolar effect because the source-well-drain of the NMOS transistor act as a n-p-n bipolar transistor. Furthermore, with technology downscaling, the channel length decreases. The PBE becomes dominant in scaled technologies[15, 17].

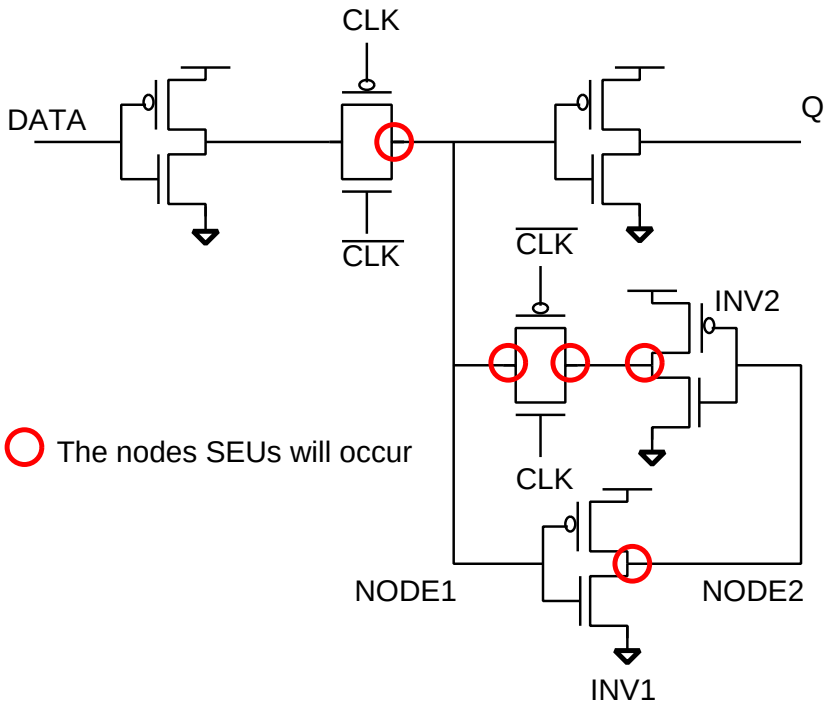


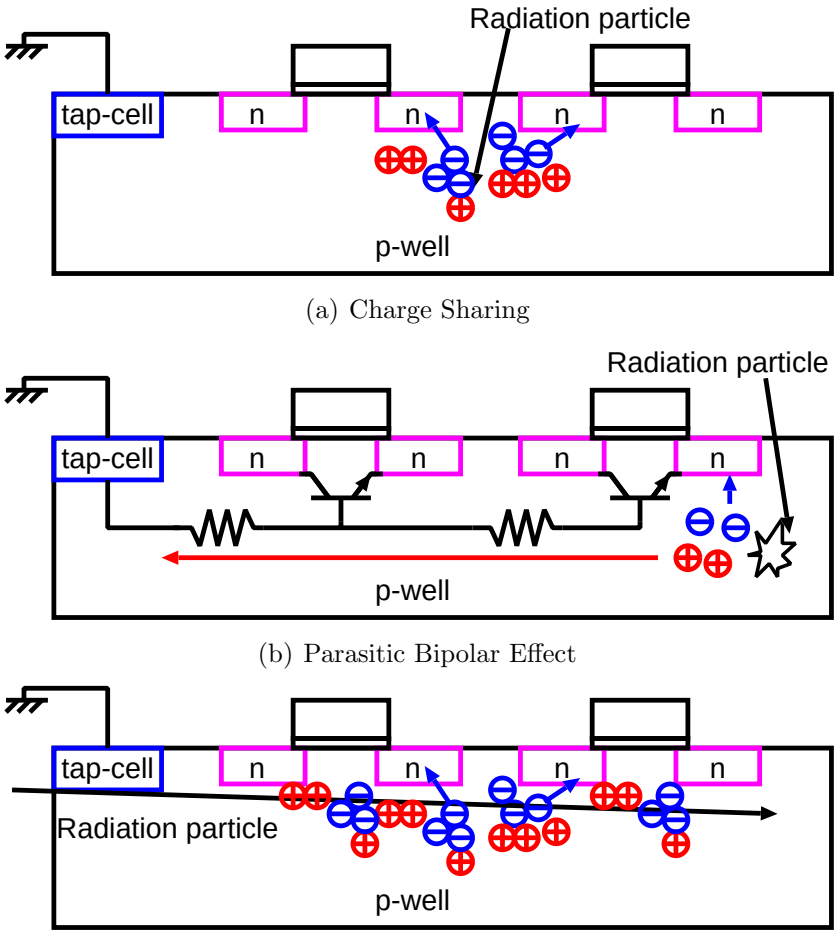
Figure 1.5: The mechanisms for SEU.

The charge collection at the drain node results in a current transients at that node. This is the main factor of soft errors.

1.3 Single Event Upset (SEU)

It store value in a loop structure micro-electronic devices such as SRAM and latch. It makes a change of state caused by one single ionizing particle striking the sensitive node in the circuits as shown in Fig. 1.5. Q is stored by "1" in this circuit. Charge is collected into the drain of NMOS in INV1 by a particle hits. Then the value of N2 is flipped from "1" to "0". The value of N1 is also flipped by inputting the Flipped value of N2. After that, the stored values of N2 is "0" and N1 is "1", the output of latch Q is upset. It directly flip the stored state of latch by a particle hits, causing a SEU.

There is a close relationship between the stored value of circuit and collected charge. The output is flipped when the value of collected charge is large enough. The smallest collected charge can flip the stored value is called critical charge (Q_{crit})[18]. As the technology downscaling also the reduction of VDD, the gate capacity of transistor keeps



(a) Charge Sharing

(b) Parasitic Bipolar Effect

(c) Successive Hits

Figure 1.6: Three factors which can cause MCU.

decreasing. It makes the reduction of Q_{crit}. SEU becomes much easier to occur. It necessary to increase the tolerance of SRAM circuits in server, super computer, and etc. The utilization of SEU tolerant latch circuit in server is also reported[19].

1.4 Multiple Cell Upset (MCU)

Several bits in SRAMs or latches upset at the same time by a radiation particle hit. This phenomena is referred as multiple cell upset (MCU). There are three factors which can cause MCU as follow:

Charge Sharing Fig. 1.6(a) shows the MCU caused by charge sharing. The size of transistor decreases by the technology downscaling. However, the area of the

nuclear reaction by the radiation particle does not be scaled. As a result, the generated electrons are collected at more than one drain node. It results MCU.

Parasitic Bipolar Effect As mentioned earlier, PBE is a main factor for charge collection. It is also cause MCU in the circuit as shown in Fig. 1.6(b). Since the electrons are collected into drain, holes are left in the p-well, the potential of the p-well is increased. Not only the bipolar transistor is turned on, also the adjascents bipolar transistors can be turned on. As a result, multiple transistor upset and cause MCU[20]. It will be discussed in Chap. 4 of this thesis, MCUs are effectively suppressed by high density well-contacts[21, 22].

Successive Hits There is another factor for MCU, which is referred as successive hits as shown in Fig. 1.6(c). Charge deposited near several transistors depends on the angle and location of the radiation particle.

The possibility of successive hits is very low. Thus, it is usually referred that charge sharing and PBE are two dominant factor for MCU. In order to reduce MCU rate in circuit, the suppression for charge sharing and PBE is important. The dummy transistor between transistors can collected the generated charge, it suppress the charge sharing effectively[23]. However, the MCUs caused by PBE can not be suppressed by the dummy transistor. Moreover, the probability of MCUs compared with SEUs is 10% in a 65 nm process[24]. MCU is one of critical issues to diminish soft-error resiliency of radiation designs[25, 26]. The radiation-hardened circuit such as redundant flip-flops become sensitive for MCU as the technology downscaling. The device level countermeasure for MCU is mainly discussed in this thesis later.

1.5 Objective of My Thesis

Usually, beam tests and simulation are two ways to investigate the soft error tolerance of circuits. However, as beam test costs expensive, it is hard to test all logic elements of VLSIs. Moreover, the mechanisms and the tolerance of soft errors in the highly-scaled processes and future structures have not been discussed enough. Thus, simulations play a very important role in mitigations and projections for SER.

As discussed in this chapter, the charge collection mechanism has become more complex due to technology downscaling and high densities of circuits. Not only the charge sharing, also the PBE become dominant when a particle hits on latches or flip-flops[26]. Radiation-hardened circuits sometimes become sensitive for MCU. In order to suppress MCU, the mechanisms for MCU in the scaled radiation-hardened circuit must by analyzed. However, it is time consuming to simulate all charge collection mechanisms by circuit level simulations. Also the accuracy of simulations must be increased. Utilization of device- and physiccal-level simulations becomes much more important.

My thesis focuses on projection and mitigation of SERs on various radiation-hardened circuits by device- and physical-level simulations. SERs of different various circuits, lay-out and device structures are discussed. A Monte-Carlo based simulation methodology is also proposed to persuit accuracy.

The organization of this thesis is as follow:

The importance of device and physical level simulations are described in Chapter 2. The charge collection mechanisms in device-level can be analyzed clearly with low cost in short time. Several simulation tools are used in this research. In order to compare the simulation results to neutron-beam test, the Monte-Carlo based physical-level simulator PHITS is also used. In this thesis, the charge generation and collection mechanisms by direct ionization are simulated by a TCAD simulator, and the mechanisms by indirect ionizations are simulated by PHITS.

In Chapter 3, the PBE are investigated to suppress MCUs on radiation-hardened dual-modular flip-flops 65-nm process[27]. Device simulations reveal that a simultaneous flip of redundant latches is suppressed by storing opposite values instead of storing the same value due to its asymmetrical structure. The state of latches becomes a specific value after a particle hit due to the PBE. Spallation neutron irradiation proves that MCUs are effectively suppressed in the D-FF arrays in which adjacent two latches in different FFs store opposite values. The redundant latch structure storing the opposite values is robust to the simultaneous flip.

In Chapter 4, the contributions of layout structures to suppress MCU are analyzed by device-level simulations and neutron experiments[28]. Device simulation results reveal that the ratio of MCU to SEU decreases by increasing the distance between 65-nm

process redundant latches. MCU is suppressed when well contacts are placed between redundant latches. Experimental results also show that the ratio of MCU to SEU decreases by increasing the distance between redundant components. MCU is suppressed effectively by increasing the density of well contacts.

In Chapter 5, the SERs of 65-nm SOTB (Silicon on Thin BOX) and 28-nm UTBB (Ultra Thin Body and BOX) FD-SOI processes are evaluated. The proposed Monte-Carlo based simulation methodology called PHITS-TCAD estimates the SERs depending on thickness of BOX regions and body bias. The SERs can be analyzed with layout patterns. The simulated results are consistent with the alpha and neutron irradiation measurement results. Simulated results reveal that the SERs are decreased by increasing the thickness of BOX region. By applying the reverse body bias, the tolerance for soft error becomes stronger in SOTB while that in UTBB becomes weaker.

Finally, Chapter 6 summarizes the contribution of this thesis.

Chapter 2

Simulation Methods for Soft Errors

There are two ways to evaluate the tolerance of radiation-hardened circuits, the irradiation experiments and simulations. However, irradiation experiments cannot be carried out for all logic elements because the experimental cost is high, a normal standard cell library usually has several hundred logic cells. Simulations are necessary to evaluate the tolerance for soft errors in sequential circuits.

As mentioned in the last chapter, there are two charge generation mechanisms by radiation particles, the direct and indirect ionizations. In this thesis, the TCAD simulator Sentaurus[29] is used to perform all device-level simulations. However, since there are heavy-ion models in Sentaurus. It is difficult to simulate the charge generation mechanism by indirect ionization. The nuclear reactions by indirect ionization can be simulated by physical-level simulators, such as PHITS[30]. In this chapter, the simulation methods for soft errors are explained in detail.

2.1 Basics of Device-Level Simulations

The charge collection mechanism has become more complex due to technology downscaling and high densities of circuits. Not only the charge sharing, also the bipolar effect become dominant when a particle hits on latches or flip-flops[26]. Some radiation-hardened circuits become sensitive for MCU. In order to suppress MCU, it is necessary to analyze mechanisms for MCU in the scaled radiation-hardened circuit. However, it is difficult to simulate all charge collection mechanisms by the circuit level simulation. The high simulation accurate is necessary. Utilization of device-level simulation becomes much more important. In this section, the basic simulation methods for soft errors are

explained.

2.1.1 Simulation Tools

The followings are the advantages of device-level simulation.

1. The device structures and elements of circuits can be constructed in short time.
2. The high-cost irradiation experiments can be replaced.
3. The phenomena or mechanism in device-level can be replaced.

The device-level simulations are performed by the following tools in this thesis.

Sentaurus WorkBench (SWB) SWB is a software package that provides a convenient framework to design, organize, and automatically run complete TCAD simulation projects. SWB also supports design-of-experiments, extraction and analysis of results, optimization and uncertainty analysis. It has an integrated job scheduler to speed up simulations and takes full advantage of distributed, heterogeneous and corporate computing resources[31].

Sentaurus Structure Editor (SSE) SSE is a two-dimensional (2D) and three-dimensional (3D) device structure editor. Two-dimensional models can be used to create 2D structures or 3D structures can be defined directly. When a 3D model is created, three-dimensional device editing operations and process emulation operations can be applied interchangeably to the same model. The 2D and 3D structure editing modes include geometric model generation, doping and refinement definition, and submesh inclusion to generate the mesh command file[32].

Sentaurus Device Sentaurus Device is a multidimensional, electrothermal, mixed-mode device and circuit simulator for one-dimensional, two-dimensional, and three-dimensional semiconductor devices. It incorporates advanced physical models and robust numeric methods for the simulation of most types of semiconductor device ranging from very deep-submicron silicon MOSFETs to large bipolar power structures[33].

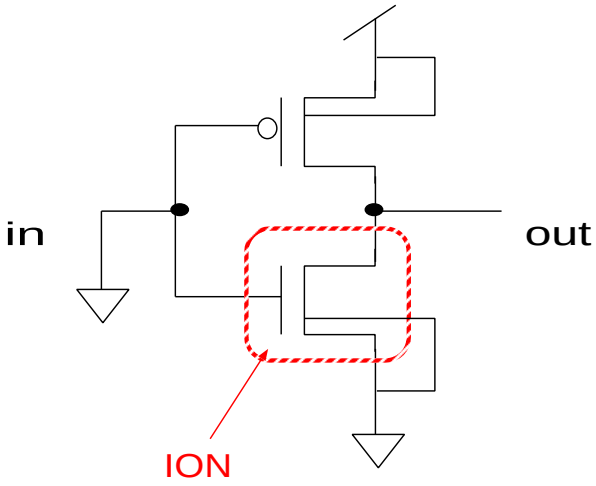


Figure 2.1: Circuit of inverter in 65-nm process.

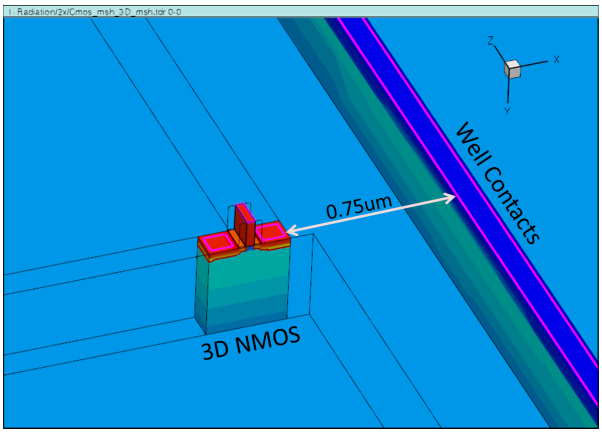


Figure 2.2: 3D device-level NMOS transistor constructed by Sentaurus.

Inspect Inspect is a curve display and analysis program. It works with curves specified at discrete points. Inspect enables users to work interactively with data using both a graphical user interface and a script language[34].

2.2 Analysis of Soft Error Tolerance by the Device-level Simulations

In this section, the simulation methods to evaluate SEU in an inverter are introduced. It is the basis of simulations for soft errors.

Simulation Setup

A radiation particle hits at the NMOS transistor of an inverter (INV) shown in Fig. 2.1. It is constructed in a 65-nm bulk technology. The input of INV is connected to GND and hence, the PMOS transistor is ON state and the NMOS transistor is OFF state. The 3D device simulation is used to simulate INV in Fig. 2.2 when a radiation particle hits at the drain of the NMOS transistor. Sentaurus is a mixed-level device and circuit simulator. The NMOS transistor of INV is modeled in the 3D device domain as described later. The PMOS transistor of INV is modeled using a PTM[35] SPICE model in the circuit domain.

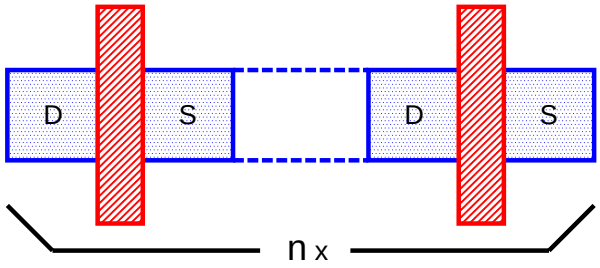
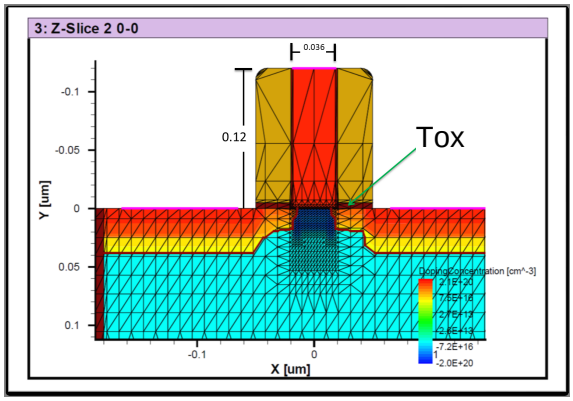
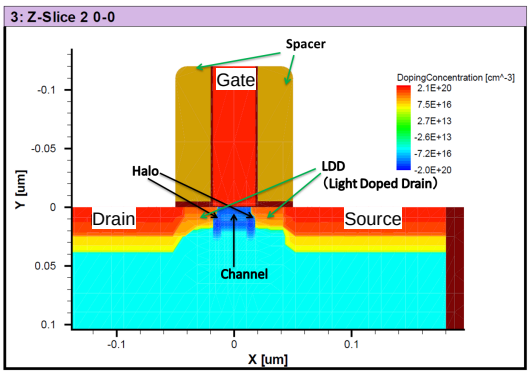


Figure 2.3: N × Inverter



(a) The Parameter of NMOS Transistor (with mesh)



(b) The Doping of NMOS Transistor

Figure 2.4: The Cross Section of 3D Device-level NMOS Transistor.

To analyze the soft error tolerance of the INV circuit, the size of INV of Fig 2.1, as well as the LET of the radiation particle, are varied to simulate different radiation scenarios. The supply voltage (VDD) of INV is 1 V in the 3D simulations. INVs of sizes 2x, 4x and 15x are simulated as shown in Fig. 2.5∼2.7. The width of the NMOS and PMOS transistors in a 2x INV is 0.13μm and 0.52μm. The radiation particle LET values are 2, 10, 20 and 50 MeV-cm^2/mg.

3D Device-Level Model

The Sentaurus-Structure editor tool[29] is used to construct the 3D NMOS transistor of the INV in Fig. 2.1. The cross section of this NMOS model is shown in Fig. 2.4. The NMOS device is constructed in a 65-nm bulk technology. The 3D 65-nm bulk model is developed based on the data available in[26, 36, 37, 38, 39]. According to these

references, the value of the parameters are as follows: the gate length L=35 nm, oxide thickness Tox=12 nm, spacer width=30 nm and the height of the polysilicon gate=0.12 μm. The punch through, halo and latchup implants are also modeled in the NMOS device. (Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. Scaling requires the use of Halo and latchup implants for control of short channel .)

The details of the above implants are as follows: For the threshold (punch through) implant, the peak doping concentration of Boron atoms is 8x10^{1}8 cm^3 (7x10^{1}8 cm^3) at 2 nm (14 nm) below the SiO2-channel interface, the doping decreases with a Gaussian profile, and reduces to 1x10^{1}7 cm^3 (2x10^{1}7 cm^3) at a depth of 14 nm (5 nm) below the peak concentration surface. The peak concentration of Boron for halo implants is 2x10^{1}9 cm^3. These implants are in the channel region at the source-well and drain-well junctions. For the latchup implant, the peak doping of Boron is 5x10^{1}8 cm^3 at 1.25 μm below the SiO_2-channel interface. The doping reduces to 1x10^{1}6 cm^3 at a depth of 0.4 μm.

Particle Irradiation Simulation Results

Fig. 2.5〜2.8 shows the voltage outputs by a particle hits at the drain of the NMOS transistor. The LET of the particles are 2, 10, 20 and 50 MeV-cm^2/mg. A radiation particle is capable to generate a significant voltage glitch at the outputs. For larger LET values, the voltage at the output of INV becomes negative. These simulation results shows that the 65-nm devices are very sensitive to radiation particle hits. Fig. 2.8 show the widths of the voltage glitch at the VDD/2 (0.5 V) depending on the size of INVs. The width decreases by increasing the size of INV. The soft error tolerance becomes stronger by upsizing INV.

2.3 Particle and Heavy Ion Transport Code (PHITS)

As the above introduction, the soft error by a radiation particle can be simulated by the device-level simulation SENTAURUS. However, there is only heavy ion and alpha irra-

diation particle models in SENTAURUS. Hence, the soft error mechanisms by indirect ionization can not be simulated. At the ground level, errors are induced by reactions of cosmic ray neutrons. The neutron irradiation test is always used to evaluate the soft error tolerance of circuits. In order to compare the simulation results to neutron irradiation test, the Monte-Carlo based physical-level simulator PHITS is used in this research.

PHITS stands for Particle and Heavy Ion Transport Code. It can transport and collision of nearly all particles over wide energy range. All contents of PHITS (source files, binary, data libraries, graphic utility etc.) are fully integrated in one package. In this thesis, PHITS is used to evaluate and project the soft error rate by the indirect ionization such as neutron. It will be explained in Chapter 5 in detail.

2.4 Chapter Summary

Simulation is required to evaluate the tolerance for soft errors in sequential circuits. The charge collection mechanism has become more complex due to technology downscaling. Utilization of device-level simulations becomes much more important. The charge collection mechanisms in device-level can be analyzed clearly with low cost in short time. Several simulation tools are used in this research. In order to compare the simulation results to neutron irradiation test, the Monte-Carlo based physical-level simulator PHITS is also very important. In this thesis, the charge generation and collection mechanisms by direct ionization are simulated by TCAD simulator SENTAURUS, and the mechanisms by indirect ionization are simulated by Monte-Carlo based physical simulator PHITS. The details are described from the next chapter.

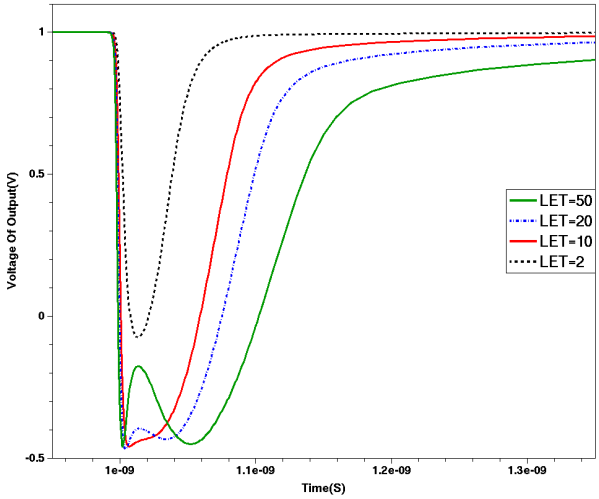


Figure 2.5: Voltage output by a particle hits at 2×INV

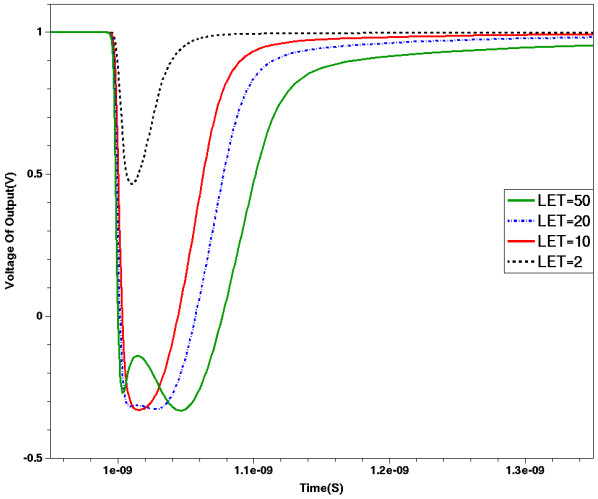


Figure 2.6: Voltage output by a particle hits at 4×INV

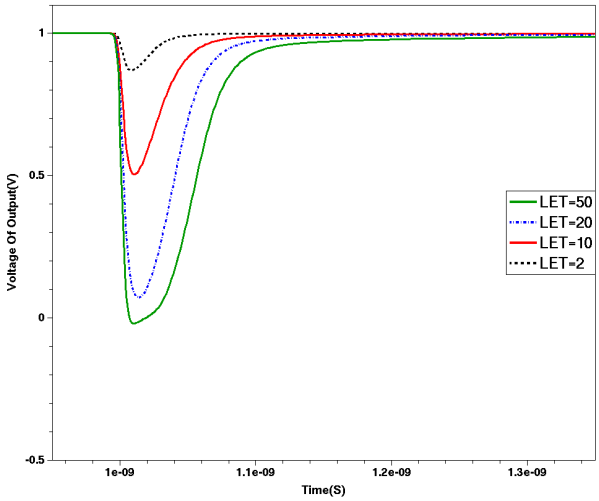


Figure 2.7: Voltage output by a particle hits at 15×INV

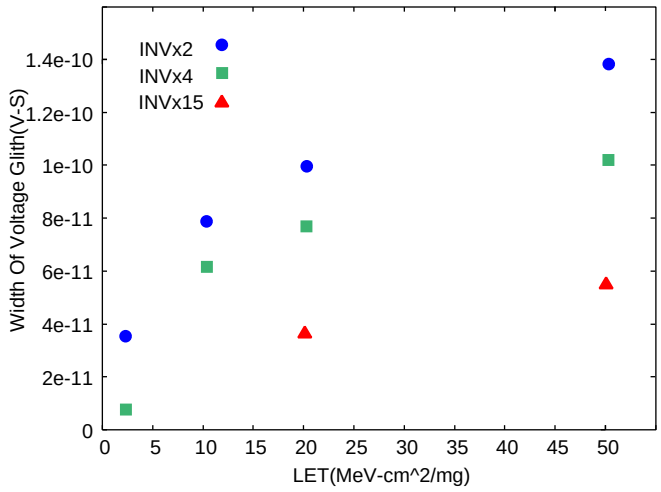


Figure 2.8: The width of the voltage glitch at VDD/2 depending on the size of INV.

Chapter 3

Suppression for Multiple Cell Upset by Parasitic Bipolar Effects in a Radiation-Hardened Redundant Flip-Flops

According to the process scaling, radiation-hard devices are becoming sensitive to soft errors caused by Multiple Cell Upset (MCUs). In this chapter, the parasitic bipolar effects are utilized to suppress MCUs of the radiation-hard dual-modular flip-flops. Device simulations reveal that a simultaneous flip of redundant latches is suppressed by storing opposite values instead of storing the same value due to its asymmetrical structure. The state of latches becomes a specific value after a particle hit due to the bipolar effects. Spallation neutron irradiation proves that MCUs are effectively suppressed in the D-FF arrays in which adjacent two latches in different FFs store opposite values. The redundant latch structure storing the opposite values is robust to the simultaneous flip.

3.1 Introduction

Process scaling makes semiconductor chips less reliable to temporal and permanent failures. Temporal failures flip a stored value on SRAMs or flip flops. Soft errors are classified into Single Event Upset (SEU) and Single Event Transient (SET). SEU is caused by a particle hit on sequential elements, and SET is caused by a particle hit on combinational circuits. Recently, parasitic bipolar effects have been reported to be a

source of multiple cell upset (MCUs). Seifert et.al. [24] reveals that the probability of MCUs compared with SEUs is 10% in a 65 nm process. MCUs are one of critical issues to diminish soft-error resiliency of radiation designs.

Various redundant flip-flop structures are proposed such as TMR, DICE[19] and BISER[40] to mitigate soft errors, However, aggressive process scaling makes the probability of MCUs greater. MCUs are one of critical issues to diminish soft-error resilience of radiation-hard designs because these designs are very sensitive to simultaneous flips. The parasitic bipolar effect plays an important role on soft errors in a current deep-submicron process[41]. If a particle hit on a transistor, adjacent transistors are affected by the parasitic bipolar effects, which results in an MCU of redundant components. This chapter shows the parasitic bipolar effects to have a significant impact on MCUs. We show that two latches storing opposite values can suppress the simultaneous flip due to the parasitic bipolar effect[42]. All simulation models are constructed by using a 65-nm process.

This chapter is organized as follows. Section 3.2 and 3.3 explains the relationship between latch and the parasitic bipolar effects. In Section 3.4, device-level simulations investigate the simultaneous flip and error rate of redundant latches in detail. Section 3.5 shows the experimental results by spallation neutron irradiation of a D-FF array. Finally, Section 3.6 concludes this Chapter.

3.2 Relationship between PBE and SEU

When a neutron hits to a Silicon atom, electron-hole pairs are generated. Electrons can be collected at the drain-well or well-substrate junction. However, the holes are left in the p-well, which reduces the source-well potential barrier due to the increase in the potential of the p-well. Thus, the source injects electrons into the channel which can be collected at the drain. This effect is called the parasitic bipolar effect because the source-well-drain of the NMOS transistor acts as an n-p-n bipolar transistor. It will turn on the parasitic bipolar transistor. SRAMs in the triple-well structure have 3.5x higher probability of MCUs compared to twin-well in a 65-nm process by neutron irradiation[43]. Due to these bipolar effects, adjacent transistors are affected, which results in simultaneous upsets of latches. These simultaneous upsets diminish the error

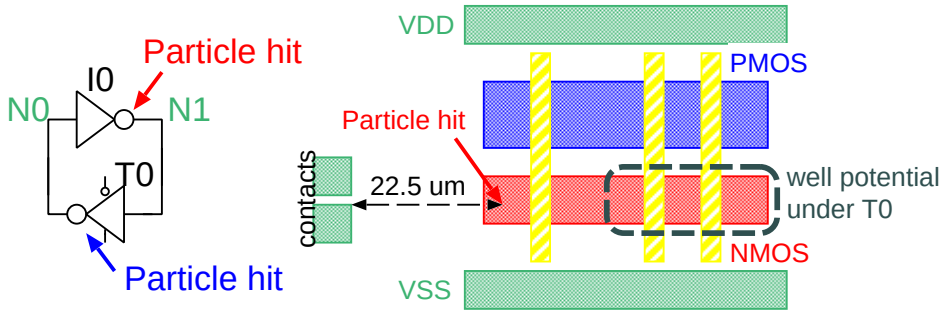
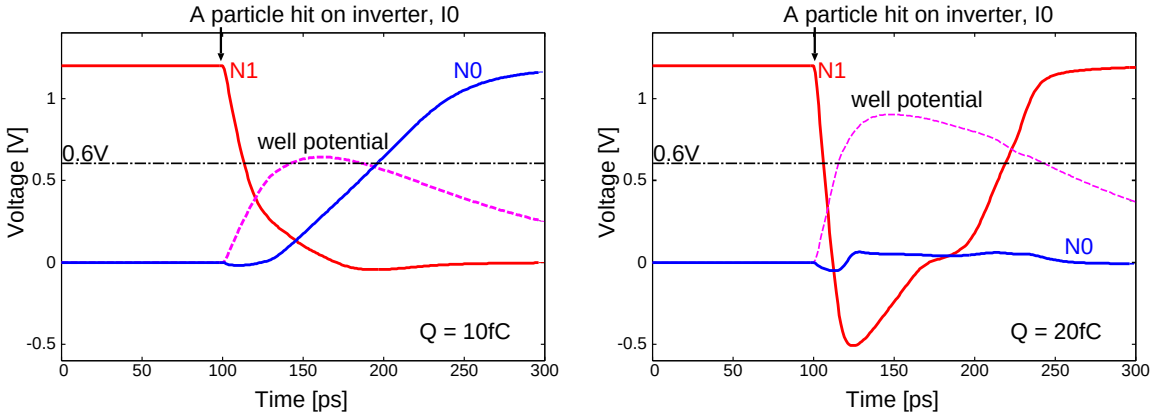


Figure 3.1: Schematic (left) and layout (right) of conventional latch.

resilience of redundant latches. But it is possible to eliminate simultaneous upsets from soft errors by enhancing circuit structures which utilizes the parasitic bipolar effects.

Figure 3.1 is a conventional latch structure and its layout. Fig. 3.2 shows two circuit level simulations results[44] when generated charge (Q) is 10 fC and 20 fC respectively. A particle hit on the NMOS transistor of I0 in Fig. 5.9 (red line). Well contacts are placed at 22.5 μm far away from the particle hit. If generated charge is more than the critical charge (Q_{crit}), the latch is upset as in Fig. 3.2 (a). Thus the latch is always upset by a particle hit with higher energy without considering parasitic bipolar effects. On the other hand, if generated charge is large enough to elevate well potential under T0 above a certain level, the latch is stable with considering the parasitic bipolar effect as in Fig. 3.2 (b). In this case, the output values of the inverter becomes around 0 after a particle hit. Due to the high particle energy, the bipolar transistor under the tristate inverter is turned on. Thus, the output values of these two components keep 0 for a while at the same time. When the well potential falls to a certain level at which the bipolar transistors turn off, the output of the inverter always goes back to its original state. It is because the delay time of the inverter is faster than the tristate inverter. The process variations may influence the delay time. By the circuit-level simulations, the tristate inverter is never faster than the inverter even if variations influence delay. Note that we assume that variations influences the transistor parameters by 2σ since these two inverters are placed very closely. Thus, by utilizing the parasitic bipolar effects, it is possible to enforce redundant flip-flops to MCUs and soft errors.

There are two device simulation results as shown in Fig. 3.3 (a) and (b). They are the similar to the results of circuit simulations as shown in Fig. 3.2. Fig. 3.4 (a) and



(a) (b)

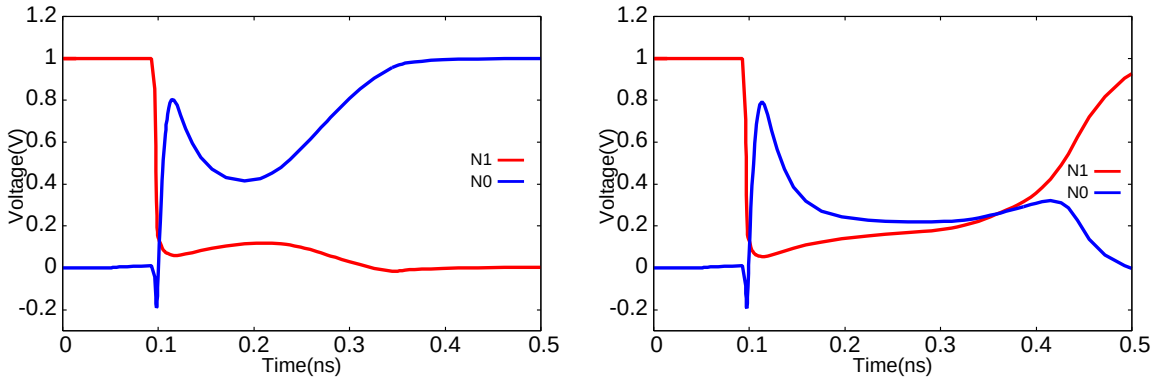
Figure 3.2: Circuit-level transient simulation by a particle hit on I0 in Fig. 5.9 with Q=10 fC (a) and Q=20 fC (b).

(b) show other device simulation results when N0=1, N1=0. In this case, the latch is not stable even if the parasitic bipolar transistor turns on. Due to the parasitic bipolar effect, the outputs of the inverter and the tristate inverter keep "0". After the bipolar transistor turns off, the inverter always goes to "1" before the tristate inverter. Thus the latch is upset when Qcrit is large in this case.

There are other two simulations results as shown in Fig. 3.5 (a) and (b) when a particle hit (blue line) on the tristate inverter T0. The latch is always stable (Fig. 3.5) when N0=0, N1=1, because the parasitic bipolar transistor under the tristate inverter is always "ON" by a particle hit. The tristate inverter always keeps "0". Then, the inverter goes back to its initial state quickly when the bipolar transistors turn off. In contrast the latch is always upset (Fig. 3.6) when N0=1, N1=0. In this case, the parasitic bipolar effects keep the outputs of tristate inverter and inverter "0" at the same time. However, the inverter always goes to "1" firstly.

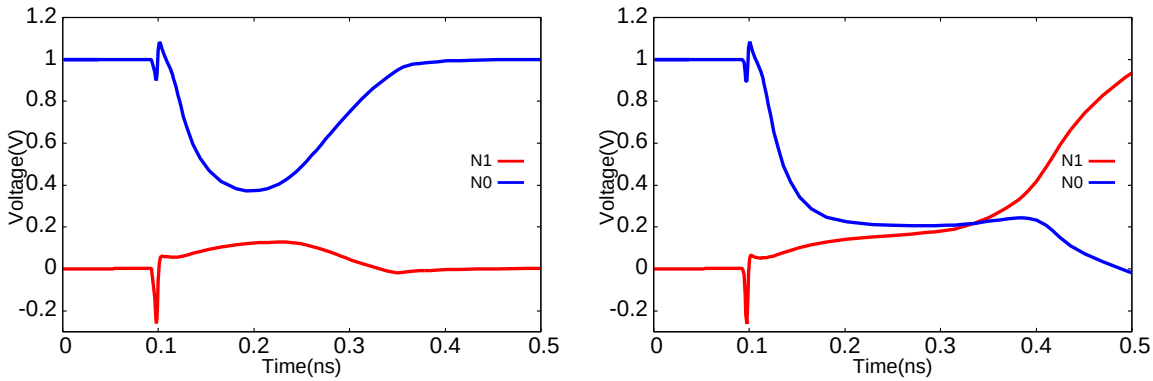
3.3 Redundant Latch Structure to Suppress MCUs

Fig. 3.7(a) shows a pair of redundant latches which store the same value in conventional redundant FFs such as TMR or BISER, while Fig. 3.7(b) shows of those storing the opposite values in the BCDMR FF [45] as shown in Fig. 3.8. In the BCDMR FF, two latches (ML0+ML1 or SL0+SL1) and a keeper (KM or KS) construct a triple-modular redundancy (TMR). In BISER or BCDMR, the output of FFs is stable even if one of



(a) Q=30 fC (b) Q=80 fC

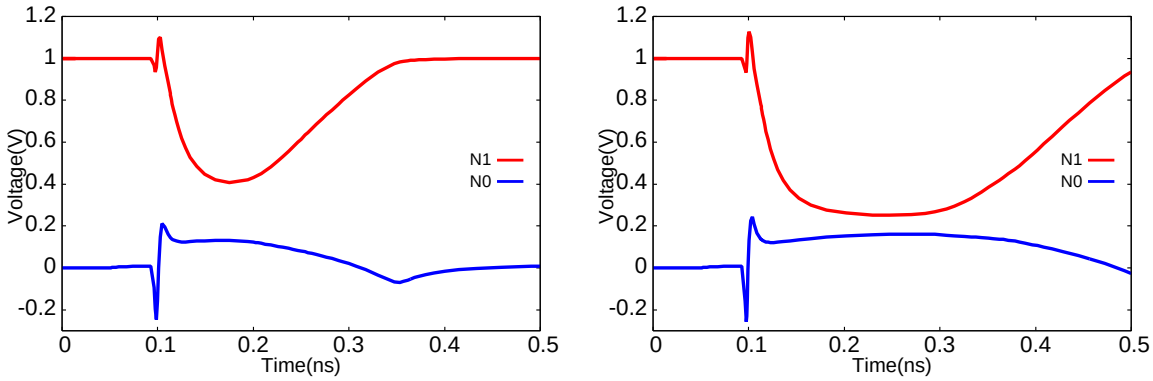
Figure 3.3: Transient waveform of N1 and N0 by a perpendicular particle hit on T1 according to the charge "Q" (N1=1, N0=0).



(a) Q=30 fC (b) Q=80 fC

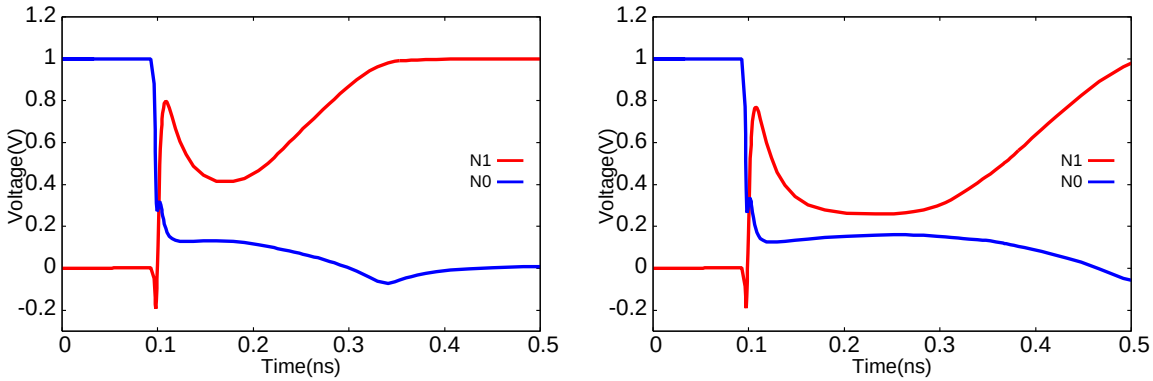
Figure 3.4: Transient waveform of N1 and N0 by a perpendicular particle hit on T1 according to the charge "Q" (N1=0, N0=1).

two redundant latches is flipped. In order to eliminate a simultaneous flip among these TMR components, these two latches are placed in two rows as shown in Fig. 3.9, which structure is called the double-height cell structure[23]. The keeper is in the same row as one of two latches but it is placed as far apart as possible [46] from the latch. If both redundant latches stores the same value as in Fig. 4.10, they can be upset at the same time by a particle hit. It is because the parasitic bipolar effects change the latches to the same value. However, if both latches store the opposite values, a particle hit with large amount of charge may change the latches to the same value. At least one of two latches is stable in the original state when they store opposite values. As a result, the



(a) Q=30 fC (b) Q=80 fC

Figure 3.5: Transient waveform of N1 and N0 by a perpendicular particle hit on T0 according to the charge "Q" (N1=0, N0=1).



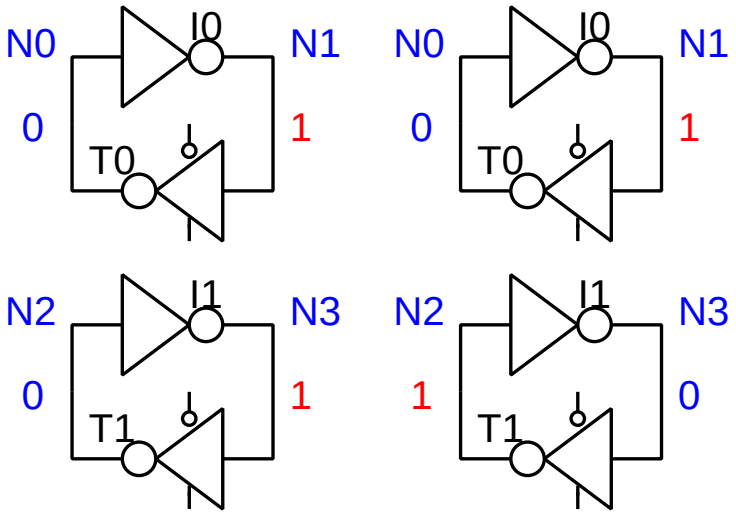
(a) Q=30 fC (b) Q=80 fC

Figure 3.6: Transient waveform of N1 and N0 by a perpendicular particle hit on T0 according to the charge "Q" (N1=0, N0=1).

output of the redundant FF is not flipped. The possibility of the simultaneous flip can be drastically reduced when both latches store opposite values.

3.4 Suppression for MCU in Redundant Latches by Device-level Simulations

In this section, we use device simulations to show that MCUs are suppressed by the parasitic bipolar effects.



(a) Store the same value (b) Store opposite values

Figure 3.7: Two redundant latch structures.

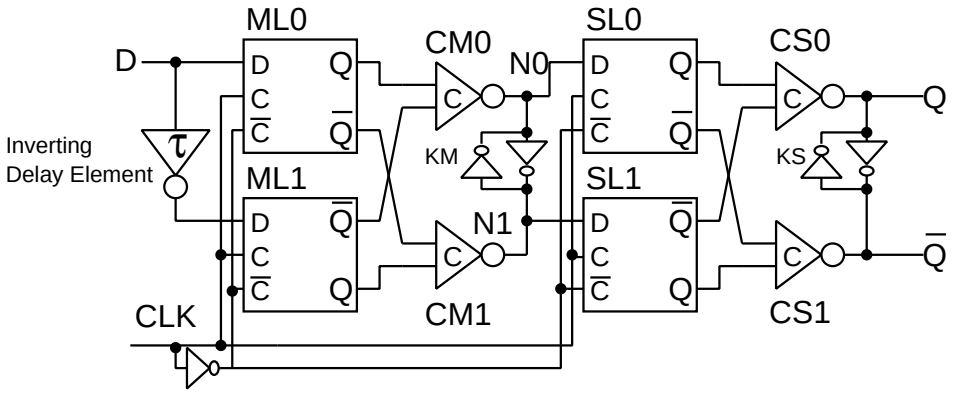


Figure 3.8: BCDMR FF

3.4.1 Device-level Simulation Setup

Fig. 3.9 shows the layout structure of two latches placed in two rows sharing the NMOS region in the p-well. The double-height cell structure sharing PMOS regions is more robust to soft errors than sharing the NMOS regions, since the mobility of holes is slower than that of electrons. For showing the results clearly, we constructed the device models sharing the NMOS regions. As the full 3D device-level model prolong simulation time, the mixed-mode device-simulation is used in which the 2D PMOS and 3D NMOS device-level models are connected by wires in the circuit-level as shown in Fig. 3.10. The well contact is placed at 2.75 μm from T0 and T1. The distance between I0 (T0) and

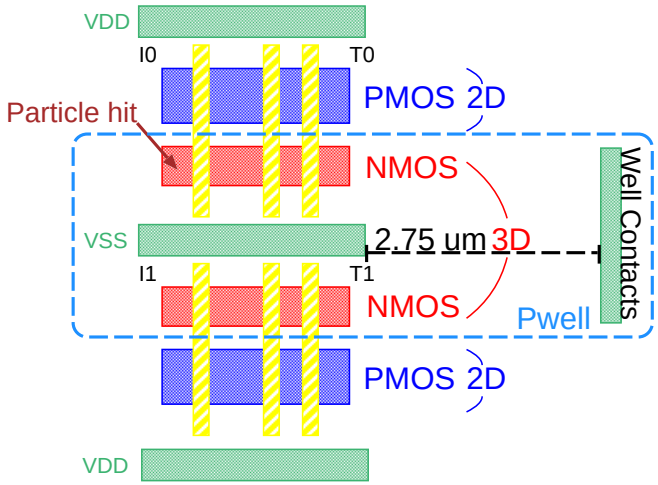


Figure 3.9: Two latches placed in two rows.

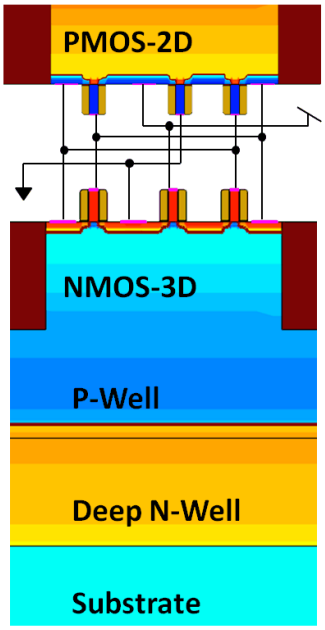


Figure 3.10: Mixed-mode model.

I1 (T1) is 0.3 μm. The area of the p-well is 10 μm x 10 μm. As we mentioned in the Sect. 3.2, MCUs are very likely to occur in the triple well structure. Thus all device-level structures are constructed in the triple-well. The device model is constructed according to the 65-nm device structures and parameters in Sect.2.

According to the results of device simulations, there are MCUs in both structure in which two latches store the same or opposite values. However, the MCU rates of the structure in which two lathes store opposite values are much lower. We explain details

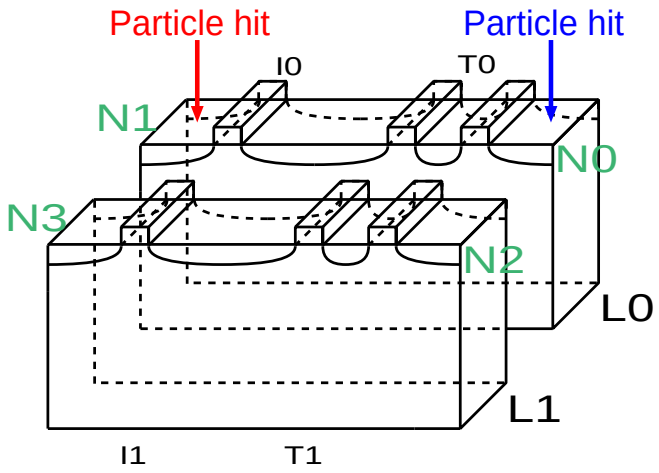


Figure 3.11: Perpendicular particle hit on NMOS of I0 or T0.

in the following sections.

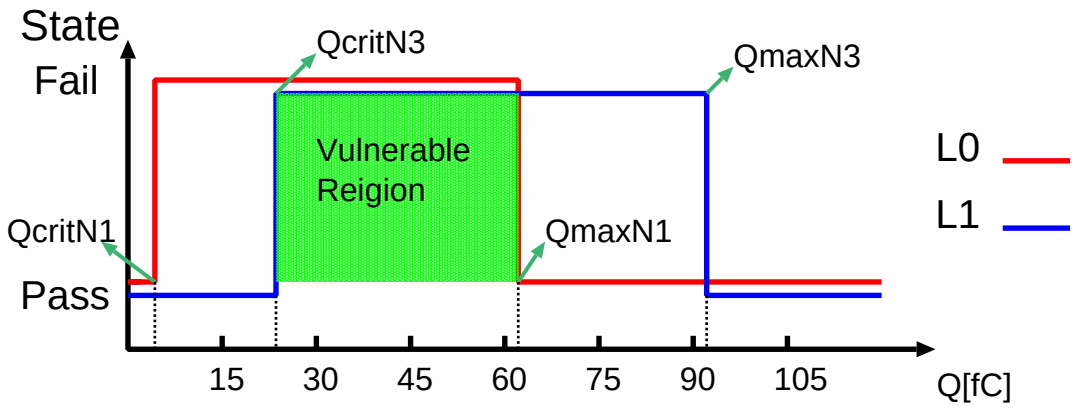
3.4.2 Perpendicular Particle Hit Case

When a particle hit on the NMOS transistor of I0 perpendicularly as drawing with the red line in Fig. 3.11, the upper latch (L0) is affected by the collected charge and the bipolar effect while the lower latch (L1) is mainly affected by the bipolar effect.

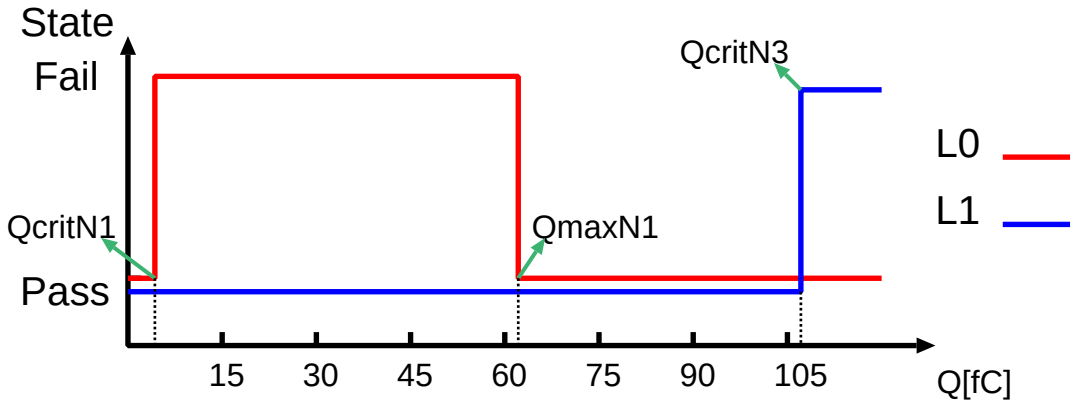
Fig. 3.12 (a) and (b) represent the states of the pair of two latches according to the charge collected to the node N1 and N3 as in Fig 3.7. We set "1" as the original value of N1. The results when latches stores the same value (N3=1) and opposite values (N3=0) are shown in Fig. 3.7(a) and (b), respectively. The values of collected charge "Q", $Q_{\mathrm{crit}N_x}$, $Q_{\mathrm{max}N_x}$ denote the collected charge when a latch is flipped and goes back to its original state by the parasitic bipolar effect, respectively.

When two redundant latches store the same value, they are flipped at the same time by charge between $Q_{\mathrm{crit}N_3}$ and $Q_{\mathrm{max}N_1}$ as shown in Fig. 3.2 (a). We call the green region in Fig. 3.12 (a) as the vulnerable region in which both redundant latches flip. The inverter I0 is stable at its original state and the tristate inverter T0 does not flip at the charge above $Q_{\mathrm{max}N_x}$ by the parasitic bipolar effect as shown in Fig. 3.2 (b). A vulnerable region exists between 22.5 fC and 62 fC as in Fig. 3.12 (a) when latches store the same value. When they store the opposite values, however, they are not flipped at the same time as shown in Fig. 3.12 (b). In this case, T1 is vulnerable, but the required charge is much more than I0 because of its poor drivability. Therefore, there is no vulnerable region in which both redundant latches are flipped at the same time. Fig. 3.13 (a) and (b) show transient voltage waveforms obtained from device-level simulations of particle hits with collected charge Q=30 fC and 80 fC in which the latches store the same value. The original value of N1 is "1". The node N1 flips at Q=30 fC but goes back to its original state at Q=80 fC, while the node N3 flips in both cases. In contrast, Fig. 3.14 (a) and (b) show transient voltage waveforms when the collected charge Q=30 fC and 80 fC in which the latches store the opposite values. The node N3 does not flip in both cases. No simultaneous flips are observed.

When we set "0" as the original value of N1 as in Fig. 3.15 (a) and (b), the results of these two situations in which two redundant latches store the same value and opposite values are shown in Fig. 3.16 (a) and (b) respectively. In the former case, they are flipped



(a) Store the same value

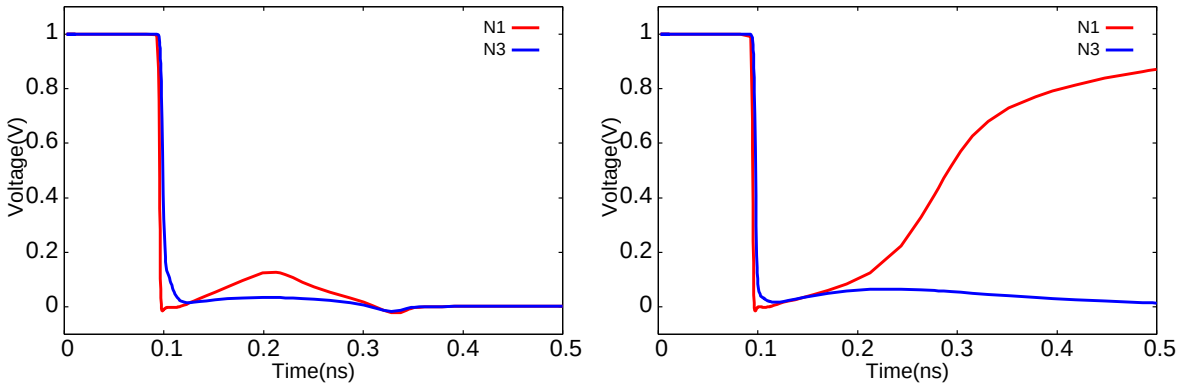


(b) Store opposite values

Figure 3.12: States of N1 and N3 by a perpendicular particle hit according to the charge "Q".

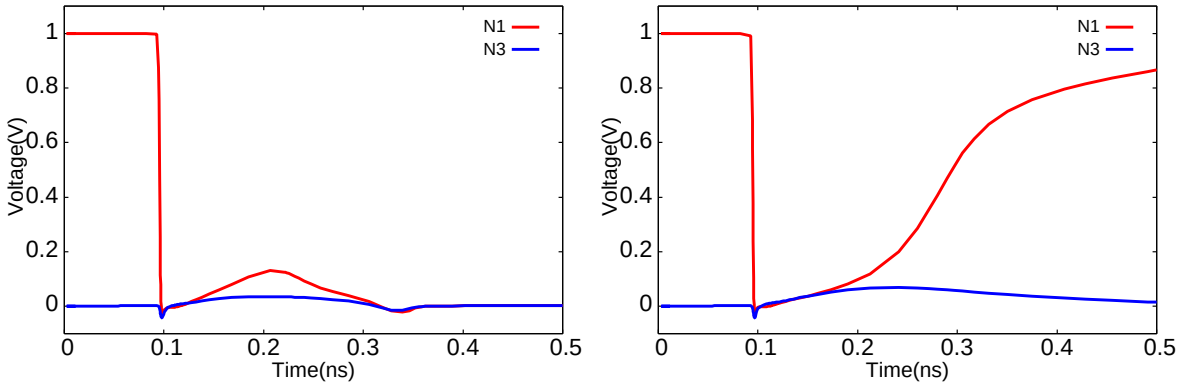
at the same time when the collected charge is bigger than 107 fC as in Fig. 3.16 (a). In the latter case, they are also flipped at the same time by the collected charge between 60 fC and 92 fC as in Fig. 3.16 (b). The MCU tolerance when storing the opposite value is much stronger when storing the same value as in Fig. 3.12 (a).

Fig. 3.17 shows two other results of device simulations in which a particle hit on NMOS of the tristate inverter T0 when N1=N3=0 (Fig. 3.11 (blue line)). When N1=0, both latches are flipped at the same time as shown in Fig. 3.17 (a) when both latches store the same value. Only one latch is flipped when the two lathes store opposite values as in Fig. 3.17 (b). Thus, there is no vulnerable region when two lathes store opposite values in this case. In contrast, there is no MCU occurrence in both of redundant FFs when N1=1.



(a) Q=30 fC (b) Q=80 fC

Figure 3.13: State of N1 and N3 vs. Q when two latches store the same value (N1=1,N3=1)



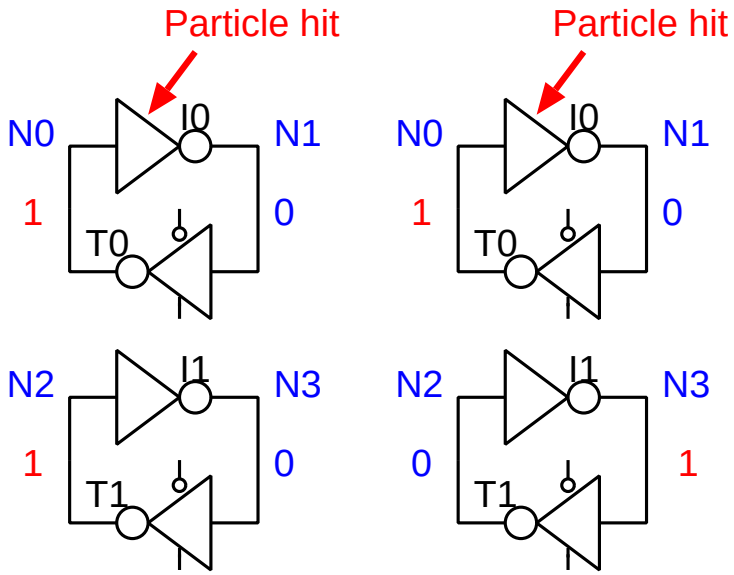
(a) Q=30 fC (b) Q=80 fC

Figure 3.14: State of N1 and N3 vs. Q when two latches store opposite values (N1=1, N3=0).

3.4.3 Diagonal Particle Hit Case

On the perpendicular particle hit in the previous section, one of two latches is affected by collected charge and the bipolar effect, while the other is mainly affected by the bipolar effect. We investigate the vulnerability of two redundant latches by changing the angles of particle hits as in Fig. 3.18.

The angles of particle hits are set to 30 degree in all three cases. Fig. 3.19(a)-(c) show the results when the two latches store the same value (N1=1). In the case of I0 to I1, the vulnerable region becomes wider mainly due to lower Q_{critN3}. The critical charge of N3 Q_{critN3} becomes lower since the diagonal hits promote the parasitic bipolar effect



(a) two latches storing the same value

(b) two latches storing opposite values

Figure 3.15: Circuit structure of two latches which set "0" to node N1.

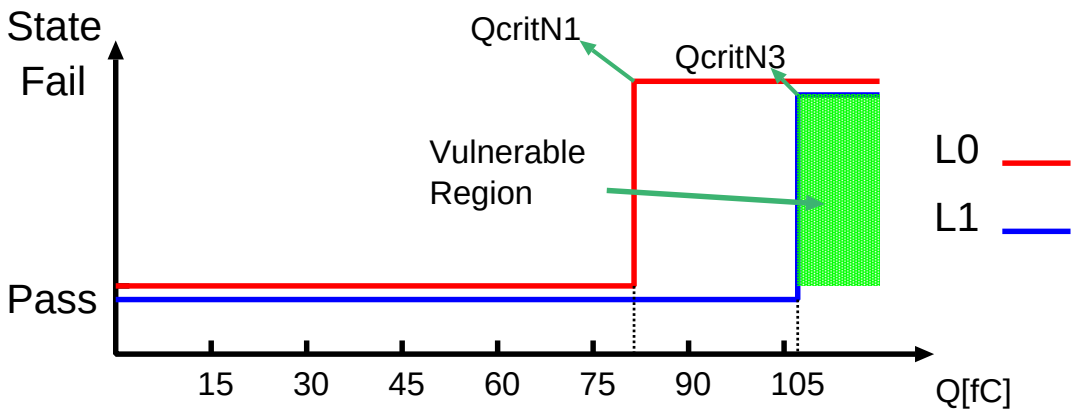
on I1. This is the weakest case when storing the same value. However, the vulnerable region becomes narrower when a particle passes from I0 to T1. It is mainly due to lower Q_{maxN1}. The bipolar transistor on T0 turns on by a lower-energy particle because it passes much closer to T0. When a particle passes I0 to T0, there is no vulnerable region because of lower Q_{maxN1} and higher Q_{critN3}. In contrast, there is no vulnerable region in the structure storing the opposite values in any particle direction. Table. 3.1 and 3.2 summarise the collected charge of N1 and N3 in both cases of the perpendicular and diagonal particle hits.

3.4.4 Soft Error Rate Calculation

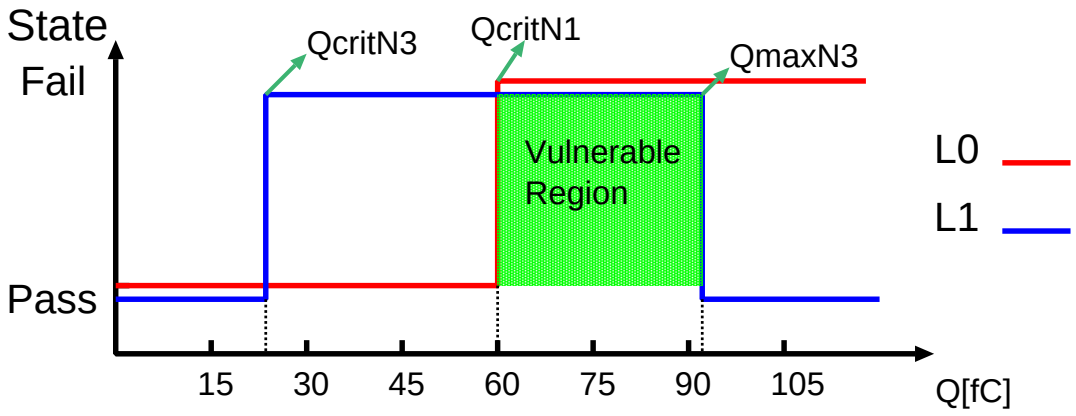
Eq. (4.1) [47] is used to calculate SER in FIT (Failure In Time, error numbers/10^9 h).

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) \quad = \quad F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \tag{3.1}$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors, and K is a fitting parameter. Q_{s} is called "charge collection efficiency" that is correspond to the sensitivity of the critical charge. Q_{s} strongly depends on doping



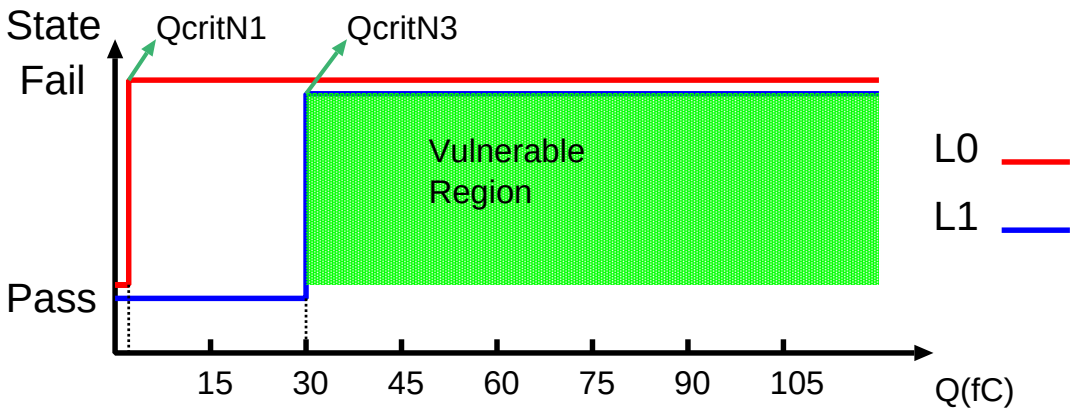
(a) two latches storing the same value



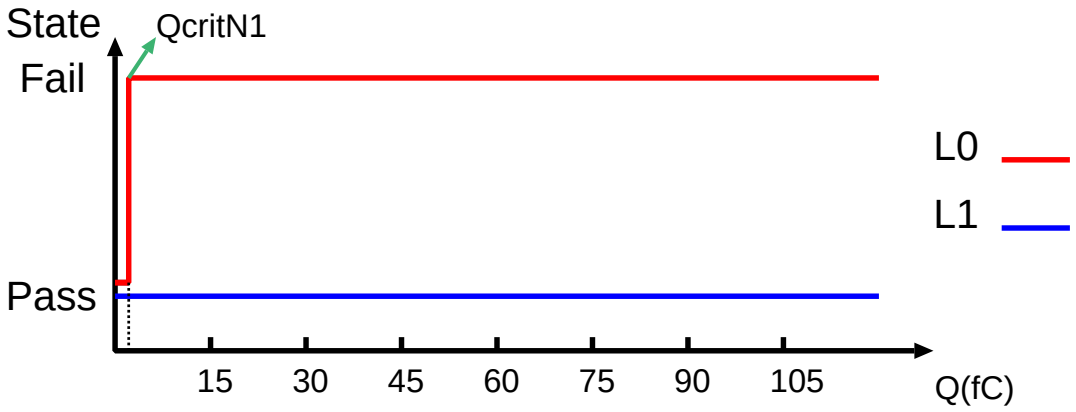
(b) two latches storing opposite values

Figure 3.16: State of N1 and N3 vs. Q (N1=0)

and supply voltage [18]. We use the parameter values as in Table 4.2 that are scaled from 100 nm [47] to 65 nm.



(a) two latches store the same value (N1=N3=0)



(b) two latches store opposite values (N1=0, N3=1)

Figure 3.17: State of N1 and N3 vs. Q (particle hit on the tristate inverter).

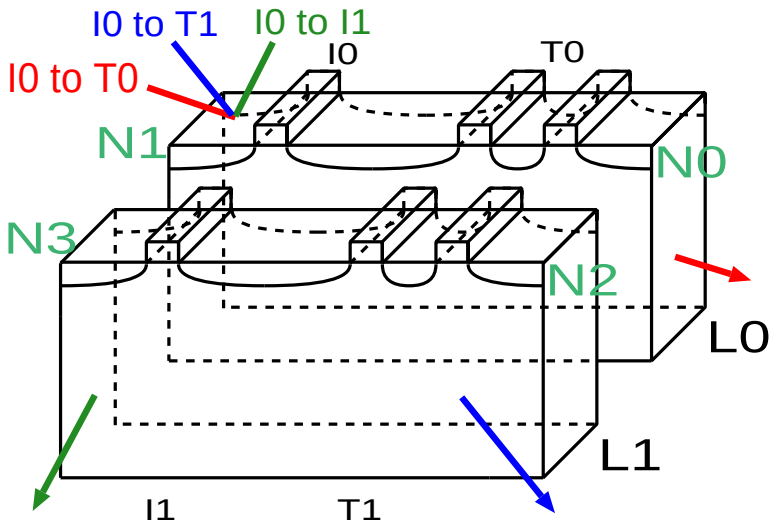
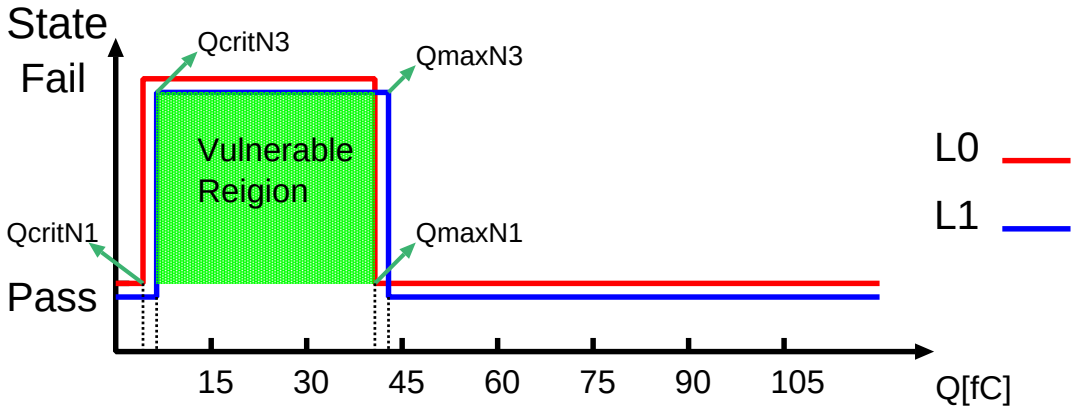
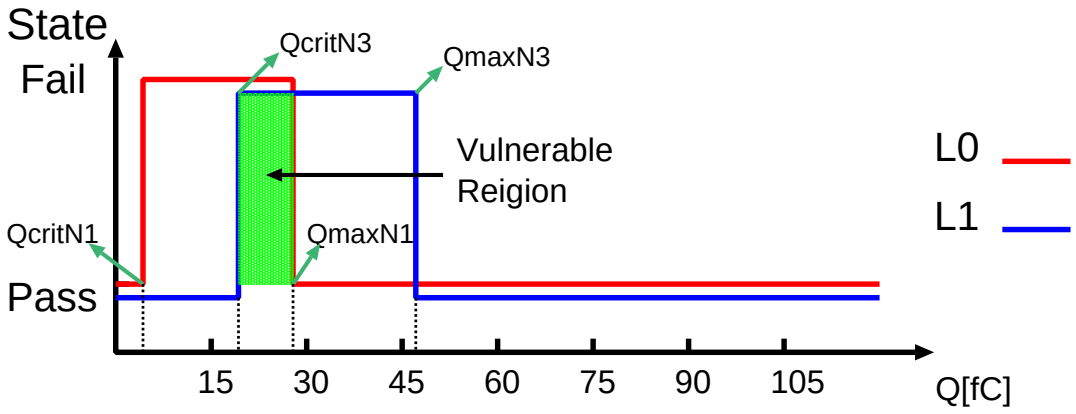


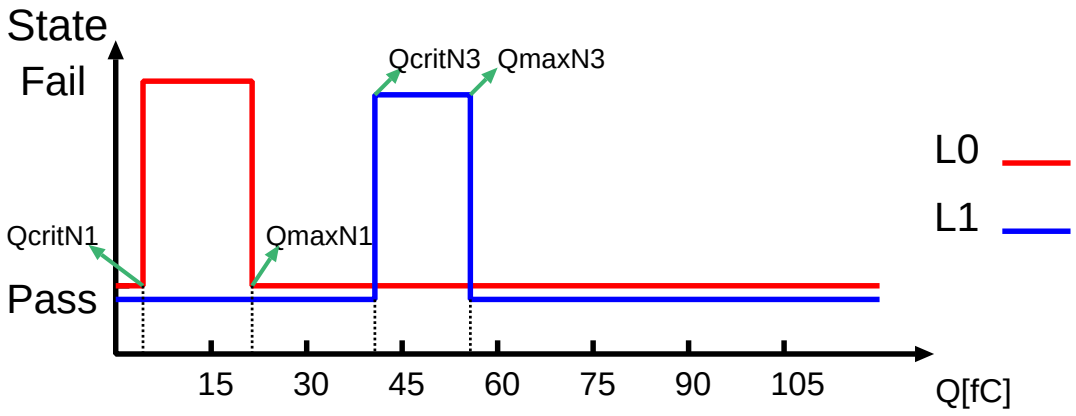
Figure 3.18: Diagonal particle hits on I0 to I1, T1 and T0.



(a) I0 to I1 case



(b) I0 to T1 case



(c) I0 to T0 case

Figure 3.19: State of N1 and N3 according to collected charge "Q" when a particle hit diagonally on two latches which store the same value.

Table 3.1: Collected charge "Q" (fC) in the latches which store the same value (Diagonal particle hit case).

	Q_{critN1}	Q_{maxN1}	Q_{critN3}	Q_{maxN3}
I0 to I1	5.2	41.8	5.5	44.0
I0 to T1	5.2	29.0	18.4	46.6
I0 to T0	5.2	22.6	40.8	53.0

Table 3.2: Collected charge "Q" (fC) in the latches which store opposite values (Diagonal particle hit case).

	Q_{critN1}	Q_{maxN1}	Q_{critN3}
I0 to I1	5.2	41.8	57.5
I0 to T1	5.2	29.0	69.7
I0 to T0	5.2	22.6	79.5

Table 3.3: Parameters for SER estimation

F ($\mathrm{cm}^{-2}\mathrm{s}^{-1}$)	5.65e-3
$\mathrm{Q_s}$ (fC)	5.72
K	2.2e-5

Table 3.4: Qcrit and MCU rates from device simulations.

Latch state (N1/N3)	Q_{crit}	SER
Store the same value (1/1)	22.5 fC	1.48 FIT/Mbit
Store opposite values (1/0)	60.2 fC	2.10e-3 FIT/Mbit

Table 3.5: Qcrit and SEU rates from device simulations as shown in Fig. 3.11.

Particle hit on	Q_{crit}	SER
Inverter	5.2 fC	30.5 FIT/Mbit
Tristate inverter	4.2 fC	36.3 FIT/Mbit

MCU rates are calculated by the minimum charge which two latches flipped at the same time as shown in Table 3.4. SEU rates are calculated by the minimum value of "Q" at which only one latch is flipped. The SEU rates of the inverter and the tristate inverter are shown in the Table 3.5. Note that the device simulations results in which perpendicular particle hit on the latches is used to calculate the error rates. MCU rates of the structure in which two latches store opposite values are roughly 1,000 times lower than those of the same values.

3.5 Experimental Results by Neutron Irradiation

A test chip was fabricated in a 65 nm bulk CMOS process including a general D-FF array to show vulnerabilities of FFs by the parasitic bipolar effect. Figure 3.20 show the layout structure of the FF array [48] which consists of a D-FF in Fig. 3.21. Spallation neutron-beam irradiation was carried out at RCNP of Osaka University. Clock is fixed to 0 or 1 to keep master or slave latches in the latch state. Table 5.2 show the numbers of SEUs and MCUs when both latches store the same value and opposite values, respectively. Table 3.7 show the MCUs/SEUs ratio according to the states of two lathes. Accrding to the results of device simulations, the MCU rates of the structure in which two latches store opposite values are roughly 1,000 times lower than those of the same values. The MCUs/SEUs ratio of the experimental results is 10x bigger that of the device simulations.

3.6 Chapter Summry

The simulation results show that two redundant latches store opposite values suppress a simultaneous flip by a particle hit effectively due to the parasitic bipolar effect. In contrast, redundant latches store the same value are very sensitive to MCUs. From device-level simulations, both latches store the same value are flipped between a certain range of generated charge which is called a vulnerable region. Because of the asymmetric

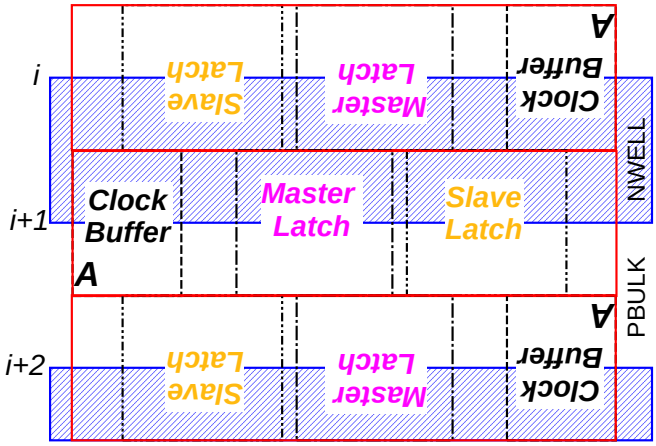


Figure 3.20: Floorplan of the general D-FF array to measure MCUs/SEUs rates.

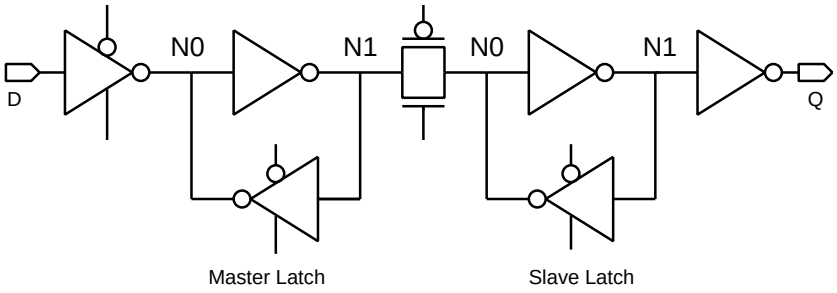


Figure 3.21: Schematic of D-FF.

structure of latches, they become a specific state when the parasitic bipolar transistors turn on by a particle hit. When storing opposite values in two latches, both latches become the same state by a particle hit. But it does not change the output of the redundant FFs because one of these two latches stores the correct value. Even if there is also MCU occurrence in the latter, the probability is very low because it needs more than 107 fC collected charge. Experimental results on a D-FF array fabricated in a 65 nm CMOS prove that the MCU rates are about 1,000 times lower when latches store opposite values. The ratio of MCUs/SEUs from the device simulations is lower than the results of experiments. However, the MCU rates of the structure in which two latches store opposite much lower in device simulations and experimental results.

The high MCU tolerant layout structures are proposed in this next Chapter.

The parasitic bipolar effect is one of dominant factors of MCUs to decrease the reliability of redundant FFs. But the simple circuit-level technique to store the opposite

Table 3.6: The numbers of SEUs and MCUs from experimental results.

Latch state (N1/N3)	N_{SEU}	N_{MCU}
Store the same value (1/1)	483	155
Store opposite values (1/0)	138	1

Table 3.7: MCUs/SEUs ratio from experimental results and device simulations.

States of two latches (N1/N3)	Experimental	Device Simulation
Store the same value (1/1)	0.3	0.05
Store opposite values (1/0)	0.7e-2	6.5e-5

values enhances the tolerance to MCUs without any area, power and delay overhead.

Chapter 4

Dependence of Layout structures on MCU Rate by Device Simulations and Neutron Experiments in 65-nm Bulk Redundant Flip-Flops

Technology scaling increases the role of charge sharing and bipolar effect with respect to multiple cell upset. In this chapter, we analyze the contributions of layout structures to suppress MCU by device-level simulations and neutron experiments. Device simulation results reveal that the ratio of MCU to SEU exponentially decreases by increasing the distance between redundant latches. MCU is suppressed when well contacts are placed between redundant latches. Experimental results also show that the ratio of MCU to SEU exponentially decreases by increasing the distance between cells. MCU is suppressed effectively by increasing the density of well contacts.

4.1 Introduction

Radiation-induced charge collection at a single sensitive node, such as the drain region of a single transistor, is a possible source of SEU. Radiation-hardened circuits, for instance Triple Modular Redundancy (TMR), Built-in Soft Error Resilience (BISER)[49], Dual Interlocked Storage Cell (DICE)[19], and Error Correction Code (ECC) have been employed to mitigate an SEU. As device dimensions are scaled down, multiple node charge collection has an increasing impact on the response of the circuit[50]. Soft errors have become an increasingly troublesome issue for memories as well as sequential logic

circuits.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hit on latches or flip-flops. It makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs)[26].

MCU rate depends on cell distance and well-contact density. In order to reduce radiation-induced multiple errors, each vulnerable transistor is placed on different p-well regions or separated over 1.1 μm[21, 22]. The parasitic bipolar effect and the charge sharing also affect SEU[42] and Single Event Transient (SET) pulse widths[51]. Several device simulations results show that charge sharing can be suppressed by high well contact density, or separating the distance between transistors in a 130 nm process [52, 17] and a 90 nm process [53]. However, the experimental results of these references do not clearly show the relationship between soft error rates and the distance between transistors. The results of a 65 nm process has not been presented either. To estimate soft-error rates and increase its resilience, it is necessary to measure characteristics of radiation-induced MCU.

In this chapter, the impact of cell distance and well-contact density on redundant flip-flops is analyzed by device-level simulations [54] and neutron experiments [55]. All device-level models are constructed in a 65-nm process. Test chips are fabricated in a 65-nm bulk CMOS process and accelerated tests are carried out at Research Center for Nuclear Physics (RCNP).

This chapter is organized as follows. Section 4.3 shows the impact of cell distance and well-contact density on redundant latches in device-level by device-level simulations. The results by neutron experiments are shown in Section 4.4. We compare the simulations and experimental results in Section 4.5. Section 5.5 sammarizes this chapter.

4.2 Radiation-hard Layout Structures of Bulk Transistors

4.2.1 Three Layout Structures

Fig. 4.1 shows a circuit including two latches placed on two adjacent rows in a 65nm bulk technology. Figs. 4.2-4.4 show three layout structures of the circuit. Structure

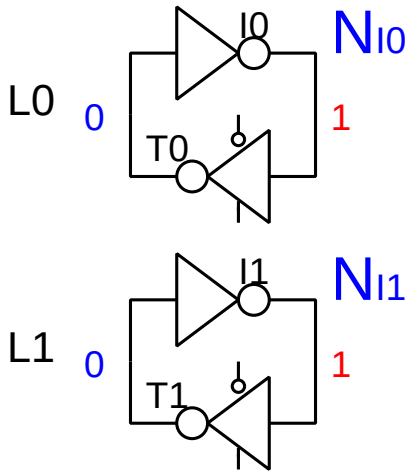


Figure 4.1: Redundant latches.

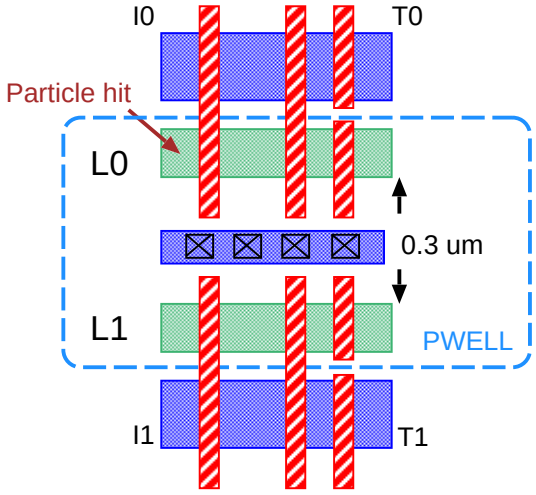


Figure 4.2: layout structure A: well contacts are placed between latches.

A is a layout in which well contacts are placed between latches (Fig. 4.2). Structure B (Fig. 4.3) is a layout in which well contacts are placed beside latches with P+ tap between latches. Structure C (Fig. 4.4) is a layout in which well contacts are placed beside latches without any tap between redundant latches. In this section, the tolerance of these layout structures to soft errors are compared by TCAD simulations. In the layout structures B and C, the distance between latches and well contacts is defined as D_{WC}.

4.2.2 Simulation Setups

A device simulator Sentaurus is used to do all TCAD simulations. A radiation particle penetrates the NMOS transistor of the inverter I0 perpendicularly. All of the NMOS transistors are placed in the same P-well. The output nodes (N_{I0}, N_{I1}) of the inverter I0 and I1 are initially set to "1". Output voltage of inverter is decreased by charge collection and bipolar effects when a particle hits NMOS of the inverter. Thus, the redundant latches become very sensitive to a particle hit. It is order to analyze the tolerance of each layout structure to MCU. We create a 3D device-level NMOS model as shown in Fig. 4.5 based on the circuit and layout structures. It is a triple well structure. The distance between the redundant latches L0 and L1 is 0.3 μm as shown in Fig 4.5. All device-level models are fabricated based on a 65 nm process.

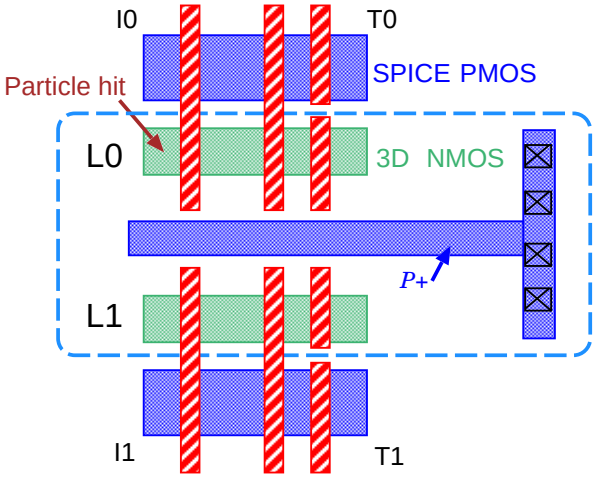


Figure 4.3: Layout structure B: well contacts are placed beside latches with P+ tap between latches.

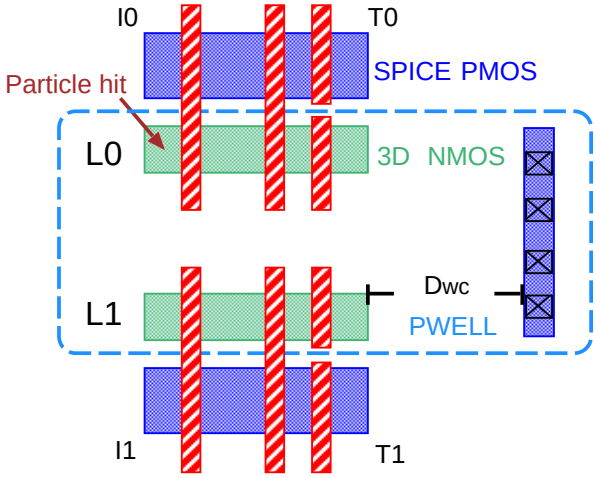


Figure 4.4: Layout structure C: well contacts are placed beside latches without any tap.

4.2.3 Comparison of the Tolerance by Layout Structures

Fig. 4.20 shows two pairs of voltage outputs when a particle penetrates latch L0 of the layout structure A with LET=10 and 20 MeV/mg/cm^2. As the particle penetrates, the output N_{I0} of latch L0 upsets while the output N_{I1} does not upset as shown in Fig. 4.6(a) and (b). In this case, generated charge under the latch L0 can not cross over the well contacts to the L1 side. Thus the charge sharing between L0 and L1 is almost prevented. The bipolar effects[27] is also suppressed effectively, because the well contacts suppress the well potential elevation.

Fig. 4.7 shows another two pairs of voltage outputs when a particle penetrates latch L0 in the layout structure B with LET=10 and 20 MeV/mg/cm^2. The output N_{I0} of latch L0 upset while the output N_{I1} does not flip when LET=10 MeV/mg/cm^2 as shown in Fig. 4.7(a). However, when LET is increased to 20 MeV/mg/cm^2, node N_{I0} and N_{I1} are flipped simultaneously as shown in Fig. 4.7(b), MCU occurs in the layout structure B by a higher energy particle.

When the redundant latches are constructed in the stucture C, the voltage outputs by the paticle are shown in Fig. 4.8. The well contacts is placed beside latches in the structure C. It cannot suppresses well potential elevation effectively. The charge sharing and bipolar effects appear in the structure C. Thus, both latches upset simultaneously when LET=10 and 20 MeV/mg/cm^2 as shown in Fig. 4.8(a) and 4.8(b). Table 4.1

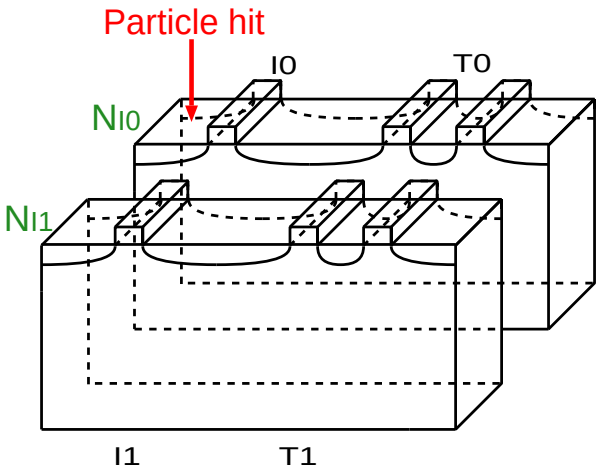


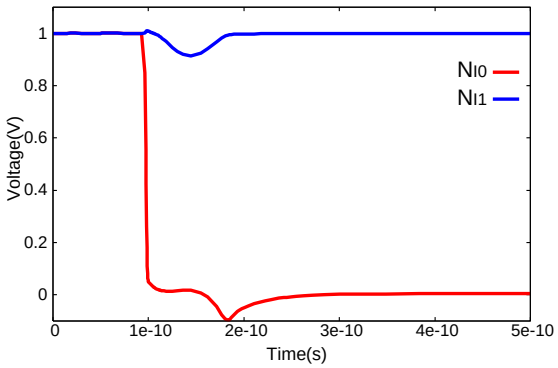
Figure 4.5: 3D device-level structure of redundant latches in two rows. A particle penetrate at the drain of NMOS I0.

Table 4.1: The threshold LET of the three kinds of layout structures.

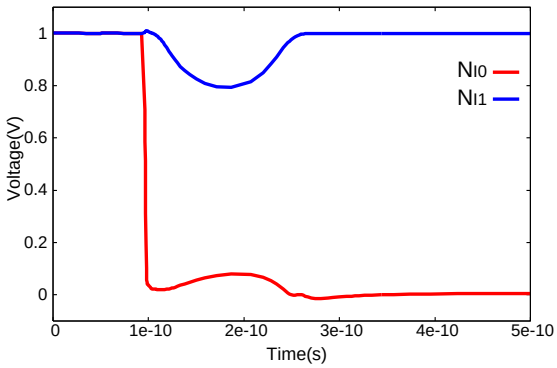
Layout structure	LET of SEU	LET of MCU
A	7.0	35.0
B	6.3	18.5 (52.86% of A)
C	5.2	8.3 (23.71% of A)

shows the threshold LET of the three layout structures. The threshold LET of MCU on the structures B and C are decreased by 52.86% and 23.71% compared with that on A respectively.

Fig. 4.9 shows the threshold LET of the particle which upsets the redundant latches simultaneously according to D_{WC}. The threshold LET exponentially decreases when the distance between well contact and the redundant latches, D_{WC} is increased. The LET of the structure B is bigger than that of C. The LET of the structure C reduces steeper than structure B when D_{WC} is increased. It is because that the p+ tap between latches stabilizes the well potential of structure B. The well potential of B do not change lot by a particle. The well potential of C is stabilized when well contacts are placed close to latches. It makes structure C stronger to particle. However, the tolerance of structure C becomes weaker when well contacts are placed far away from latches.

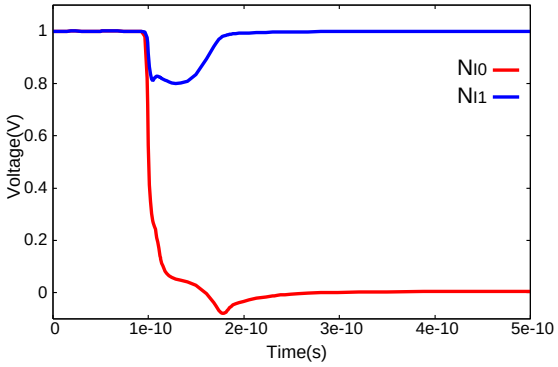


(a) LET=10 MeV/mg/cm^2

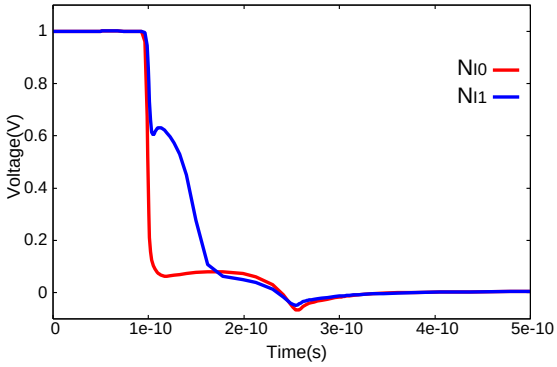


(b) LET=20 MeV/mg/cm^2

Figure 4.6: The voltage outputs of redundant latches in layout structure A by a particle.

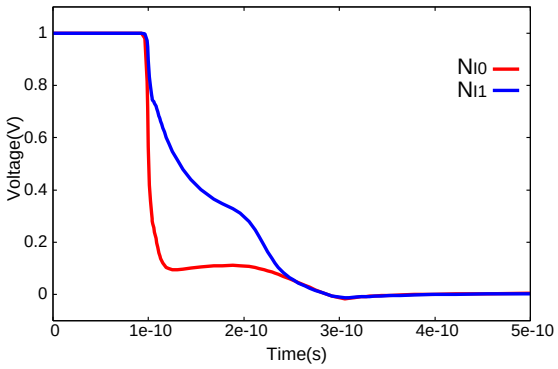


(a) LET=10 MeV/mg/cm^2

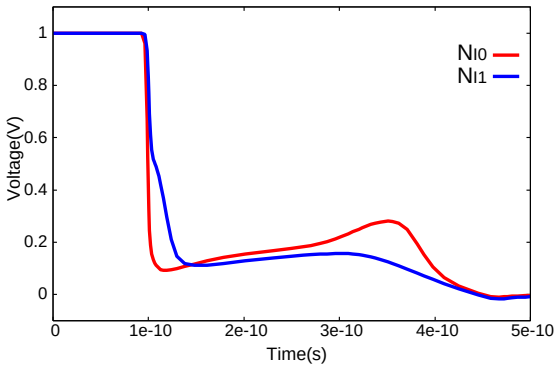


(b) LET=20 MeV/mg/cm^2

Figure 4.7: The voltage outputs of redundant latches in layout structure B by a particle.



(a) LET=10 MeV/mg/cm^2



(b) LET=20 MeV/mg/cm^2

Figure 4.8: The voltage outputs of redundant latches in layout structure C by a particle.

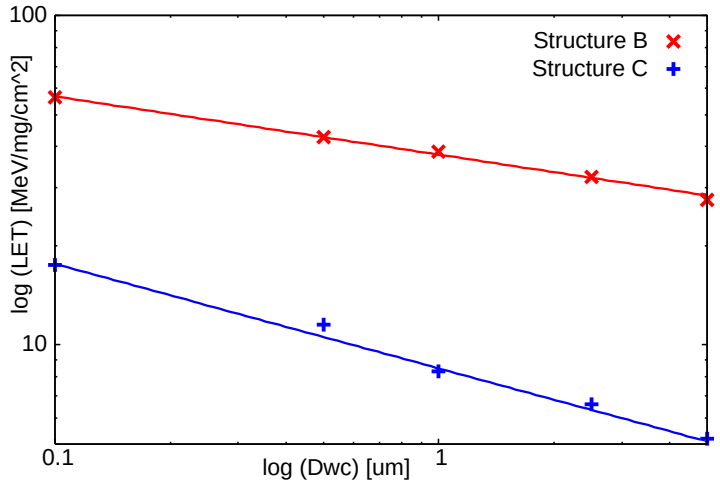


Figure 4.9: LET of paticles which upset redundant latches simultaneously accroding to D_{WC}.

4.3 Impact of Cell Distance and Well-contact Density by Device-level simulations

4.3.1 Device-level Simulation Setup

In order to analyze the MCU tolerance of redundant latches, we examined several device-simulations by using the circuit as shown in Fig. 4.10. The circuit including two unconnected independent latches placed in two adjacent rows in a 65 nm bulk technology called redundant latches. They are regarded as two latches in a TMR structure. We assume that a radiation particle hits the tristate inverter T0 of the NMOS transistor of latch L0 in the odd row. The tristate inverter T1 can also be flipped by charge sharing and bipolar effect between T0 and T1. The layout structure of the redundant latches in two rows is shown in Fig. 4.11. All of the NMOS transistors are placed in the same P-well. Well contacts are placed side by side in the same well. The output nodes (N_{T0}, N_{T1}) of the tristate inverters T0 and T1 are initially set to "1". Output voltage of the tri-satate inverter is decreased by particle hits on the NMOS of the tristate inverter. The redundant latches are simultaneously flipped by charge sharing and bipolar effect.

Based on the circuit and layout structures, we construct a 3D device-level NMOS model as shown in Fig. 4.12. It is constructed in a triple well structure. The distance between the well contacts and latches is defined as D_{WC}. D is the distance between redundant latches L0 and L1. D is 0.3 μm when the redundant latches are aligned vertically as shown in Fig. 4.12. A Gaussian heavy-ion model is used in device simulations. The ion hits T0 at 0.1 ns from the beginning of simulation.

4.3.2 Contribution of Cell Distance D to Suppress MCUs

Fig. 4.13 shows the magnitude of collected charge of L0 and L1 when D is increased. D_{WC} is 20 μm. LET values of the ion particle are 10 and 20 MeV·cm^2/mg. The collected charge of L0 increases gradually while the collected charge of L1 decreases by increasing D as shown in Fig. 4.13. Less charge is collected into L1 as a function of D. Therefore, the charge sharing becomes weak between redundant latches by longer D. The collected charge of L0 become dominant. It is because less charge is shared by L1.

Fig. 4.14 shows the drain current of tristate inverters T0 and T1 when the redundant latches are simultaneously flipped. D_{WC} is 20 μm. D is 0.5, 3.0 and 5.0 μm. The

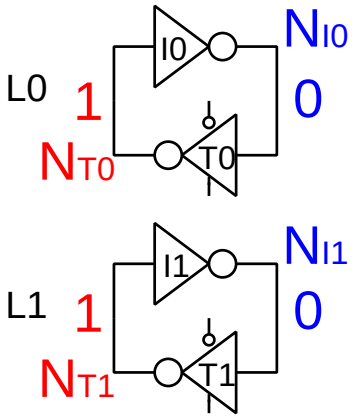


Figure 4.10: Redundant latches Two unconnected independent latches).

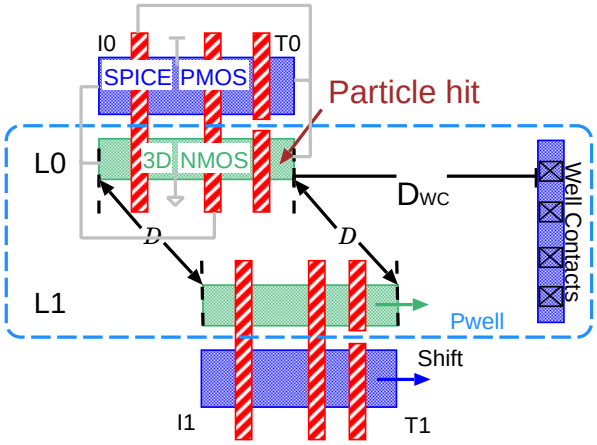


Figure 4.11: Layout of two latches in two rows.

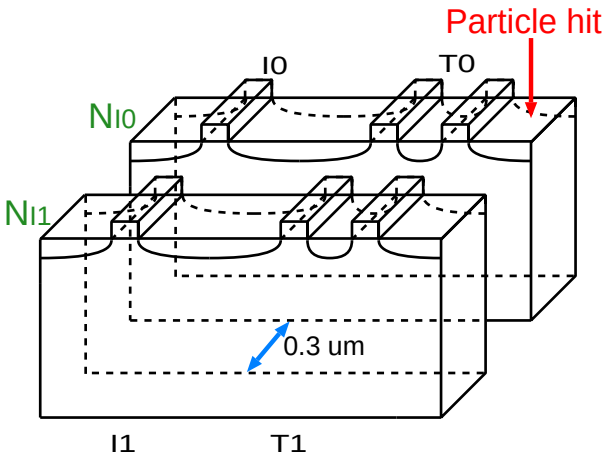
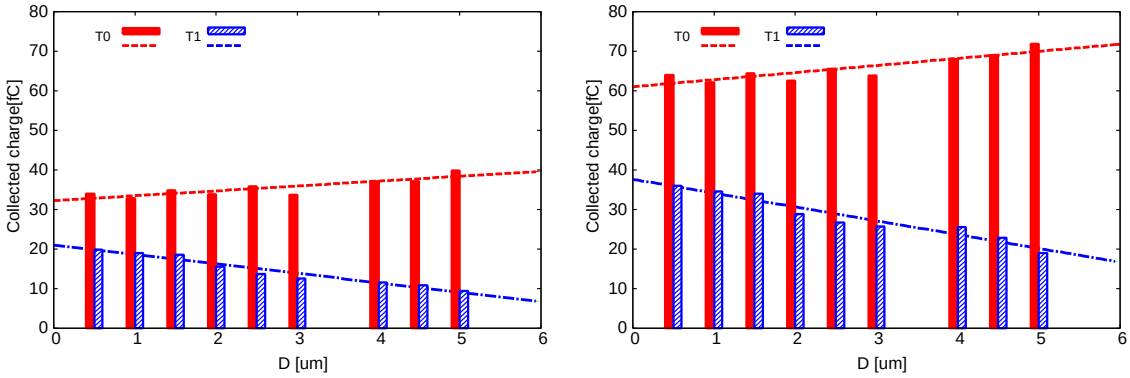


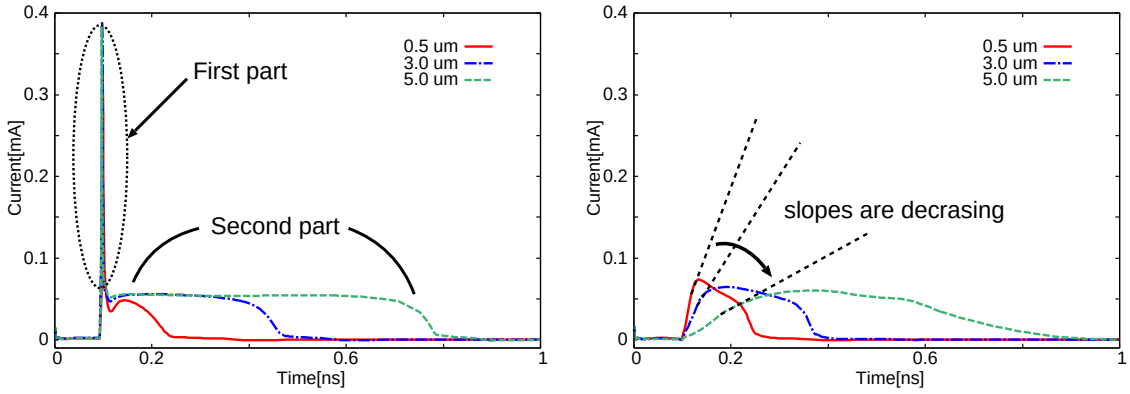
Figure 4.12: 3D device-level structure of redundant latches in two rows. A particle hit at the tristate inverter T0.

waveform of T0 can be divided to two parts as shown in Fig. 4.14(a). The first part is very steep, that can be modeled by a single or double exponential model, while the second part is shallow. From the simulation results, we can obviously recognize that there are two mechanisms that occur in the whole charge collection. After the particle hit, a large amount of electrons are collected in the drain region immediately. The first part appears as a steep current by the drift. After that, holes still remain in the bulk region, which reduces the source-well potential barrier due to the increase in the potential of the P-well. The source injects electrons into the channel which can be collected to the drain. This effect is called the parasitic bipolar effect because the source-well-drain of an NMOS transistor acts as an n-p-n bipolar transistor. The shallow current waveform



(a) LET=10 MeV·cm^2/mg (b) LET=20 MeV·cm^2/mg

Figure 4.13: Collected charge to L0 and L1 by increasing D. D_{WC}=20 μm.



(a) Drain current waveform of T0 (b) Drain current waveform of T1

Figure 4.14: Transient drain current of T0 (a) and T1 (b) caused by a particle hit at T0 when the redundant latches are simultaneously flipped. D is 0.5, 3.0, 5.0 μm

in the latter part is caused by the parasitic bipolar effect.

As D is increased from 0.5um to 5.0 um, the first parts do not change a lot while the shallow parts become wider as shown in Fig 4.14(a). Fig. 4.14(b) shows the current waveforms of T1. The slopes are decreasing by increasing D. The current waveforms do not go to the peak volume immediately. The area of generated charge by a particle hit is large. The charge is both collected into L0 and L1 at the same time by drift if L0 and L1 are too close. It makes the current waveform of L1 increase to the peak volume immediately. The charge collection of L1 by drift becomes weaker if D is increased. However, the waveforms become wider. The current waveforms of L1 is less dq/dt because of the charge collected into L1 mainly by PBE. It becomes easier to flip redundant

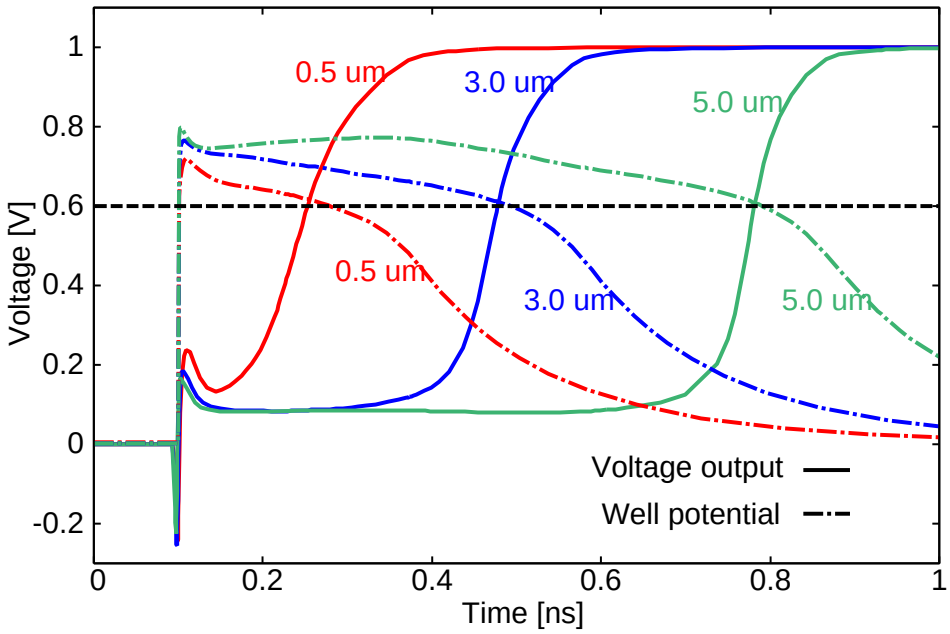


Figure 4.15: Voltage outputs of inverter I0 of latch L0 and the well potential under the latch L0 after a particle. D is 0.5, 3.0, 5.0 μm.
latches simultaneously by the charge sharing than PBE in the 65 nm bluk process.

Fig. 5.15 shows the voltage waveforms of inverter I0 of latch L0 and the well potential under L0 after a particle hit on the tristate inverter T0. D is 0.5, 3.0 and 5.0 μm. The voltage waveforms keep low when the well potential is higher than 0.6 V. The voltage waveforms start to go up when well potential decreases below 0.6 V. The flipped voltage waveforms cross the well potential waveforms at 0.6 V. It is because the parasitic bipolar transistor of latch L0 can not turn off until the well potential decreases below 0.6V.

Fig. 4.16 shows the minimum magnitude of critical charge of the latches L0 and L1 when the redundant latches are simultaneously flipped. We call it the threshold charge. The magnitude of the threshold charge becomes bigger when D is increased. As D is increased, charge sharing between L0 and L1 becomes weaker as shown in Fig. 4.14. Charge is mainly collected into L1 by the bipolar effect. However, it becomes harder to elevate the well potential under L1 because the latch L1 is placed far away from L0 ($D \gg 0.3$ μm). Thus, LET of the ion particle which simultaneously flips the redundant latches becomes higher. Threshold charge are increased in L0 and L1 by increasing D. Note that just the collected charge of tristate inverter T0 and T1 is shown in Fig. 7. Larger amount of charge is also collected into inverter I0 and I1. Thus, the charge of T1 is larger than T0 when D is 0.5 μm. But it does not influence the results of the device

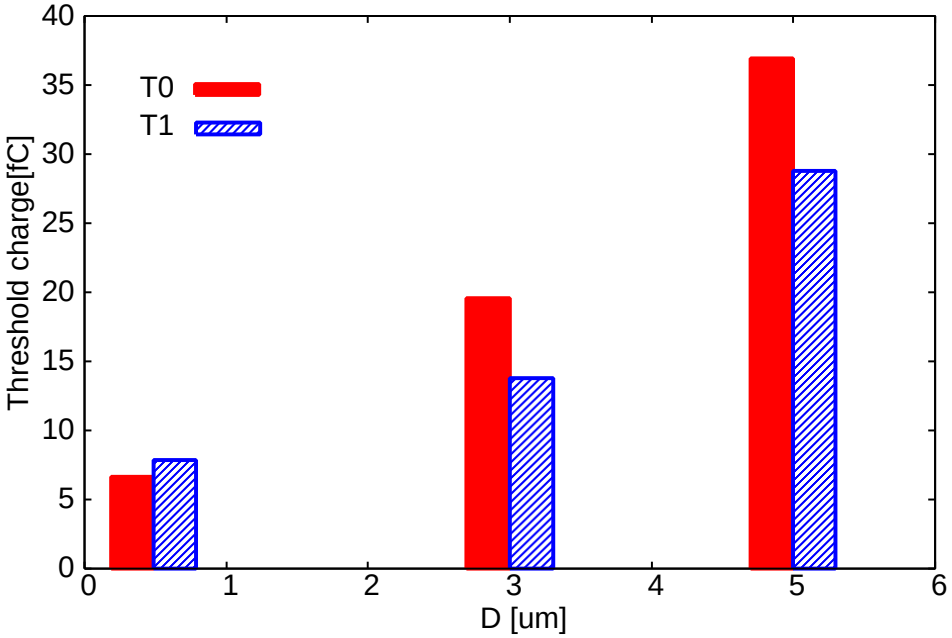


Figure 4.16: Threshold charge of L0 and L1 when the redundant latches are simultaneously flipped. D is 0.5, 3.0, 5.0 μm.
simulations.

4.3.3 Contribution of Well-contact locations to Suppress MCUs

In order to analyze the relationship between well-contact position and MCU tolerance, we place the well contacts adjacent to latches, D_{WC} is shorten to 1.0 μm from 20 μm. LET of the ion particle are 10 and 20 MeV·cm^2/mg. The redundant latches are aligned vertically (D = 0.3 μm) in these simulations. The volume of collected charge of L0 and L1 are shown in Fig. 5.2. When the distance D_{WC} is shortened from 20 μm to 1.0 μm, the magnitude of collected charge of the redundant latches L0 and L1 decreases by 50%. It is because the well potential under latches keeps steady by placing well contacts close to the latches. Bipolar effect under L0 and L1 is suppressed. Thus, less charge is collected into the redundant latches.

Fig. 4.18 shows the threshold charge of L0 influenced by D_{WC}, when redundant latches are simultaneously flipped. D is 1.0, 2.0 and 3.0 μm. The threshold charge exponentially decreases by increasing D_{WC}. There is a large amount of charge collected into the latch L0 when redundant latches are simultaneously flipped if the well contacts are placed adjacent to redundant latches. It is because the adjacent well contacts

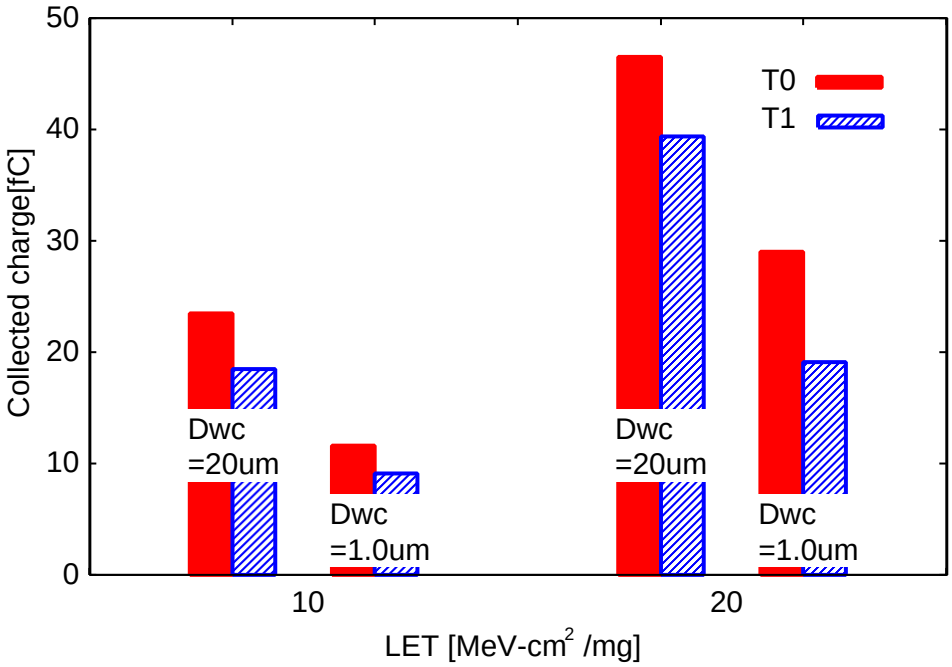


Figure 4.17: Collected charge of the redundant latches L0 and L1 influenced by D_{WC}. LET is 10 and 20 MeV·cm^2/mg.

stabilize the well potential. The bipolar effect is also suppressed. A higher LET ion particle can flip the redundant latches simultaneously. Therefore, MCU tolerance of the redundant latches become stronger by shortened D_{WC}.

When the well contacts are placed between the redundant latches L0 and L1 as shown in Fig. 4.19, the magnitude of collected charge is shown in Fig. 4.20. The collected charge of L0 and L1 decreases by about 60% and 90% respectively compared to the collected charge when D_{WC} is 20 μm, even if the redundant latches are aligned vertically. In this case, generated charge under the latch L0 can not cross over the well contacts to the L1 side. Thus the charge sharing between the redundant latches is almost prevented. Also the bipolar effect is suppressed effectively, because the well contacts between the redundant latches suppress the well potential elevation.

4.3.4 Soft Error Rate Calculation

Eq. (4.1) [18] is used to calculate SER in FIT (Failure In Time, number of errors/10^9 hours).

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) \quad = \quad F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \tag{4.1}$$

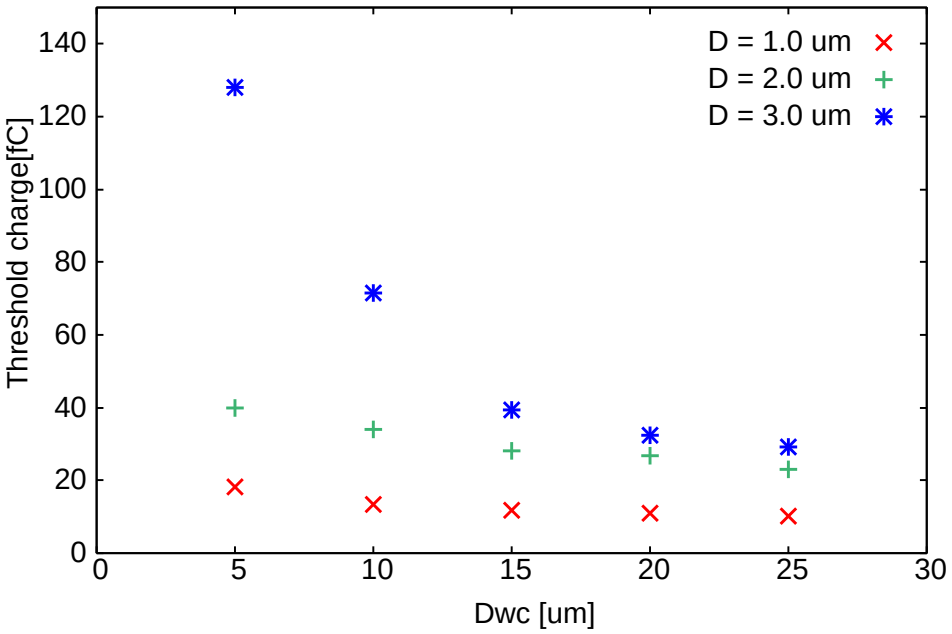


Figure 4.18: Threshold charge of L0 by increasing D_{WC} when redundant latches are simultaneously flipped.

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_{s} is called "charge collection efficiency" that strongly depends on doping and supply voltage[47]. We use the parameter values as in Table 4.2. We use a fitting line to scaled Q_{s} based on the Q_{s} of 350 nm and 100 nm as [18] to 65 nm.

MCU rate is calculated by the threshold (minimum) charge of latch L0 at which the redundant latches are simultaneously flipped. D_{WC} is the distance between the redundant latches and well contacts as in Fig. 4.11. The distances between redundant latches D which we use for device simulations are shown in Table 4.3. D_{WC} is 20 μm. The threshold charge Q_{crit} and the ratios of MCU to SEU are also shown in Table 4.3. Fig. 4.21 shows the ratio of MCU to SEU influenced by D on redundant latches from device simulations when D_{WC} is set to 20 μm. Note that the ratio of MCU to SEU which is lower than 0.1% are not shown on Fig. 4.21. According to the device-simulation results as shown in Table 4.3, the ratio of MCU to SEU exponentially decreases by increasing D. If the well contacts are placed between redundant latches, they are simultaneously flipped when LET is 35 MeV·cm^2/mg, and the threshold charge is 45.7 fC. The ratio of MCU to SEU decreases to 0.073%.

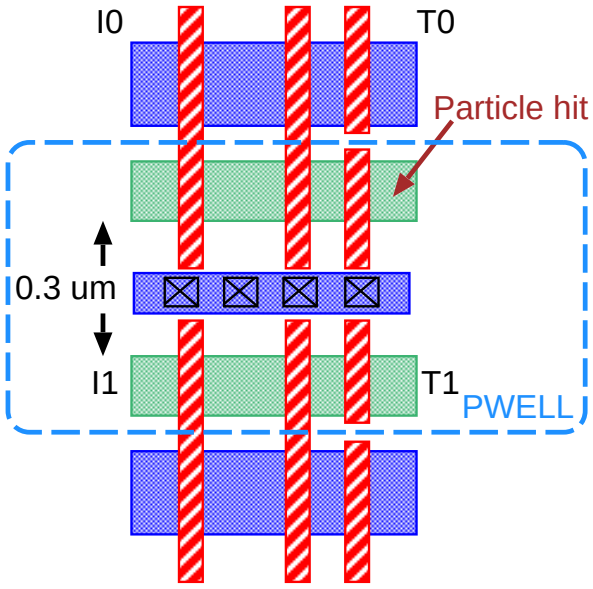


Figure 4.19: The layout structure in which well contacts are placed between the redundant latches.

4.4 Impacts of Cell Distances and Well-contact Densities on Redundant FFs by Neutron Experiments

The experimental results of neutron-induced MCU on D-FFs are described in this section. We use four different shift registers to estimate soft error rates on redundant flip-flops[55]. The dependence of MCU rates on the distance of FFs and well-contact density is also shown in this section.

4.4.1 Test Chips

In order to measure the soft error rates, we fabricated a 65 nm bulk CMOS test chip as shown in Fig 4.22. There are four different shift registers in the test chip. Each shift register includes 10k FFs. All shift registers are constructed by FFs and clock buffer chains [56]. These FFs are constructed in the same layout structure except for well contacts. The distance between two rows in registers (a)-(c) are 0 μm, 1 μm, and 2 μm as shown in Fig. 4.22. These shift registers are used to estimate the cell-distance independence MCU rates. Fig. 4.23 shows different distances between slave latches and between master latches according to flip-flop placements.

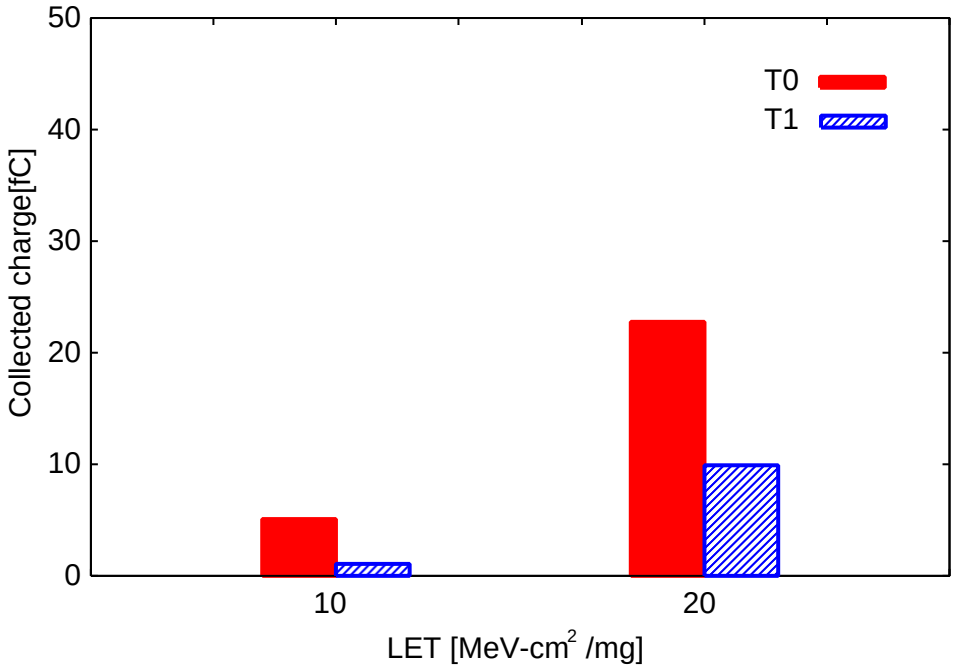


Figure 4.20: Collected charge of L0 and L1 when the well contacts are placed between the redundant latches.

The well contacts of the shift registers (a)-(c) are inserted every 50 μm. In order to obtain dependence of MCU rates on well-contact density, we fabricated well-contact arrays under the power and ground tap of the shift register (d) as shown in Fig. 4.22. The well-contact density is 60x higher than the others.

4.4.2 Experimental Results Analysis

The spallation neutron irradiation experiments were carried out at RCNP. In order to increase error counts, 28 chips is measured at the same time using stacked DUT boards. We use an engineering LSI tester to control DUTs and collect shifted error data. Fig. 4.24 shows the ratio of MCU to SEU according to the minimum distance by experiments. The ratio of MCU to SEU is reduced from 17.8% to 0.2% by inserting well-contact arrays under supply and ground rails of FFs, even if the minimum distance is the same. Therefore, we can improve soft-error resilience of the redundant FFs by increasing well contacts between redundant latches. It also shows that in the fabricated technology, almost all MCU is caused by the parasitic bipolar effect since it is caused by well-potential perturbation[57].

Table 4.2: Parameters for SER estimation

F (n·cm^{-2}s^{-1})	5.65×10^{-3}
Q_s (fC)	5.72
K	2.2×10^{-5}

Table 4.3: Qcrit and the ratio of MCU to SEU by device simulations when D_{WC} is 20 μm.

D	Q_{crit}	MCU/SEU [%]
0.5	8.31	50.18
0.6	9.95	37.70
1.0	11.3	29.70
1.5	17.2	10.59
2.0	26.9	1.94
2.5	30.9	0.97
3.0	32.4	0.74
4.0	51.5	0.026
4.5	61.5	0.0046
5.0	75.4	0.0004
Fig. 4.19	45.7	0.073

4.5 Comparison of Device-level Simulation Results and Experimental Results

FFs are placed every 5 μm on the measured chips. In order to get device-simulation result with higher accuracy, we use different (D_{WC}) as shown in Table 4.4 for calculating the ratio of MCU to SEU. Note that the ratios of MCU to SEU below 0.001% are not shown in the table. The distance-dependence of MCU / SEU by device simulations are shown in Fig. 4.25. Even if the ratios of MCU to SEU are different when we use different D_{WC} in device-simulations, all of the ratios decrease as shown in Fig 4.25.

We assume average values of all MCU / SEU for different D_{WC} in Table 4.4 from device-simulations is the MCU / SEU rate at each D. The average ratios of MCU to SEU are shown in Fig. 4.26. Fig. 4.27 shows the distance-dependence of MCU / SEU on FFs which is obtained from the shift registers (a)-(c). The ratio of MCU to SEU (y-axis) is obtained from measurement results. The ratio of MCU to SEU decreases influenced by $D^{-1.67}$ (D is the distance between redundant latches) and fitting line shows that it is

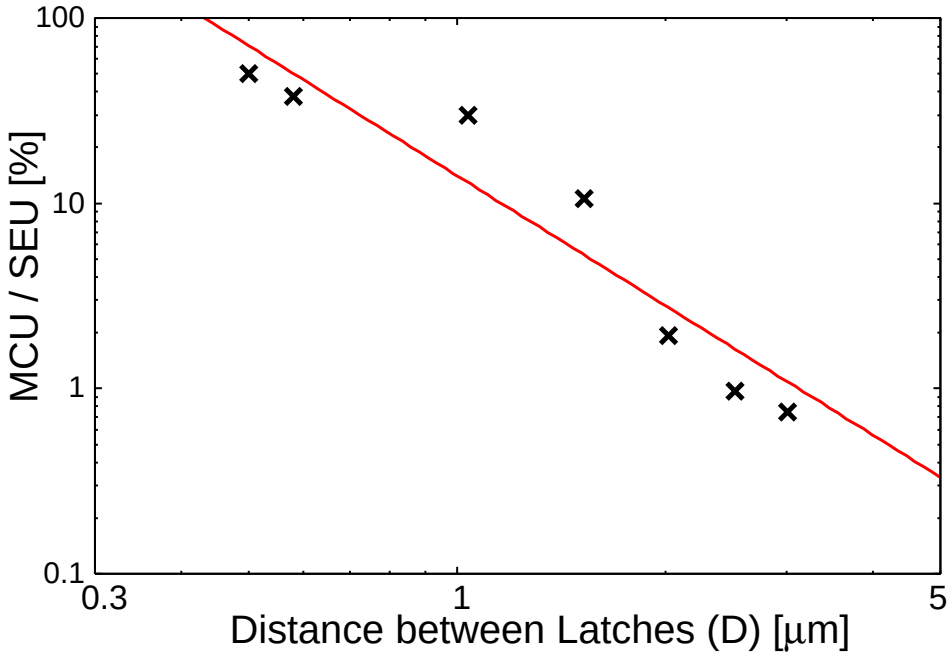


Figure 4.21: The ratio of MCU to SEU by increasing D when D_{WC}=20 μm.

almost 100% when $D < 0.3$ μm. The master and slave latches in the FF have different structures. However, the ratio of MCU to SEU by neutron experiments is distributed along the same straight line. Therefore, the MCU / SEU does not depend on the drive strength and load capacitance.

It is obviously shown that the ratios of MCU to SEU by device simulations and experimental results exponentially decrease by increasing the cell distance D. The fitting line decreases influenced by $D^{-2.07}$ by device simulations. Note that the fitting line is over 100%, it is means the ratio of MCU/SEU is 100% when D is shorter than 0.3 μm. According to the results of experiments and simulations, we must implement redundant FFs whose latches are separated by 4 μm from each other, in order to achieve 100x higher soft-error tolerance in redundant FFs than in non-redundant FF. It consumes huge area or complicated design procedures and these drawbacks become dominant by the process scaling.

Only one MCU is observed when the well contacts are placed between flip-flops by neutron experiments. Thus, MCU is suppressed by placing well-contact array under the supply and ground rail. However, the well potential is tightly connected to power or ground rails in this layout structure. This kind of structure can not be used if the well

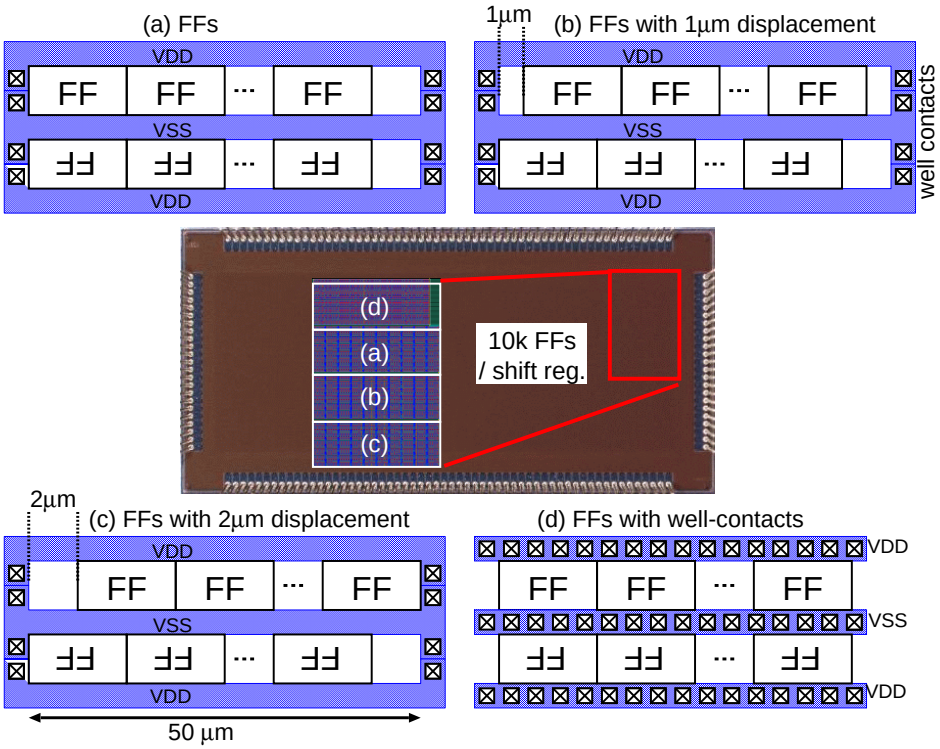


Figure 4.22: Chip micrograph and conceptual layout structures of four different shift registers on the test chip.

potential is changed to mitigate variations or to control performance and leakage.

There is only heavy ion model which is used in the device-simulations. Mostly, it is difficult to compare the results between device-simulations and neutron experiments. We examined device-simulations agree with the conditions of neutron experiments as possible as we can. The device-simulation results coincide with the experimental results very well in this work. We reveal that the MCU / SEU rates can be calculated by simple device-simulations.

4.6 Chapter Summry

Based on the results of device simulations, charge sharing and bipolar effect are two main factors when MCU occurs in redundant latches. MCU is suppressed when the distance between the redundant latches (D) is increased. Total collected charge of L0 and L1 decreases by 50% by placing the well contacts adjacent to the redundant latches

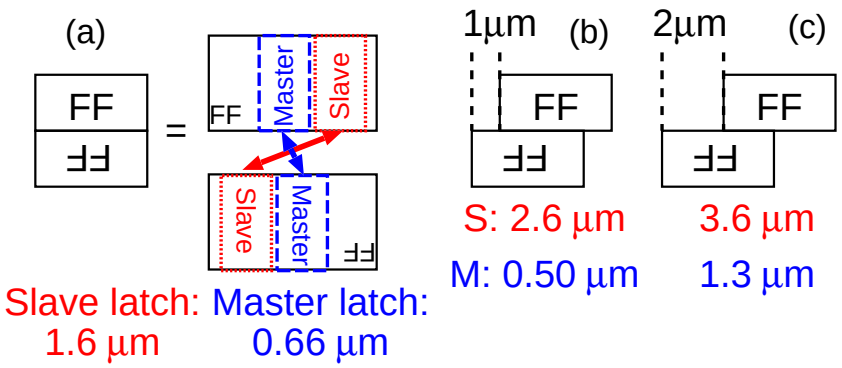


Figure 4.23: Distance between master or slave latches on shift register (a)-(c) in Fig. 4.22.

Table 4.4: The ratio of MCU to SEU influenced by D_{WC} accroding to the device simulations.

D	D_{WC} [μm]					
	2.75	5.00	10.0	15.0	20.0	25.0
	MCU/SEU [%]					
0.5	4.57	26.28	43.63	46.38	48.79	49.65
0.6	2.31	22.31	28.18	33.56	37.70	45.74
1.0	0.0042	8.89	20.57	27.69	29.70	36.63
1.5	–	0.42	7.08	9.37	10.59	13.52
2.0	–	0.20	0.57	1.60	1.94	3.84
2.5	–	–	0.045	0.51	0.97	1.57
3.0	–	–	–	0.22	0.74	1.32
4.0	–	–	–	0.0017	0.026	0.32
4.5	–	–	–	–	0.0046	0.02
5.0	–	–	–	–	–	0.0038

at which the distance between well contacts and redundant latches D_{WC} is 1.0 μm. Total collected charge of L1 reduces by 90% when the well contacts are placed between redundant latches. The ratio of MCU to SEU decreases to 0.073% in this layout structure. According to the results of neutron experiments and device simulations, the ratio of MCU to SEU decreases by increasing the distance of latches D. The fitting lines are influenced by $D^{-1.67}$ and $D^{-2.07}$ by experiments and simulations respectively. Experimental results also show that MCU rates drastically reduce by inserting well-contact arrays under supply and ground rails. The number of MCU reduces to one. We use several simple device simulations to estimate the MCU tolerance of redundant latches. The results of device simulations almost coincides with the neutron experiments.

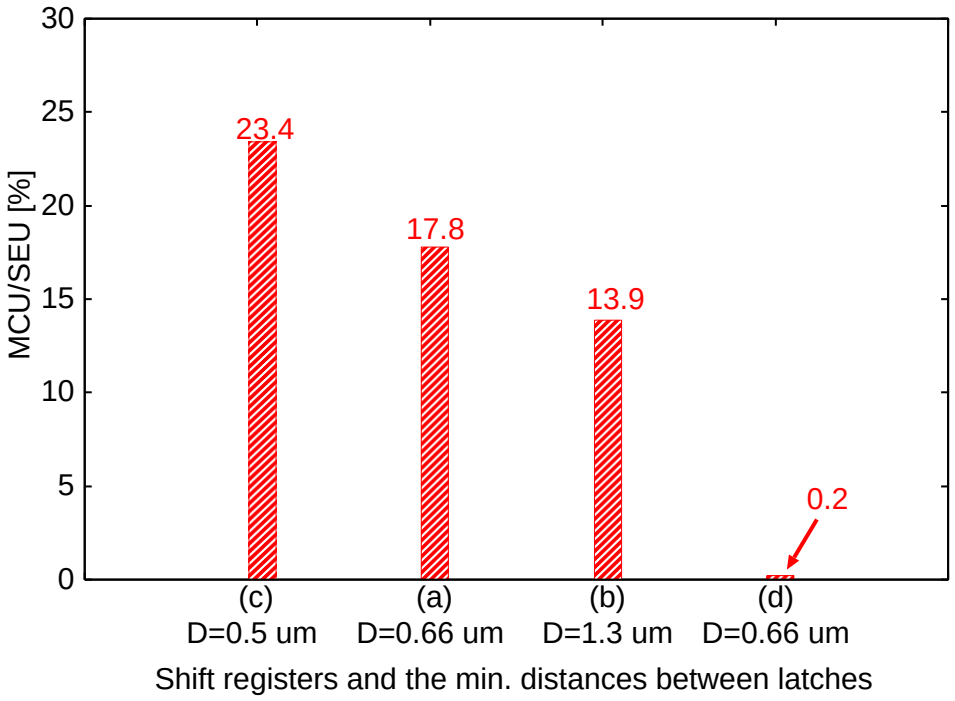


Figure 4.24: The ratio of MCU/SEU according to the min. disatance between latches by experiments.

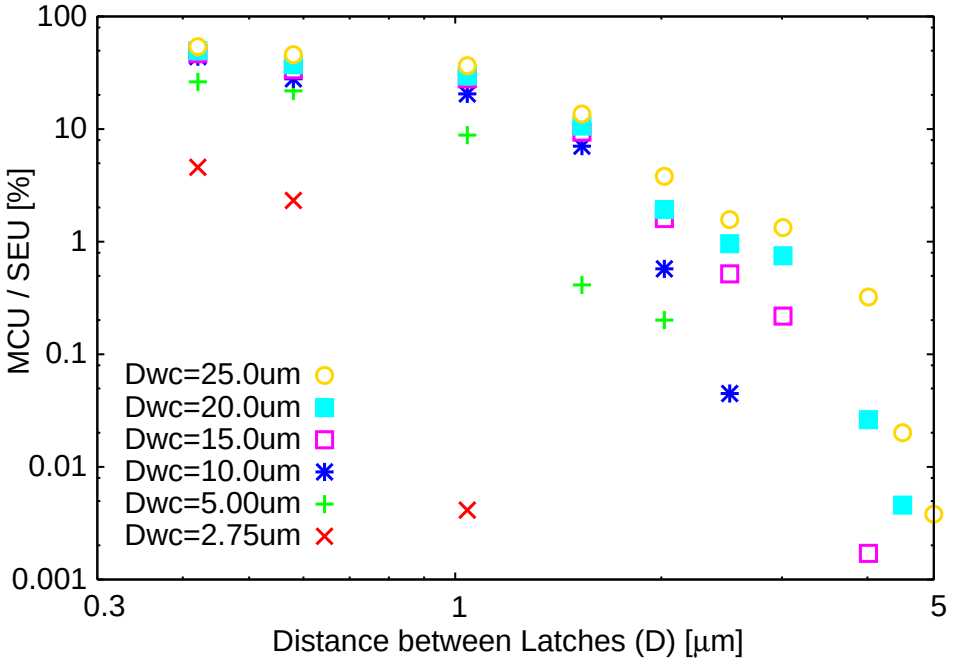


Figure 4.25: Distance-dependence of the ratio of MCU to SEU by device-simulations in different D_{WC}.

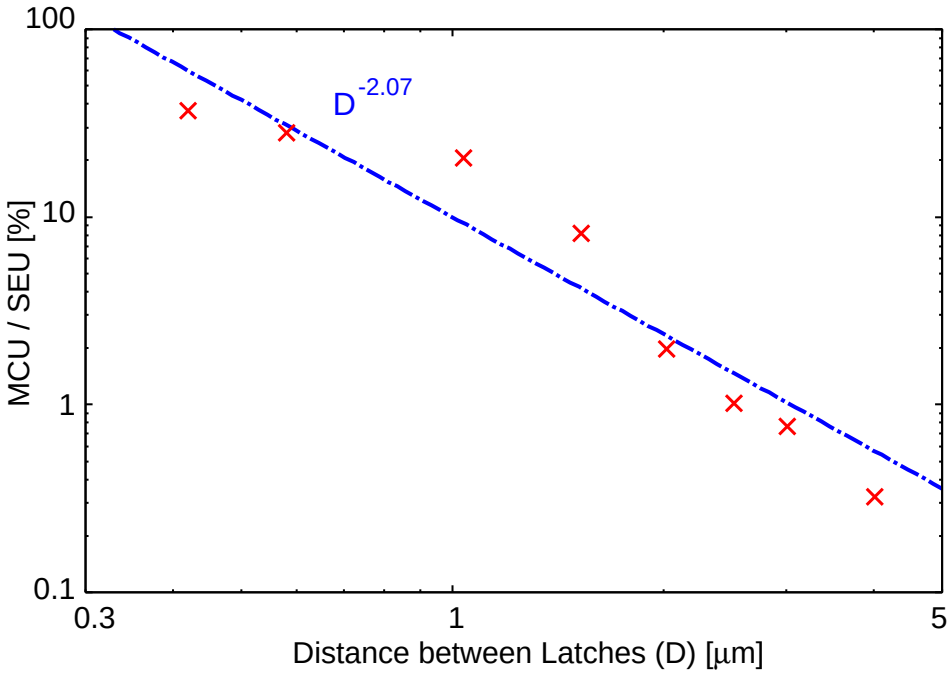


Figure 4.26: Distance-dependence of the ratio of MCU to SEU by device simulations.

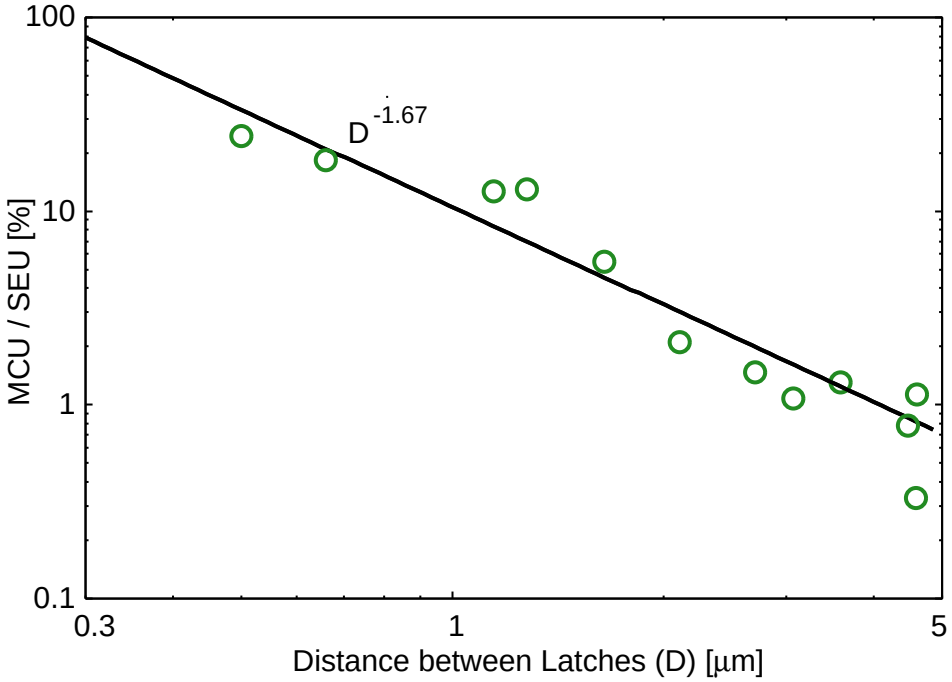


Figure 4.27: Distance-dependence of the ratio of MCU to SEU by neutron experiments.

Chapter 5

Analysis of Soft Error Rates in 65- and 28-nm FD-SOI Processes depending on BOX Region Thickness and Body Bias by Monte-Carlo Based Simulations

In this chapter, the SERs (Soft Error Rates) of FD-SOI processes depending on BOX (Buried OXide) regions and body bias are estimated by alpha, neutron irradiation experiments and Monte-Carlo based simulations. The 65-nm SOTB (Silicon on Thin BOX) and 28-nm UTBB (Ultra Thin Body and BOX) FD-SOI processes are evaluated in this work. A Monte-Carlo simulation methodology called PHITS-TCAD estimates the SERs depending on thickness of BOX regions and body bias. The SERs of those structures are analyzed with layout patterns of test chips. The simulated results are consistent with the alpha and neutron irradiation measurement results. Simulated results reveal that the SERs are decreased by increasing the thickness of BOX region. By applying the reverse body bias the tolerance for soft error becomes stronger in SOTB while that in UTBB becomes weaker.

5.1 Introduction

SEU (Single Event Upset) is caused by radiation induced charge collection at a single sensitive node, such as the drain layer of a single transistor. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), or Dual Interlocked storage CEll

(DICE)[19] have been employed to suppress the effects of charge collection at multiple circuit nodes. Silicon On Thin BOX (SOTB)[58] and Ultra Thin Body and BOX (UTBB)[59] are two FD-SOI processes with a thin BOX layer. It can efficiently mitiage the charge collected into device. Thus, they have higher soft error tolerance than bulk structures. Threshold voltage variations by fabrication process variability are reduced due to the dopantless channel of FD-SOI. The supply voltage of SOTB can be decreased to 0.4 V[60]. It is necessary to investigate the soft error tolerance of FD-SOI structure at lower voltage.

The charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the drift and diffusion, also the parasitic bipolar effect (PBE) become dominant when a single event occurs in the circuit[50]. It is difficult to analyze the SER by only circuit-level simulations such as SPICE. Thus, TCAD simulation is indispensable. However, there are only heavy ion models in most TCAD simulators. In order to get precise results by TCAD simulation to compare to neutron or alpha-induced SERs, we nomally perform simulation a few dozen times with variety particle direction. It takes long time to get simulation results.

In this Chapter, we measure alpha-particle and neutron-induced SEUs on 65-nm SOTB and 28-nm UTBB latches. We also analyze these experiments by Monte-Carlo based simulation called PHITS-TCAD. The simulation tool is similar to the simulation tools such as MRED[61], IRT[62] and PHYSERD[63]. PHITS[30] is a physics-level simulator as Geant4. The neutron and alpha particle nuclear reactions can be run in PHITS by inputting the structures of layouts. The simulation results are consistent to the experimental results, we also make FD-SOI device-models with different BOX-layer thicknesses, and analyze the SERs of those models.

Moreover, it is commonly used to reduce power consumption by body biasing. The charge collection and well potential is also influenced by body bias when a particle hits device in 130-nm process[64] and 65-nm process[65]. The soft error rates of the radiation-hard structures are changed a lot by technology downscaling. Thus, it is also important to estimate the soft error rates in 65-nm SOTB and 28-nm UTBB structures by body biasing.

This Chapter is organized as follows. Section 5.3 introduces the PHITS-TCAD simulation methodology[66]. I compare the simulated results with alpha and neutron irradi-

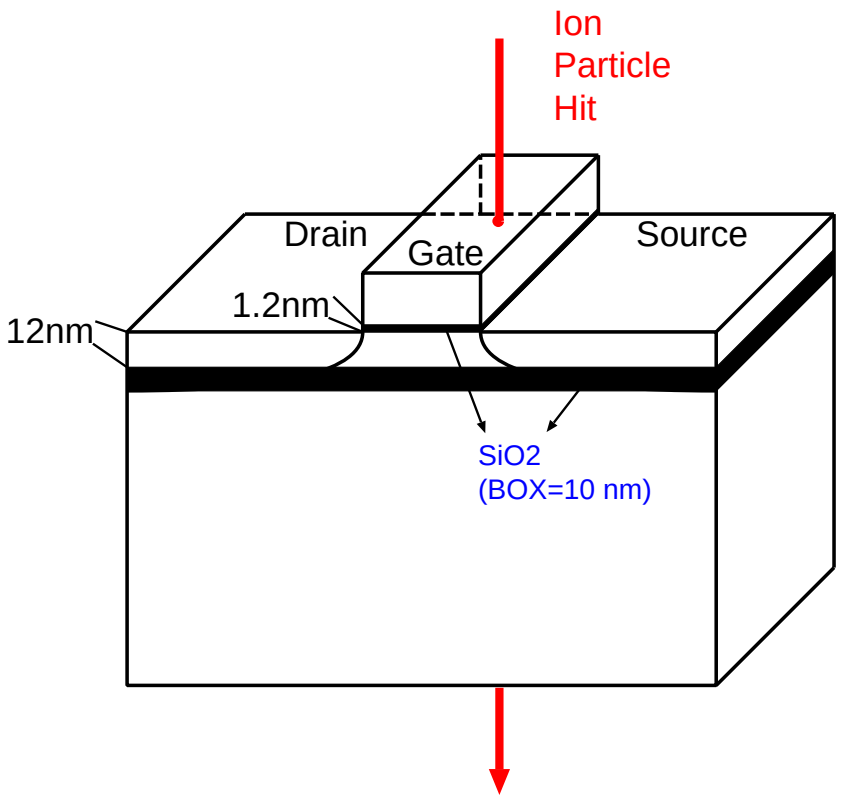
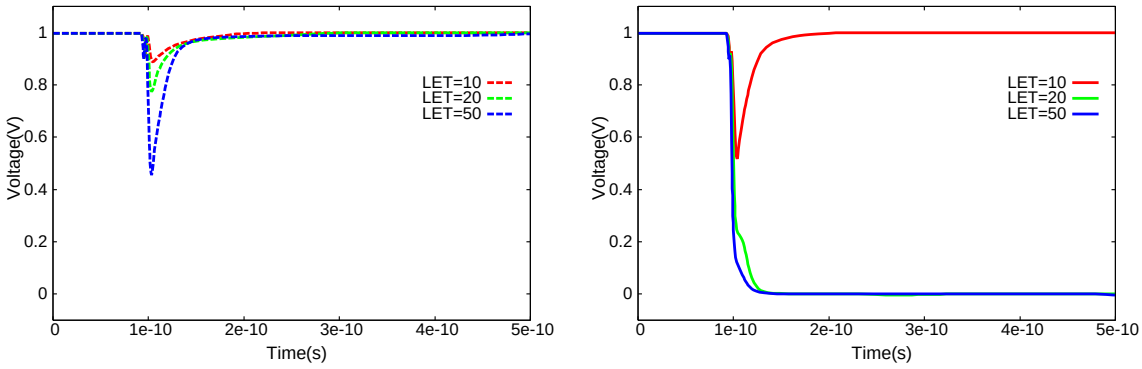


Figure 5.1: 3D device-level SOI transistor.

ation experimental results[67] by reducing supply voltage in Section 5.4. The simulated results depending on thickness of BOX layer and body bias are also shown in Section 5.4. Section 5.5 concludes this Chapter.

5.2 Tolerance of SOI Transistors to Soft Errors

In this section, the tolerance of SOI transistor is analyzed by TCAD simulations. Fig. 5.1 shows an SOI model. A 10 nm BOX (Buried Oxide)[**?**] is placed under drain and source regions. The depth of the SOI (transistor) region is 12 nm. This SOI transistor is constructed based on a 65 nm process. The tolerance of redundant SOI latches are compared in this section. In this section, a conventional latch circuit as Fig. 4.1 are used in device-level simulations.



(a) The particle penetrate on drain region (b) The particle penetrate on gate region

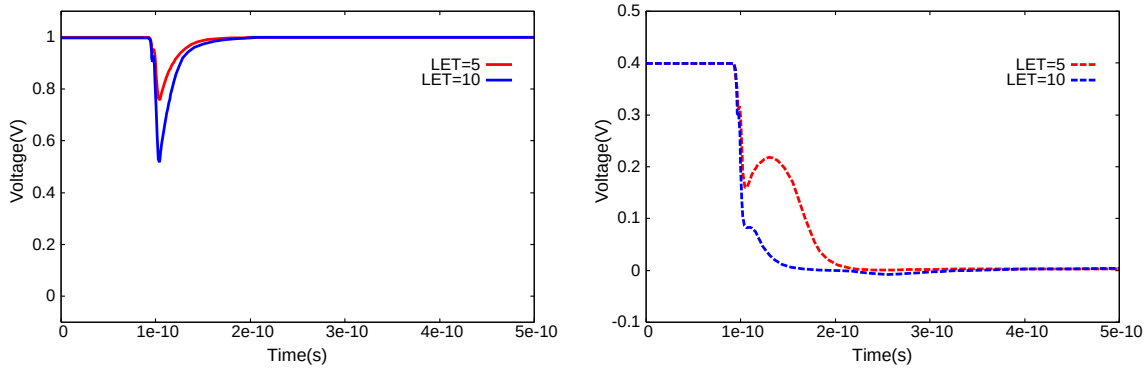
Figure 5.2: The voltage outputs of redundant latches in layout structure B by a particle.The voltage outputs of SOI latch by a particle. LET=10, 20 and 50 MeV/mg/cm^2.

5.2.1 Tolerance Analysis by Changing Particle Penetrate Locations

Fig. 5.2 shows the voltage outputs when a particle penetrates drain and gate region of SOI redundant latches respectively. the LET of the particle are 10, 20 and 50 MeV/mg/cm^2. As the charge collection is suppressed by BOX, little charge is collected into drain when a particle penetrates the drain region. The latches do not flip as shown in Fig. 5.2(a). When a particle penetrates gate region of the SOI latches, the voltage output does not upset when LET=10 MeV/mg/cm^2. However, the outputs start to upset when the LET is increased to 20 MeV/mg/cm^2 as shown in Fig. 5.2(b). Large amount of charge is collected into drain when a particle penetrates the gate region and crosses the body region of the SOI transistor. The parasitic bipolar transistor of SOI turns on by the body potential elevation. The possibilites when a particle hits on the small gate region is much smaller than that on the much larger drain region. Even when a particle hit on the gate region. generated charge is very small because of the smaller sensitive volume on the gate region over BOX. Thus, SOI transisitors become much stronger than bulk transistors. It makes SOI transistors become weak to high energy particle.

5.2.2 Tolerance Analysis by Voltage Scaling

Fig. 5.3 shows the voltage outputs by a particle whcih penetrates the gate region. The VDD is set in 1.0V and 0.4V respectively. There is no dopant in the channel of SOI



(a) VDD=1.0 V (b) VDD=0.4 V

Figure 5.3: The voltage outputs of SOI latch by a particle penetrate on gate region. LET=5 and 10 MeV/mg/cm^2.

transistors. Variations are suppressed in the SOI structure. Thus, the VDD of SOI transistors can be decreased as low as 0.4V. The LET of the ion particles are 5 and 10 MeV/mg/cm^2. When the VDD is 1.0V, the outputs does not upset as shown in Fig 5.3(a). The charge collection mechanism is suppressed by BOX of SOI transistors. However, when VDD is scaled to 0.4V, the outputs start to upset as shown in Fig. 5.3(b). The tolerance of SOI transistor to soft error decreases by VDD scaling. The relationship between power supply voltage and the tolerance of SOI transistors is shown in Fig. 5.4. The tolerance of SOI transistor to soft error linearly decreases by VDD scaling.

5.2.3 Comparison of Tolerance between Bulk and SOI Redundant Latches

Fig. 5.5 shows the voltage outputs when a particle penetrates SOI redundant latches. The LET of the particle are 10 and 20 MeV/mg/cm^2. The redundant latches are constructed in the layout structure C, which sensitive to soft errors as described in Chap. 4. It is order to compare the tolerance between SOI and Bulk structures. When LET=10 MeV/mg/cm^2, the SOI redundant latches do not upset as shown in Fig. 5.5(a), while the bulk redundant latches upset simultaneously as shown in Fig.4.8(a). When LET is increased to 20 MeV/mg/cm^2, only the output N_{I0} upsets as shown in Fig. 5.5(b), while N_{I0} and N_{I1} upset at the same time as shown in Fig. 4.8(b). The BOX on the SOI structure suppresses the charge sharing and bipolar effects between the latches L0 and L1 strongly. MCUs are suppressed in SOI redundant latches, even though layout struc-

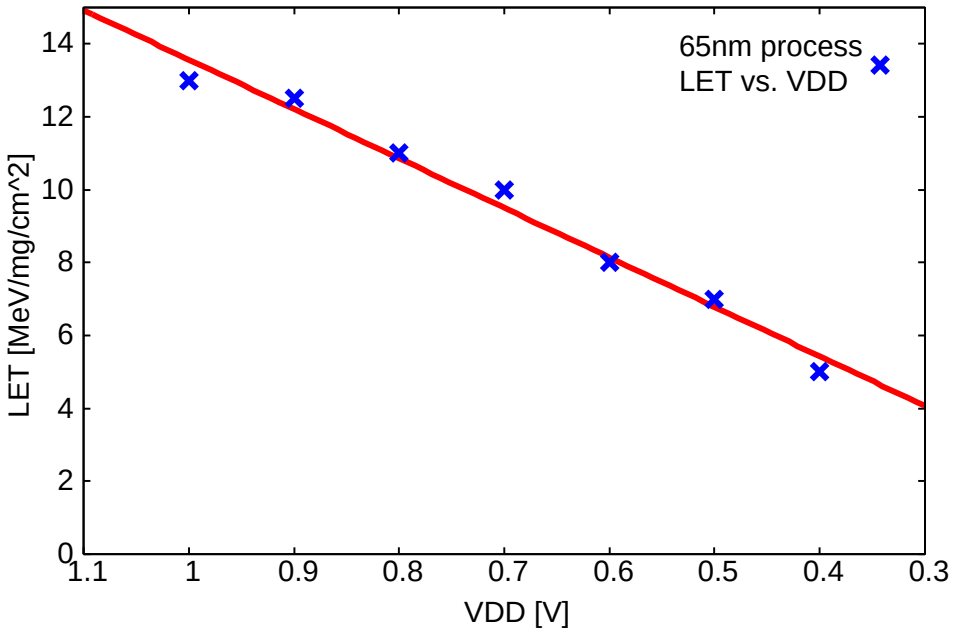


Figure 5.4: LET of particle which upset SOI latch vs. VDD

Table 5.1: The threshold LET of SOI and Bulk redundant latches in layout C.

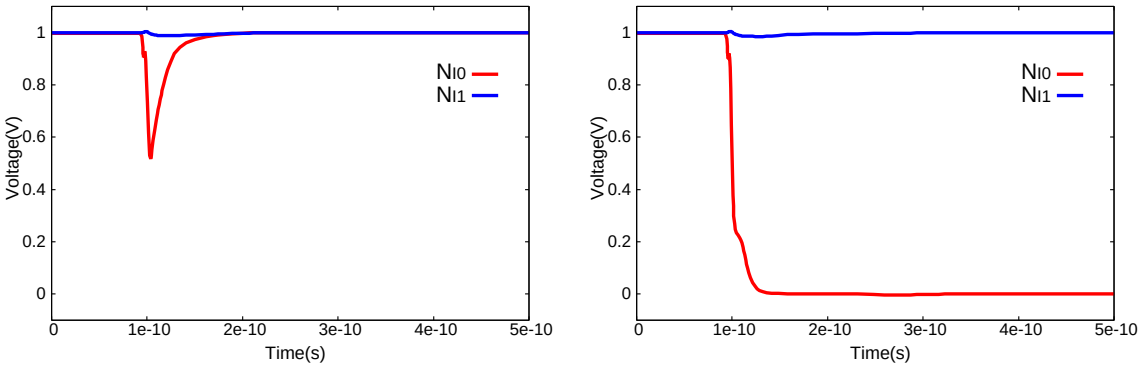
Structure	LET of SEU	LET of MCU
SOI	12.4	N/A
Bulk	5.2 (44% of SOI)	8.3

ture C is used. Table 5.1 shows the threshold LET when SEU(MCU) occurs in SOI and bulk redundant structure. The threshold LET of SEU is decreased by 44% cpmpared with that on A when the redundant latches are fabricated in bulk structure instead of SOI. There is no MCU occurrence in SOI redundant latches. Thus, the tolerance of SOI redundant latches to soft error is stronger than bulk structure according to the results of TCAD simulations.

5.3 PHITS-TCAD Simulation Methodology

5.3.1 PHITS-TCAD simulation

Fig. 5.6 portrays a flow chart of the proposed simulation methodology by PHITS and TCAD. PHITS is a Monte-Carlo physics simulator. It simulates the nuclear reaction of an incident particle with constituent atoms in a device, and the sequential charge



(a) LET=10 MeV/mg/cm^2 (b) LET=20 MeV/mg/cm^2

Figure 5.5: The voltage outputs of SOI redundant latches by a particle penetrate on gate region of latch L0. LET=10 and 20 MeV/mg/cm^2.

deposition. PHITS can calculates the deposit energy when directed ion particles (heavy ion, alpha particle) or secondary particles crosses the sensitive volume of a device as shown in Fig. 5.6. The deposit energy (E_{D}) corresponds to the lost energy of the particle. Soft errors occur in a circuit when E_{D} reaches the threshold value. All calculation modes we used are refer to [63].

In the TCAD simulation, generated charge (Q_{gen}) is collected into drain by a particle hit as shown in Fig. 5.6. An SEU occurs in the circuit when Q_{gen} is large enough. We call the Q_{gen} which just upsets latch circuit threshold charge (Q_{th}) in this paper. It is used to calculate the threshold E_{D}. Q_{gen} can be converted to E_{D}. In silicon, it takes 3.6 eV energy to create an electron-hole pair, and charge of an electron is 1.6 x 10^{-19} C. Thus E_{D} of 1 MeV is equivalent to Q_{gen} of 44.5 fC[68].

Fig. 5.7 shows the relationship between the number of particles and E_{D} in the sensitive volume by PHITS simulations. The blue dashed line shows the threshold E_{D} which is calculated by TCAD simulations. The particles, of which E_{D} is larger than the threshold E_{D}, causes SEUs (# of errors) as shown in Fig. 5.7.

5.3.2 Simulation Setup

Fig. 5.8 shows the bird view of the device structure in PHITS simulations. It shows an NMOS transistor in latch structure as shown in Fig. 5.9. The red box in Fig. 5.8 indicates a sensitive volume. It is built based on the layout structures of the test chips. The SOI body under the gate of an inverter is considered as the sensitive volume. The

thicknesses of the thin BOX and SOI layer in the 65-nm SOTB process are 10 nm and 12 nm while those are 25 nm and 7 nm in the 28-nm UTBB process respectively. The same structures are constructed in TCAD simulations as 3D device-models. Fig. 5.10 shows the cross-section of the 3D device NMOS models. The operating characteristics of the TCAD models are optimized to the SPICE model. We use the device simulator "sentaurus" to perform all TCAD simulations. A heavy ion particle hits the center of inverter gate in a SOI latch circuit. We use a classical gaussian shape to account for the radial energy deposition distribution. The radius of the particle is 70 nm. The TCAD simulations are performed by decreasing the supply voltages. We increase the LET of the particles until the latch is flipped. Then we can obtain Q_{th} in each supply voltage. The normal direction of particles are only considered in this paper. We will discuss the direction and position affects in future work.

5.3.3 $\mathrm{Q_{gen}}$ Calculation by TCAD simulations

PHITS is a Monte Carlo particle transport simulation code. Thus, it does not consider the parasitic bipolar effect as in TCAD simulations. The charge deposited into the sensitive volume is used to calculate the $\mathrm{Q_{gen}}$.

Fig. 5.11 shows two current waveforms of NMOS when a particle hits the SOI latch in Fig. 5.9 by TCAD simulations. The blue waveform is the current pulse by electrons collected into drain node, while the red one by holes collected into source node. Blue waveform shows the $\mathrm{Q_{crit}}$. We integrate the red current waveform to calculate the Q_{gen}.

5.4 Results and Discussion

We analyze the soft error rates of SOTB and UTBB structures according to supply voltages by the proposed simulations and alpha irradiation experiments. The simulation results and experimental results are shown in this section. A 3 MBq ^{241}Am alpha source is used in the experiments and the size of the alpha source is one cm^2. The irradiation time is one minute.

Alpha-particle-induced SEU cross-section is calculated as follows:

$$CS_{\alpha}(\mathrm{cm}^2/\mathrm{bit}) = \frac{N_{\mathrm{error}}}{F_{\alpha} \times N_{\mathrm{bit}}} \tag{5.1}$$

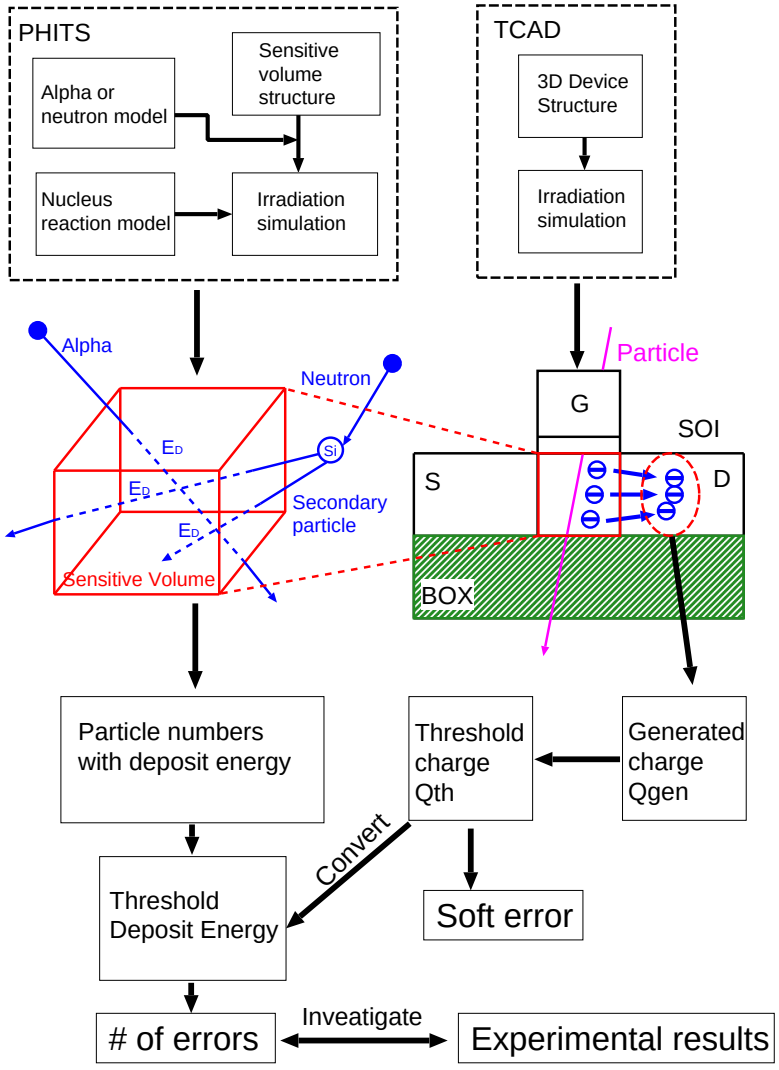


Figure 5.6: Flow chart of the PHITS-TCAD simulation system.

where N_{error} is the number of errors and F_α is the flux of alpha particles. F_α is number of generated alpha particles by alpha source ($3 \times 10^6 \times 60$ s $= 1.8\text{x}10^8$)/cm^2 in one minute test time. N_{bit} is the number of bits.

The neutron irradiation experiments were done at Research Center for Nuclear Physics (RCNP) in Osaka Univ. All experimental setup and results of this section in detail are described in [67]. The experimental results of DFF in [67] are compared to simulation results.

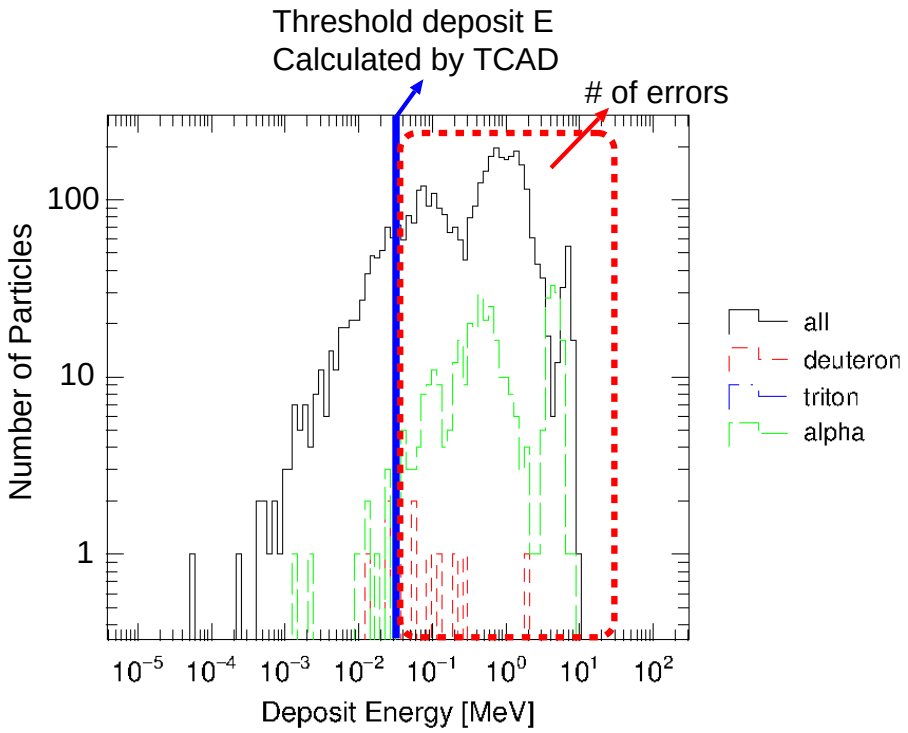


Figure 5.7: The deposited energy by PHITS. The particle, which deposited energy is larger than the threshold energy, is counted to one SEU.

5.4.1 Comparison Between Measurement and Simulation

Fig. 5.12(a) shows the alpha cross-section by the PHITS-TCAD simulations and the experimental results of the SOTB structure. supply voltage is swept from 1.2 V to 0.4 V.

In PHITS simulations the number of the alpha particles is 1.8x10^8 in one cm^2. The area of flip-flop is 4.08×1.8 μm^2. The number of FFs in the test chip is 1.06 kbit. The cross-section increases by reducing the supply voltage suggests that it easy to upset the SOTB latch by reducing the supply voltage. in the result of the experiment, the SEU cross-sections at the supply voltage of 0.4 V is six times larger than that at supply voltage of 1.2 V. The PHITS-TCAD simulation results are consistent to the experiment results.

Fig. 5.12(b) shows the alpha cross-section by the PHITS-TCAD simulations and experiments of the UTBB latch structure. There is no error in the UTBB structure

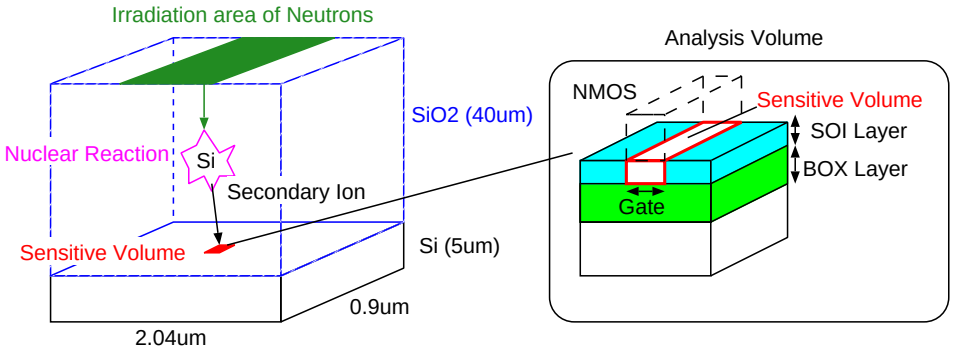


Figure 5.8: Device structure used in PHITS simulations. This structure shows the sensitive volume of a latch. The SOI layers under G is regarded as the sensitive volume according to the TCAD simulation.

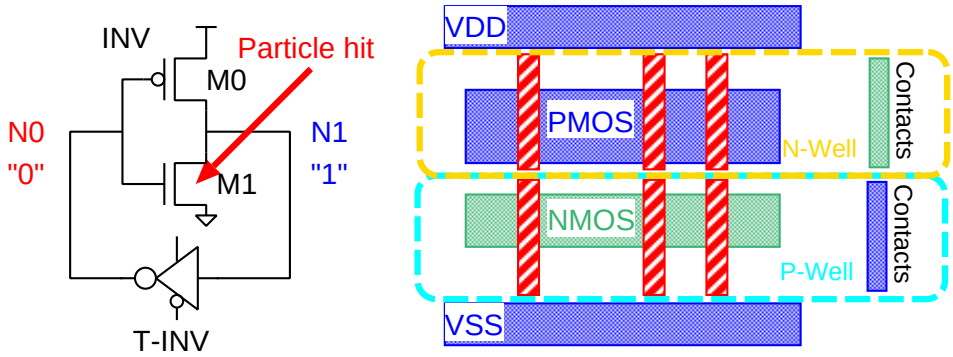
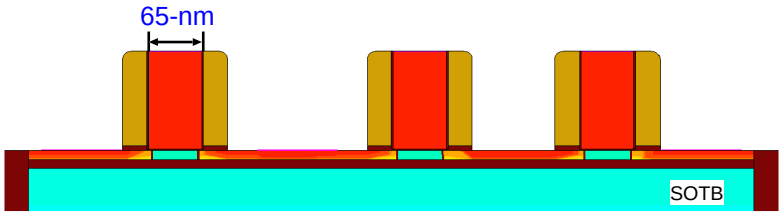


Figure 5.9: Circuit and Layout structure of a conventional latch.

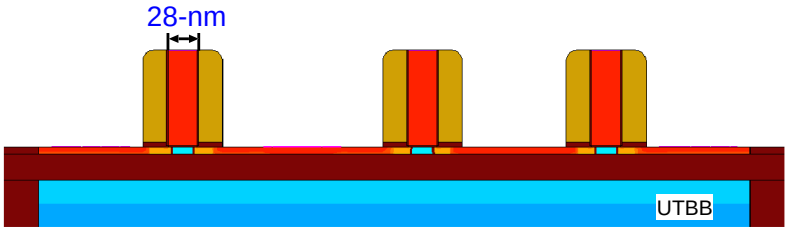
when the supply voltage is larger than 0.5 V. Therefore, we sweep the supply voltage form 0.45 V to 0.4 V in the simulations and experiments. The number of the alpha particles are also 10^8 in PHITS simulations. The area of one flip-flop is 2.04×0.9 μm^2. The number of FFs in the test chip is 40 kbit.

When supply voltage reduces from 0.45 V to 0.4 V, the SEU cross-section increases 2.5 times as large as before. According to the alpha test results, the cross-sections of SOTB and UTBB are 1.33 x 10^{-11} cm^2/bit and 3.56 x 10^{-12} cm^2/bit by applying 0.4 V supply voltage. As the sensitive volume in UTBB is smaller than SOTB, it makes the cross-section much lower.

Fig. 5.13(a) and 5.13(b) show the SERs by neutron irradiation experiments and PHITS-TCAD simulations.



(a) The cross-section of 3D NMOS device model in the 65-nm SOTB structure.



(b) The cross-section of 3D NMOS device model in the 28-nm UTBB structure.

Figure 5.10: The device-level models.

Eq. (5.2) is used to calculate the SERs of PHITS-TCAD simulations. Eq. (5.3) is employed to calculate the SER for measurement.

$$SER_{\mathrm{SEU}}[\mathrm{FIT/Mb}] = \frac{3.6 \times 10^{18} \times \mathrm{A_n} \times \mathrm{N_{SEU}} \times \mathrm{F}}{\mathrm{N_n} \times \mathrm{N_{bit}}} \tag{5.2}$$

where A_{n} is the area irradiated by neutron beam in PHITS simulations. N_{SEU} is the number of SEUs and N_{n} is number of neutrons. The number of neutrons in simulation is 10^9. F is the neutron Flux on the NYC sea-level.

$$SER_{\mathrm{SEU}}[\mathrm{FIT/Mb}] = \frac{3.6 \times 10^{18} \times \mathrm{N_{SEU}}}{\mathrm{T_{test}} \times \mathrm{AF} \times \mathrm{N_{bit}}} \tag{5.3}$$

where N_{SEU} is the number of SEUs, T_{test} is irradiation test time and AF is accelerated factor of neutron beam of irradiation test.

The simulation results are consistent with the neutron irradiation experimental results in the 65-nm SOTB as shown in Fig. 5.13(a). According to the neutron irradiation experimental results, there is no error in the 28-nm UTBB structure. Only the simulated results are shown in Fig. 5.13(b). From the results of PHITS-TCAD simulation, the soft error tolerance of 28-nm UTBB is at least 2 times stronger than that of 65-nm SOTB.

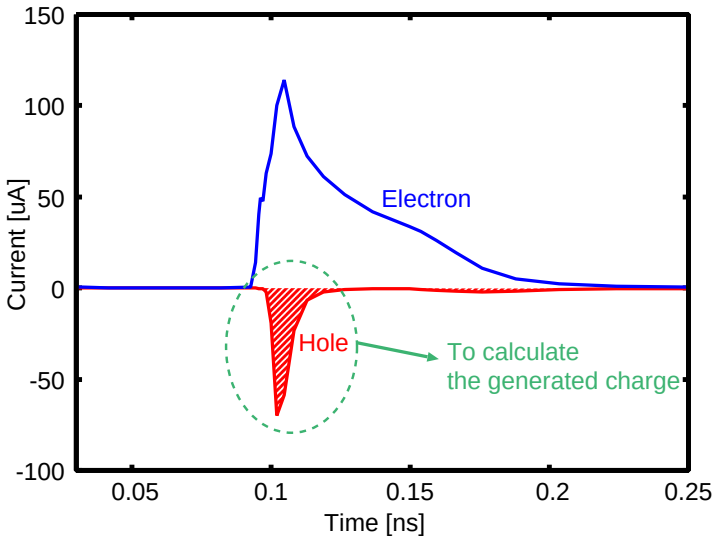


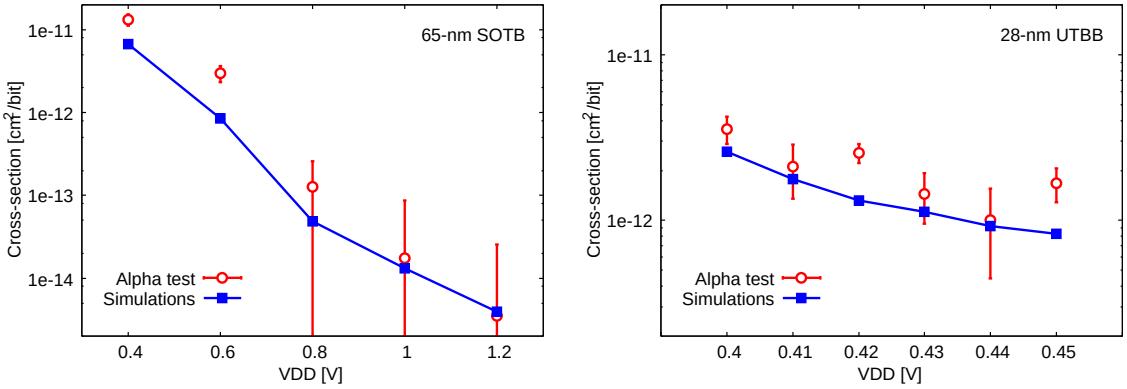
Figure 5.11: Current waveforms by a particle hit. Blue current pulse is generated by electron collection, while the red one is by hole collection. The generated charge collected by drift and diffusion is used to calculate the Q_{th}.

As the results of simulations are consistent to the experimental results, the SERs of several device models can be predicted by the PHITS-TCAD simulation.

5.4.2 Influence of BOX Region Thickness on Neutron-induced SER

In this section, we change the thickness of BOX layer in the 65-nm SOTB and 28-nm UTBB. The thicknesses of BOX layer and SOI body in 65-nm FD-SOI are 10 nm and 12 nm while those are 25 nm and 7 nm in 28-nm FD-SOI respectively. The SERs of these structures are analyzed by the PHITS-TCAD simulations with reducing the supply voltage.

Fig. 5.14 shows the result of PHITS-TCAD simulation for neutron irradiation on 65- and 28-nm FD-SOI. The SERs are reduced by increasing the thickness of the BOX layer in 65-nm SOTB and 28-nm UTBB structures. The SERs of 65-nm SOTB decrease almost 20% when the supply voltage is 0.4 V as shown in Fig. 5.14(a). There is only 10% difference in SERs between the thin and thick BOX layer in 28-nm UTBB structure as shown in Fig. 5.14(b). It is because that only few errors occur in UTBB structure. As the sensitive volume of UTBB is much smaller than SOTB, the PBE becomes weaker in



(a) The cross-section in SOTB structure according to the alpha irradiation experiments and simulations.

(b) The cross-section in UTBB structure according to the alpha irradiation experiments and simulations.

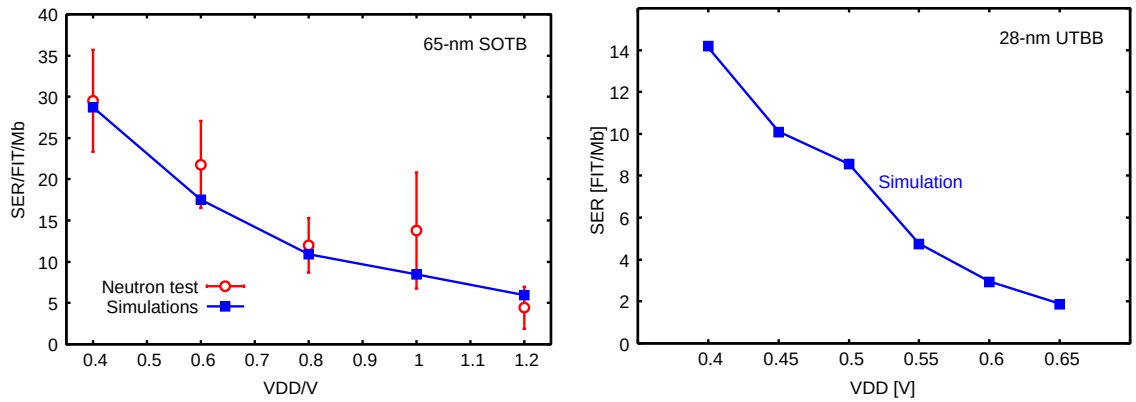
Figure 5.12: Results of alpha irradiation experiments and PHITS-TCAD simulations.

the UTBB structure.

Fig. 5.15 shows the potential of BOX and SOI layer by a particle according to TCAD simulations. The potential of BOX keeps low when the thickness of BOX layer is 100 nm while the potential of 10 nm BOX layer increases. LET of the particle is 10 MeV-cm^2/mg. It influences the potential of SOI layer.

Fig. 5.16 and 5.17 shows the potentials of BOX and SOI layers by a particle hits depending on the thickness of BOX layers in 65-nm and 28-nm SOI respectively. LET of the particle is 10 MeV-cm^2/mg. In 65-nm SOI, the peak value of potentials of BOX layer increases highly, and SOI potential becomes difficult to back to 0 V when the thickness of BOX layer is much higher. The electron-hole pairs generated in the substrate easy to affect the potential of SOI layer when the thick of BOX layer is thin. It becomes easier to turn on the parasitic bipolar transistor in the SOI layer. Thinner BOX layer of SOI weakens the tolerance for soft error.

However, in 28-nm SOI, the SOI and BOX layers potential do not increase over 0.6 V by a particle hits. They also do not change effectively by BOX thickness variation. electron-hole pairs becomes harder to generate in 28-nm SOI by it smaller sensitive volume and higher doping well. It causes the weakness of PBE.



(a) The SERs of SOTB structure according to the neutron irradiation experiments and simulations.

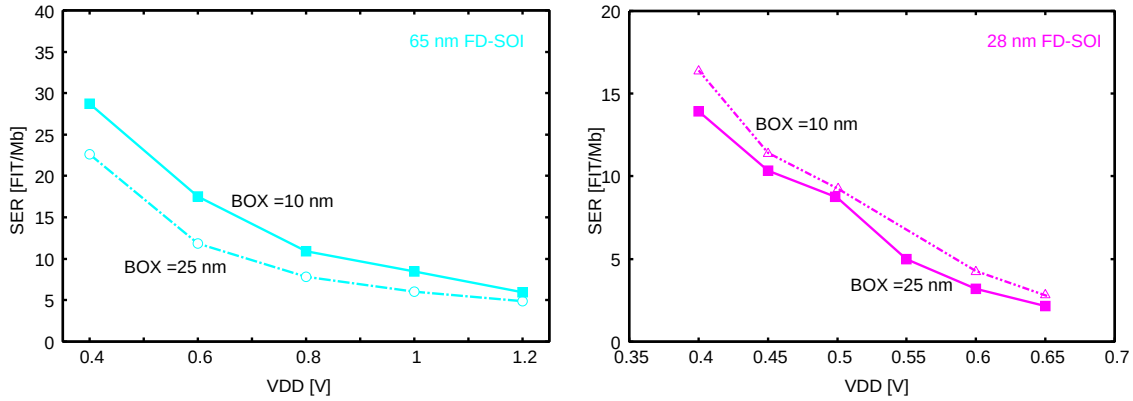
(b) The SERs of UTBB structure according to the simulations.

Figure 5.13: Results of neutron irradiation experiments and PHITS-TCAD simulations.

5.4.3 Influence of Reverse Body Bias on Neutron-induced SER

Fig. 5.18 shows the current waveforms of NMOS in the 65-nm FD-SOI structures, by a 15 MeV-cm^2/mg LET particle hit. We apply the reverse body bias on the NMOS of the FD-SOI structures. When the thickness of BOX layer is 10 nm thick, there are two parts in the current pulse as shown in Fig. 5.18(a). The first part is caused by drift and the second part is caused by the PBE. This phenomenon is shown in[65] very clearly. The first current pulse is very low because the drift mechanism is suppressed by the BOX layer. The PBE is the main factor of charge collection in the SOTB structure. When increasing the reverse body bias of the SOTB structure, the reverse bias suppresses the elevation of well potential after the particle hits. The PBE is suppressed. Thus, the second parts decrease by increasing the reverse bias. However, the pulse waves do not change a lot as shown in Fig. 5.18(b), when we increase the thickness of BOX layer to 25 nm thick.

Fig. 5.19 shows the volumes of collected charge of 65-nm FD-SOI structures. We calculate the collected charge by integrating current waveforms. The collected charge becomes 45% smaller by applying 1.0V reverse bias on NMOS as shown in Fig. 5.19(a), when the thickness of BOX layer is 10 nm. However, the collected charge becomes 26% smaller as shown in Fig. 5.19(b), when the thickness of BOX layer is increased to 25 nm. It is because that the thickness of the BOX layer become thicker, it become hard to



(a) Simulation results of 65-nm FD-SOI. The SERs decrease by thicker BOX layer.

(b) Simulation results of 28-nm FD-SOI. The SERs increase by thinner BOX layer.

Figure 5.14: Results of neutron irradiation simulations by PHITS-TCAD simulations. The thicknesses of BOX layer are changed.

increase the potential of SOI layer by reverse body bias. In the 28-nm FD-SOI structure, the current waves do not change a lot as shown in Fig. 5.20, when the thickness of BOX layers are 10 and 25 nm. The current waveforms do not change a lot by applying reverse body bias.

Fig. 5.21 shows the collected charge for the 28-nm FD-SOI with different RBBs. The collected charge does not change by reverse body bias. It is because that the volume of sensitive layer in 28-nm process becomes 15% of that in 65-nm process. The PBE of SOI layer becomes weaker. It become harder to turn on the parasitic bipolar transistor. In the other hand, RBB widens the depletion region between N-well and P-well in latches, more charge is also collected into P-well after the particle hit. Thus, the collected charge does not decrease.

Fig. 5.22 shows the threshold LETs (the smallest values of LET upsets latches) by increasing the reverse body bias on NMOS and PMOS of SOTB and UTBB. The threshold LETs of SOTB structure increases by applying the reverse body bias as shown in Fig. 5.22(a). The PBE become weaker by reverse body bias, it becomes hard to flip the SOTB latch. However, the threshold LETs of UTBB structure become lower by applying the reverse body bias on NMOS and PMOS as shown in Fig. 5.22(b). It is because that the threshold voltage of transistor becomes higher by applying the reverse body bias. It is easy to flip UTBB latches by a particle hits. The degradation of

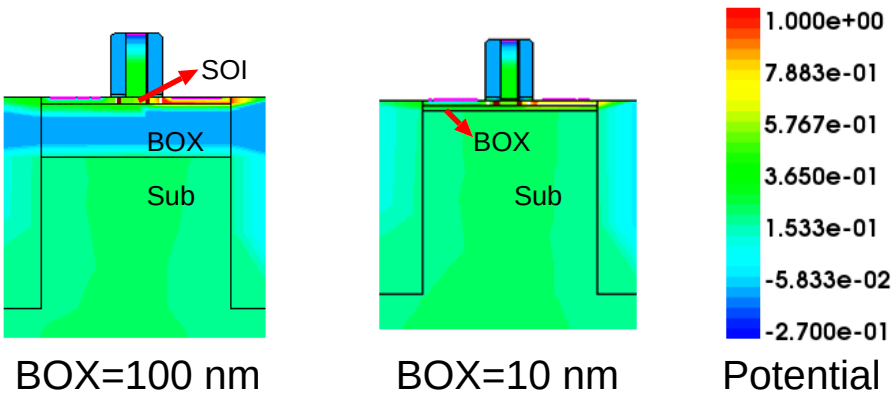


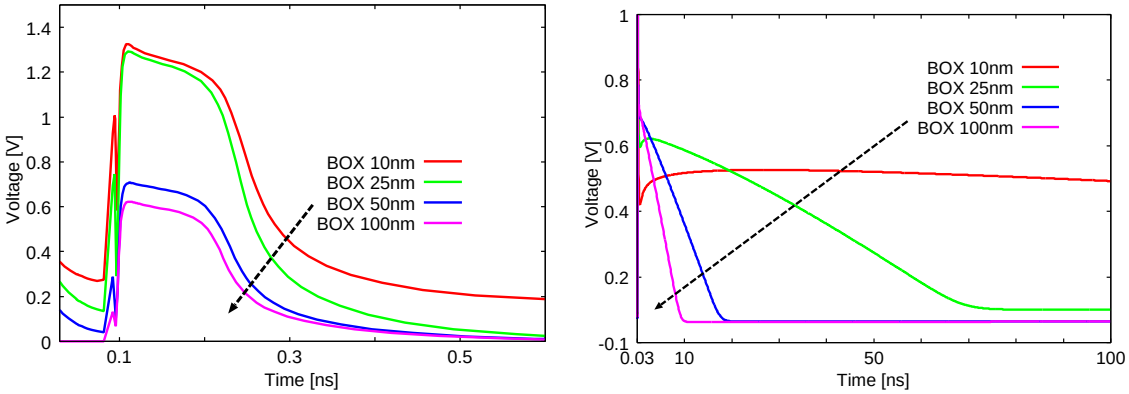
Figure 5.15: The potential by a particle hits. The potential of the 10 nm BOX layer increases while the potential of 100 nm thick BOX layer keeps low.

performance by RBB occur in both SOTB and UTBB. However, the affection of PBE in SOTB is stronger than the degradation of performance. It cause a reducing of collected charge.

Fig. 5.23 shows the neutron induced SERs depending on body bias in SOTB and UTBB structures by PHITS-TCAD simulations. The supply voltage is 1.0 V. In the SOTB structure, the SERs at 1.0 V reverse body bias becomes almost half of that at 0 V bias as shown in Fig 5.23(a). In the UTBB structure, the SERs increase by applying reverse body bias as shown in Fig. 5.23(b). As the performance of transistors in UTBB is much worse by applying high reverse body bias, the SERs increase much higher at 1.0 V bias. It becomes 8× by applying reverse body bias on UTBB from 0 V to 1.0 V. The SERs of 28-nm UTBB increases suddenly when the reverse body bias is 1.0 V. It is because that the particles, which its D_{E} are larger than threshold E, increase suddenly according to the PHITS simulation results.

5.5 Chapter Summary

I analyze the alpha particle and neutron induced SERs by irradiation experiments and Monte-Carlo based simulation: PHITS-TCAD. The 65-nm SOTB and 28-nm UTBB structures are used in our estimation. According to the alpha irradiation test, the SEU cross-sections at the supply voltage of 0.4 V is six times larger than that at supply voltage of 1.2 V in SOTB structure. However, the SEU cross-section increases 2.5 times as large



(a) The potentials of the BOX layer.

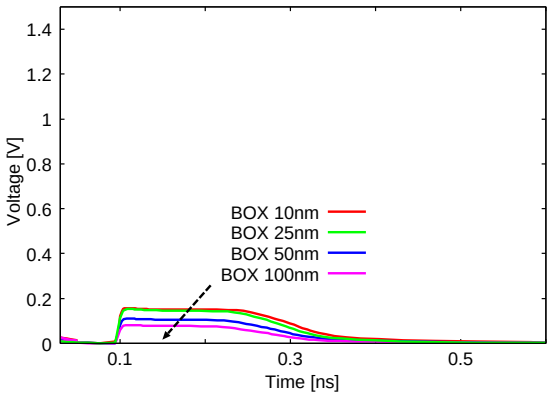
(b) The potentials of SOI layer depending on the thicknesses of BOX layer. It becomes easier to turn on the parasitic bipolar transistor when the thickness of BOX layer is much thinner.

Figure 5.16: The potential of BOX, SOI layer by the a particle hits on 65-nm FD-SOI structure.

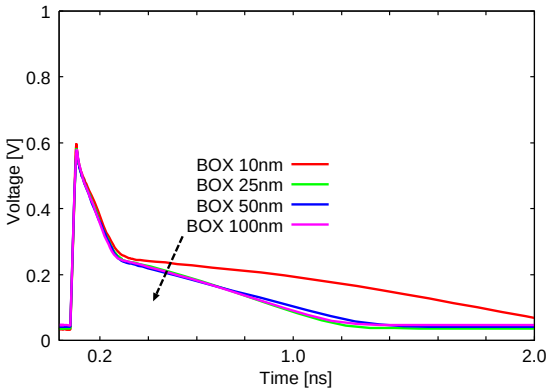
as before, When supply voltage reduces from 0.45 V to 0.4 V in UTBB structure. The cross-setions of SOTB and UTBB are 1.33 x 10^{-11} cm^2/bit and 6.78 x 10^{-13} cm^2/bit by applying supply voltage of 0.4 V.

According to the neutron irradiation test, there is no error occurrence in 28-nm UTBB. PHITS-TCAD simulation shows that the soft error tolerance of 28-nm UTBB is at least 2 times stronger than that of 65-nm SOTB. The simulation results are also consistent with the neutron irradiation experimental results.

According to the PHITS-TCAD simulation results, the SERs of 65-nm FD-SOI structure are decreased by 20% when the thickness of BOX region are increased from 10 nm to 25 nm. However, the SERs of 28-nm FD-SOI does not change a lot. By applying 1.0 V reverse bias, the SERs SOTB structure become half, however the SERs of UTBB becomes 8 times. As the technology downscaling, the sensitive volume is decreased. It is much harder to turn on the parasitic bipolar transistor in 28-nm UTBB structure than in 65-nm SOTB structure.

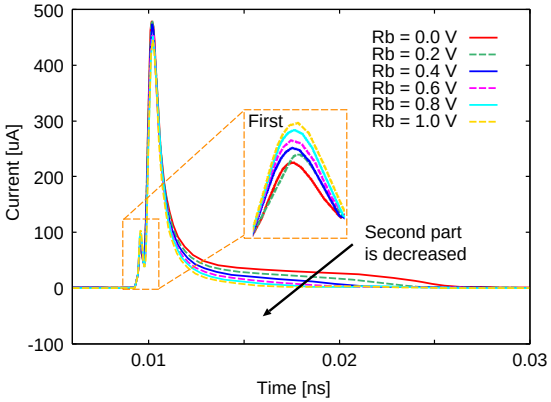


(a) The potentials of the BOX layer.

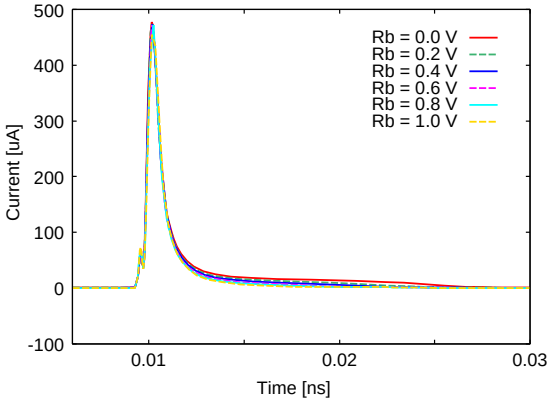


(b) The potentials of SOI layer depending on the thicknesses of BOX layer. It becomes easier to turn on the parasitic bipolar transistor when the thickness of BOX layer is much thinner.

Figure 5.17: The potential of BOX, SOI layer by the a particle hits on 28-nm FD-SOI structure.

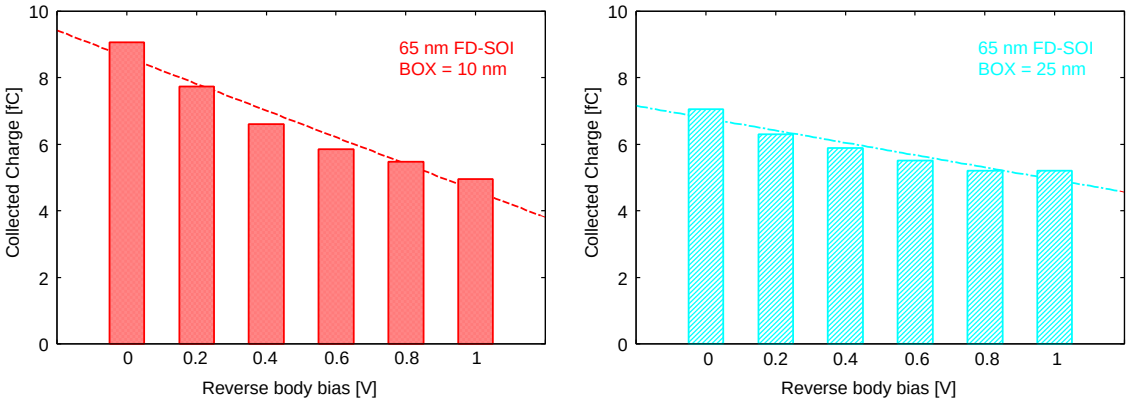


(a) The thickness of BOX layer is 10 nm



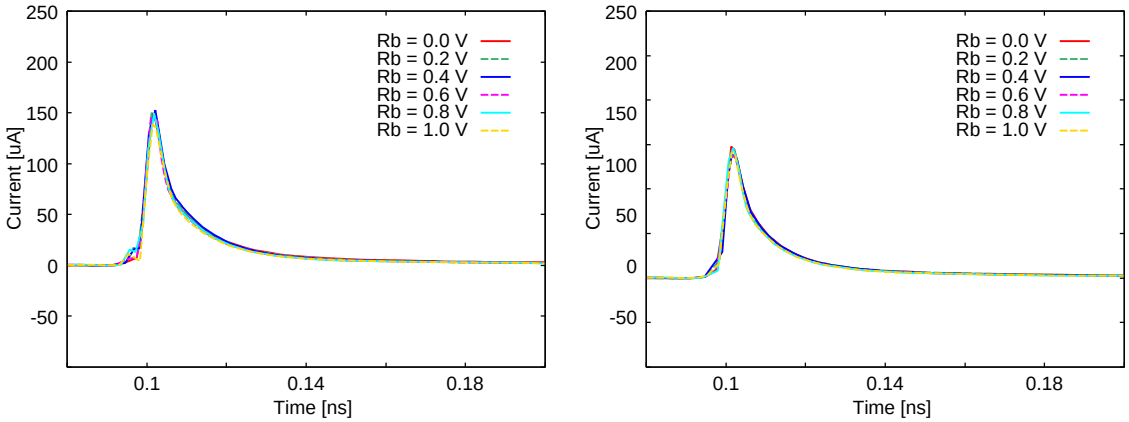
(b) The thickness of BOX layer is 25 nm

Figure 5.18: The current waves by a particle hits depending on the reverse body bias on NMOS in the 65 nm FD-SOI structures.



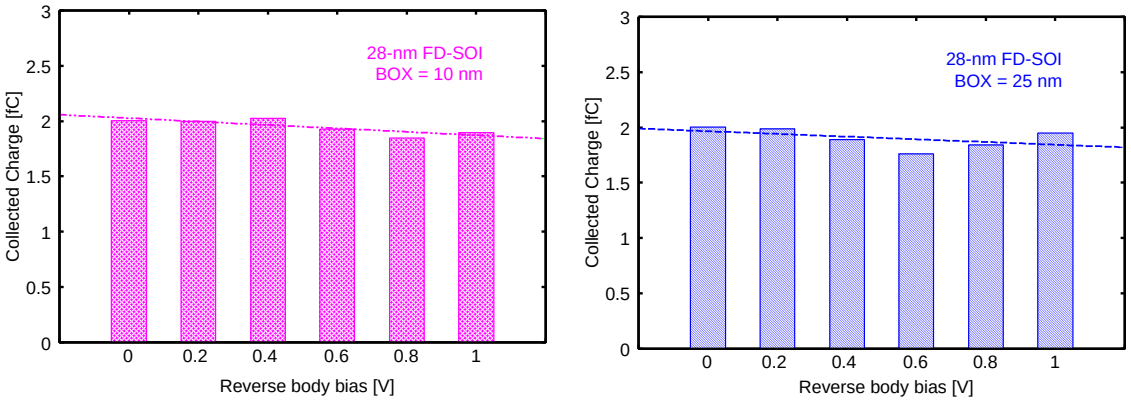
(a) The thickness of BOX layer is 10 nm (b) The thickness of BOX layer is 25 nm

Figure 5.19: The collected charge by reverse body bias on NMOS in the 65 nm FD-SOI structures.



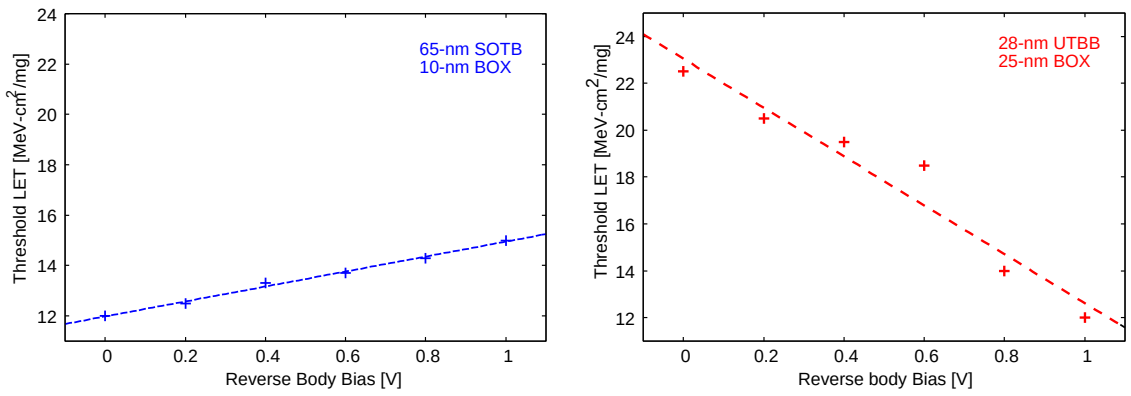
(a) The thickness of BOX layer is 10 nm (b) The thickness of BOX layer is 25 nm

Figure 5.20: The collected charge by reverse body bias on NMOS in the 28 nm FD-SOI structures.



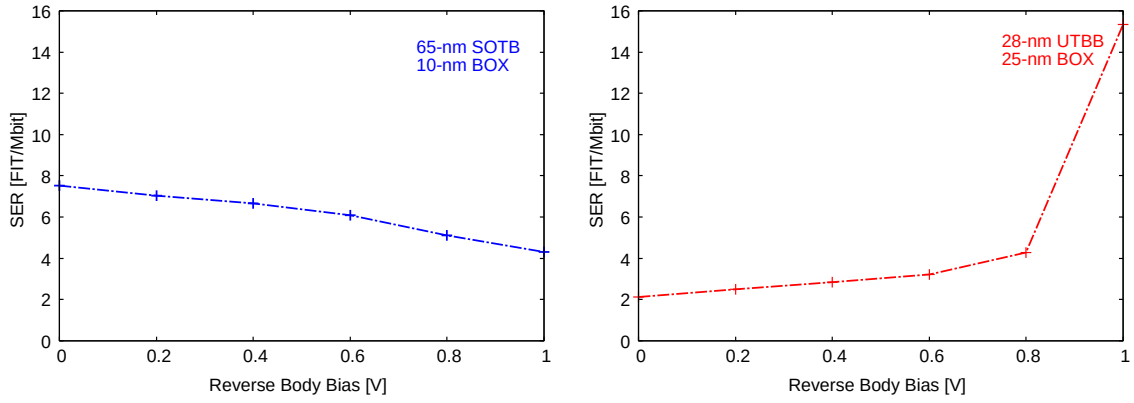
(a) The thickness of BOX layer is 10 nm (b) The thickness of BOX layer is 25 nm

Figure 5.21: The collected charge by reverse body bias on NMOS in the 28 nm FD-SOI structures.



(a) In the SOTB structure. (b) In the UTBB structure.

Figure 5.22: The threshold LET influenced by reverse bias on NMOS and PMOS of SOTB and UTBB structures.



(a) The SERs dependent on body bias in SOTB structure

(b) The SERs dependent on body bias in UTBB structure

Figure 5.23: The SERs depending on body bias which calculated by PHITS-TCAD simulations.

Chapter 6

Conclusion

With technology downscaling, The memory devices in circuits of VLSI have become very sensitive to radiation particle hits. Radiation particles affect the circuit and can result in Soft errors. It is necessary to improve system reliability and resilience to radiation particles. Thus, Mitigation and projection of the soft error tolerance in the scaled circuit and future structures such as SOI (silicon on insulator) become important. Usually, irradiation experiment and simulation are two ways to mitigate the soft error tolerance of circuits. However, as irradiation experiment cost highly, it is hard to test all logic elements of VLSIs. Moreover, The mechanisms and the tolerance of soft error in the scaled processes and future structures have not been discussed enough. Thus, simulation play a very important role in mitigation and projection for SER.

Firstly, the importance of device and physical level simulations are described. In this thesis, the charge generation and collection mechanisms by direct ionization are simulated by TCAD simulator SENTAURUS, and the mechanisms by indirect ionization are simulated by Monte-Carlo based physical simulator PHITS.

After that, the parasitic bipolar effects are utilized to suppress MCUs on the 65-nm process radiation-hardened dual-modular flip-flops. Device simulations reveal that two redundant latches store opposite values suppress a simultaneous flip by a particle hit effectively due to the parasitic bipolar effect. In contrast, redundant latches store the same value are very sensitive to MCUs. From device-level simulations, both latches store the same value are flipped between a certain range of generated charge which is called a vulnerable region. Because of the asymmetric structure of latches, they become a specific state when the parasitic bipolar transistors turn on by a particle hit. When

storing opposite values in two latches, both latches become the same state by a particle hit. But it does not change the output of the redundant FFs because one of these two latches stores the correct value. Even if there is also MCU occurrence in the latter, the probability is very low. Experimental results on a D-FF array fabricated in a 65 nm CMOS prove that the error rates of MCU is about 1,000 times lower when latches store opposite values. The ratio of MCUs/SEUs from the device simulations is lower than the results of experiments. However, the MCU rates of the structure in which two latches store opposite much lower in device simulations and experimental results.

Then, the contributions of layout structures to suppress MCU are analyzed by device-level simulations and neutron experiments. Device simulations show that charge sharing and bipolar effect are two main factors when MCU occur in redundant latches. MCU is suppressed when the distance between the redundant latches (D) is increased. Total collected charge decreases by 50% by placing the well contacts adjacent to the redundant latches at which the distance between well contacts and redundant latches is 1.0 μm. Total collected charge of the under latch decreases by 90% when the well contacts are placed between the redundant latches. The ratio of MCU to SEU decreases to 0.073% in this kind of layout structure. According to the results of neutron experiments and device simulations, the ratio of MCU to SEU decreases by increasing the distance of latches D. The fitting lines are influenced by $D^{-1.67}$ and $D^{-2.07}$ by experiments and simulations respectively. Experimental results also show that MCU rates drastically reduce by inserting well-contact arrays under supply and ground rails. MCU is suppressed effectively by increasing the density of well contacts.

Finally, the alpha particle and neutron induced SERs are evaluated by irradiation experiments and Monte-Carlo based simulation: PHITS-TCAD. The 65-nm SOTB and 28-nm UTBB structures are used in our estimation. In the SOTB structure, the alpha cross section increases 18x by reducing the supply voltage from 1.2 V to 0.4 V. In the UTBB structure, the alpha cross section increases 2.5x by reducing the supply voltage from 0.45 V to 0.4 V. The SERs of the 28-nm UTBB is 1/15 of the 65-nm SOTB when VDD is 0.4 V. There is no error occurrence in 28-nm UTBB according to the neutron experimental results. The simulation results are also consistent with the neutron irradiation experimental results. According to the PHITS-TCAD simulation results, the SERs of 65-nm FD-SOI structure are decreased by 20% when the thickness

of BOX region are increased from 10 nm to 25 nm. However, the SERs of 28-nm FD-SOI are decreased by 10% when the BOX region are increased to 25 nm. The PBE is suppressed by thicker BOX regions. By applying 1.0 V reverse bias, the SERs of the SOTB structure become half while that becomes 8x in the UTBB structure. As the technology downscaling, the sensitive volume is decreased. It is much harder to turn on the parasitic bipolar transistor in 28-nm UTBB structure than in 65-nm SOTB structure.

This thesis focus on projection and evaluation of SERs in the radiation-hardened circuit by device and physical level simulations. The SERs of redundant latch circuit structures, layout structures and FD-SOI structures are evaluated. A high accurate Monte-Carlo based simulation methodology is also proposed to project the soft error tolerance without the irradiation experiment. In the future work, the evaluation of soft error tolerance on the ultra scaled processes such as 10-nm FinFET is necessary. Furthermore, with the continuation of technology downscaling, the sensitive volumes and the charge collection mechanisms in PHITS-TCAD simulation also should be analyzed. It can increase the accuracy of simulation result.

Acknowledgment

First of all, I would like to express my special appreciation and thanks to my adviser Prof. Kazutoshi Kobayashi, he has been a tremendous mentor for me. his encourages my research and allows me to grow as a research scientist.

I would like to express my appreciation to Prof. Masahiro Yoshimoto and Prof. Yuichi Kado and Prof. Akira Hiroki in Kyoto Institute of Technology for detailed review and insightful suggestions.

I would like to demonstrate my gratitude to Dr. Jun Furuta in Kyoto Institute of Technology for his invaluable help in the research.

I would like to express my sincere gratitude to Dr. Taiki Uemura in Samsung Electronics for his invaluable suggestions in the research.

I would like to demonstrate my gratitude to Dr. Shinichiro Abe in JAEA for his invaluable suggestions for PHITS.

I would like to express my sincere gratitude to all the people who give invaluable suggestions and helps in my research.

Finally, I would like to express my appreciation to my family, especially my wife Ting. It is hard for me to finish my research without her supports in my life.

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